CV: Adnan Aziz

ACES 6.120
The University of Texas
Austin, TX 78712

Phone: (512) 475-9774
Email: adnan@ece.utexas.edu
URL: www.ece.utexas.edu/~adnan

Interests Design and analysis of digital integrated circuits, with an emphasis on communication applications.

Education

- **Ph.D.,** Electrical Engineering and Computer Sciences, May 1996, U.C. Berkeley, CA.
- **B.Tech.,** Electrical Engineering, May 1989, Indian Institute of Technology at Kanpur.

Professional Experience

Consultant, Qualcomm, Jun 05–Aug 06. Design and verification of a high-performance DSP.

Research Scientist, IBM Austin Research Laboratory, May 02–Aug 02. Verification of high-performance memory arrays.

Associate Professor, Department of Electrical and Computer Engineering, University of Texas, Austin, Sep 01–present. Research and teaching in computer engineering.

Research Scientist, Interwoven.com, Jun 00–Aug 00. Design and implementation of graph algorithms for data mining.

Visiting Professor, CAD Group, University of California, Berkeley, May 98–Aug 98. Design and verification of deep submicron integrated circuits.

Research Scientist, Advanced Technology Group, Synopsys, Inc., May 97–Aug 97. Formal verification of high-level designs.

Assistant Professor, Department of Electrical and Computer Engineering, University of Texas, Austin, Jan 96–Aug 01. Research and teaching in computer engineering.

Graduate Research Assistant, VLSI CAD Group, U.C. Berkeley, May 91–Dec 95. Research in logic synthesis and formal verification.

Graduate Student Instructor, U.C. Berkeley, Jan 91–May 91. Teaching C and assembly language.

Courses Taught

EE382N VLSI Communication Systems — Graduate course in VLSI implementation of communication systems. Topics included review of analog and digital CMOS design, digital filtering, error-correcting codecs, switch fabrics, switch and link scheduling, and system-level design.

EE382M VLSI-1 — Graduate course in digital CMOS design. Topics included CMOS fabrication, MOS physics, circuit design, clocking, datapath, RAMs, and scaling.

EE382N Interconnection Networks — Graduate course in high-speed switching systems. Topics included architectures, packet classification, fabrics, switch and link scheduling, and system-level design.

EE382M Logic Synthesis — Graduate course in the theory and practice of automatically optimizing digital circuits. In addition to fundamental combinatorial optimization algorithms, students were introduced to a number of CAD tools and Hardware Description Languages.

EE382M Formal Verification — Graduate course in the theory and practice of automatically verifying digital designs. In addition to fundamental modeling and analysis techniques, students were exposed to a number of commercial and academic verification tools.

EE397K High-Performance Processor Design — Graduate course on processor design, stressing the close relationship between the high-level design process, low-level implementation details, and the associated CAD methodology. (Taught jointly with researchers from IBM Austin Research Laboratory.)

EE360E Computing Fundamentals — Undergraduate course on data structures (lists, arrays/matrices, stacks/queues, hash tables, trees, graphs), algorithm design principles (greedy approaches, divide-and-conquer, dynamic programming, backtracking/branch-and-bound), and NP-completeness.

EE360C Data Structures in `C++` — Undergraduate course covering Object Oriented Programming using `C++` and elementary data structures.

EE360R VLSI Design — Undergraduate course covering CMOS VLSI design flow, including manufacturing technology, circuits, logic, memories, architecture, and associated CAD methodology.

Academic Honors and Awards

- Outstanding Faculty Award, CD Program, 2006.
- Fujitsu Research Award, $6,000, 2000. (Joint with Prof. N. Touba.)
- IBM Research Fellowship, $25,000, 1999.
- Synopsys Research Award, $50,000, 1999.
- IBM Research Partnership Award, $60,000, 1997–1999.
- ACM Design Automation Conference Fellowship, $12,000, 1996.

Research Contracts

Lead PI unless otherwise stated.

- GSRC, "Coding Theory for Logic Networks" $160,000, 2006-2009. (co-PI; Prof. Michael Orshansky PI).
- Semiconductor Research Corporation, "Enhancing Simulation with Symbolic Algorithms," $156,000, 2000-2003.
- State of Texas Advanced Research Program, "Theory and Tools for Verifying Digital Systems," $133,000 (no overhead), 1999–2001 (Prof. Allen Emerson co-PI).
- State of Texas Advanced Technology Program, "Synthesis for Pass-Transistor Logic," $119,000 (no overhead), 1998–1999 (Prof. Ross Baldick co-PI).
- NSF Faculty CAREER Development Award, "Formal Methods in VLSI System Design," $210,000, 1997–2001.
  - Additional $25,000 matching IBM Research Partnership Award, 1998
  - Additional $25,000 matching Synopsys Research Award, 2000

Service

- UT committee work — graduate admissions, faculty recruiting, undergraduate student appeals, undergraduate computer engineering curriculum development, software curriculum, computer engineering faculty, graduate studies.
- Program committee member — Austin Conference on Integrated Circuits and Systems (ACISC) 2006-2008, IEEE Hot Interconnects (HotI) 2002-2007, International Conference on Formal Engineering Methods (ICFEM) 2004-2005, ACM Design Automation Conference (DAC) 2004–2005, Design Automation and Test in Europe (DATE) 2003–2004, IEEE Workshop on Signal Processing Systems (SIPS) 2004, IEEE International Conference on Computer Design (ICCD) 1998–2000, ACM Timing Analysis Workshop (TAU) 2000, Conference on Formal Methods in CAD (FMCAD) 1998, Workshop on Symbolic Model Checking (SMC) 1999.
- Panel member — NSF panel on design automation, Washington D.C. 1998, NSF panel on information technology, San Francisco 2000.
- Tutorials at ACM Design Automation Conference, San Francisco CA 1998, VLSI Design Conference, Madras INDIA, 1998.
- Lectures at Microsoft, IBM, Intel, Motorola, Cisco, Lucent, CAE-plus, Cadence, Synopsys, Mentor Graphics, Fujitsu, Semiconductor Research Corporation, Lockheed-Martin, DAC, ICCAD, CAV, ICALP, ICCD, DIMACS, IWLS.

Professional Affiliations

- IEEE Computer Society; Association for Computing Machinery; Mathematical Association of America.

Current Students

PhD H. Mony, X. Wu, S. Bijansky.

MS J. Ammerman.

Former Students

1. F. Zaraket, "Program Analysis with Boolean Solvers," *PhD 2007*. Current with IBM.
2. A. Kesiraju, "An Interconnect Efficient, Reconfigurable Low Density Parity Check Decoder," *MS 2005*. Currently with Sun Microsystems.
3. M. Mohiyuddin, "Code Construction Technique for High-Performance Low-density Parity Check Codes," *MS 2004*. Currently PhD student at UC Berkeley.
4. A. Prakash, "Algorithms and Architectures for High-Performance Switching," *PhD 2004*. Currently with Google Labs, Pittsburgh, PA.
5. S. Chalasani, "A Comparative Study of Three Scheduling Algorithms for Input-queued Switches," *MS 2003*. Currently with Google, Mountain View, CA.
6. J. Yuan, "Symbolic Methods in Simulation Verification," *PhD 2002*. Currently with Jasper Design Automation, Mountain View, CA.
7. T. Khan, "Fast Scheduling Using Windows," *MS 2002*. Currently with Cisco Systems, San Jose, CA.
8. G. Rastogi, "Stateful Packet Classification," *MS 2002*. Currently with Cisco Systems, San Jose, CA.
9. S. Gupta, "Multicast Scheduling for Input-queued Switches with Multiple Queues," *MS 2001*. Currently with Cisco Systems, San Jose, CA.
10. M. Ganai, "Algorithms for Efficient State Space Search," *PhD 2001*. Currently with NEC Research Laboratory, Princeton, NJ.
11. P. Yalagandula, "Automatic Generation of Progress Measures in State Space Search," *MS 2000*.
12. I-M. Liu, "Algorithms for Interconnect Planning and Optimization in Deep-Submicron VLSI Design," *PhD 2000*. Currently with Intel, Austin TX.
13. T.-H. Liu, "BDD-based Logic Synthesis," *PhD 1999*. Currently with Avanti, Fremont CA.
14. P. Gopalakrishnan, "Timing Simulation Using Branching Programs," *MS 1999*.
15. R. Chaudhry, "Area Oriented Synthesis for Pass-Transistor Logic," *MS 1998*. Currently with IBM, Austin TX.
16. R. Chaba, "A Toolkit for Verification with Uninterpreted Functions," *MS 1998*. Currently with Qualcomm, San Diego CA.
17. T. Wongsonegoro, "Hybrid Techniques for Fast Functional Simulation," *MS 1998*. Currently with Synopsys, Mountain View CA

18. W. Hung, "Better Verification Using Symmetries," *MS 1997.* Currently with Intel, Hillsborough OR.
19. K. Sajid, "Symbolic Procedures for a Theory of Equality," *MS 1997.* Currently with Intel, Hillsborough OR.

Patents

- Patent 6,611,947, granted 8.26.2003. Method for determining the functional equivalence between two circuit models in a distributed computing environment. Inventors: J. E. Higgins, V. Singhal, A. Aziz. Assignee: Jasper Design Automation, Inc., Mountain View CA.
- Patent 6,993,730, granted 1.31.2006. "Method for rapidly determining the functional equivalence between two circuit models," Inventors: J. E. Higgins, V. Singhal, A. Aziz. Assignee: Tempus-Fugit. Inc., Albany CA.

Software

- `VIS` — A System for Hardware Verification and Synthesis; currently deployed at hundreds of companies and universities.
- `Azinix` — A System for Network Monitoring and Control; currently an open-source project hosted at `azinix.sourceforge.net`

Publications

Book

B-1 *Constraint-Based Verification.* J. Yuan, C. Pixley, and A. Aziz. Springer, 2006.

Book chapters

BC-1 A. Prakash and A. Aziz, "Binary Decision Diagrams," *Encylopedia of Algorithms*, Springer, 2007.

BC-2 A. Prakash and A. Aziz, "Symbolic Model Checking," *Encylopedia of Algorithms*, Springer, 2007.

Journal papers

J-1 A. Aziz, F. Balarin, R. Brayton, and A. Sangiovanni-Vincentelli, *Sequential Synthesis Using* `S1S`, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **19** (2000), no. 10, 1149-1163.

J-2 A. Aziz, F. Balarin, V. Singhal, R. Brayton, and A. Sangiovanni-Vincentelli, *Equivalances for Fair Kripke Structures*, Chicago Journal of Theoretical Computer Science. Accepted for publication.

J-3 A. Aziz, J. Kukula, T. Shiple, and J. Yuan, *Efficient Control State Space Search*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **20** (2001), no. 2.

J-4 A. Aziz, K. Sanwal, V. Singhal, and R. Brayton, *Model-Checking Continuous Time Markov Chains*, ACM Transactions on Computational Logic **1** (2000), no. 1, 162–170.

J-5 A. Aziz, T. Shiple, V. Singhal, R. Brayton, and A. Sangiovanni-Vincentelli, *Formula Dependent Equivalence for Compositional CTL Model Checking*, Journal of Formal Methods in System Design, September 2002, vol. 21, 193-224.

J-6 J. Baumgartner, T. Heyman, V. Singhal, and A. Aziz, *An Abstraction Algorithm for the Verification of Level-Sensitive Latch-Based Netlists*, Journal of Formal Methods in System Design. 2003, 23(1): 39-65.

J-7 M. Ganai, P. Yalagandula, A. Aziz, A. Kuehlmann, and V. Singhal, *SIVA: A System for Coverage-Directed State Space Search*, Journal of Electronic Testing: Theory and Applications, 17(1), February 2001, 11–27.

J-8 A. Goel, K. Sajid, H. Zhou, A. Aziz, and V. Singhal, *BDD-based Procedures for a Theory of Equality with Uninterpreted Functions*, Journal of Formal Methods in System Design, **22** (2003), no. 7, 205–224.

J-9 J. Kukula, T. Shiple, and A. Aziz, *Techniques for Implicit State Enumeration of EFSMs*, Journal of Formal Aspects of Computing. Accepted for publication.

J-10 T. Liu, A. Aziz, and V. Singhal, *Optimizing Designs Containing Black Boxes*, ACM Transactions on Design Automation of Electronic Systems **6** (2001), no. 4.

J-11 A. Prakash, R. Kotla, T. Mandal, and A. Aziz, *A Reconfigurable Architecture and Associated Synthesis Methodology for High Speed Packet Classification.* IEEE Transactions on Computer-Aided Design, **22** (2003), no. 6, 698–709.

J-12 V. Singhal, C. Pixley, A. Aziz, and R. Brayton, *A Theory of Safe Replacements for Sequential Circuits*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **20** (2001), no. 2.

J-13 V. Singhal, C. Pixley, A. Aziz, S. Qadeer, and R. Brayton, *Sequential Optimization in the Absence of Global Reset*, ACM Transactions on Design Automation of Electronic Systems. In press.

J-14 J. Yuan, K. Albin, A. Aziz, and C. Pixley, *Simplifying Constraint Solving in Random Simulation Generation*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004.

J-15 J. Yuan, K. Schultz, C. Pixley, H. Miller, and A. Aziz, *Automatic Vector Generation Using Constraints and Biasing*, Journal of Electronic Testing: Theory and Applications (2000), 107–120.

J-16 H. Zeineddine, A. K. Singh, A. Aziz, S. Vishwanath, and M. Orshansky, *Generation of Efficient Codes for Realizing Boolean Functions in Nanotechnologies*, ACM Journal on Emerging Technologies in Computing Systems, to appear, 2008.

J-17 H. Zhou and A. Aziz, Buffer Minimization in Pass-transistor Logic. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* **20** (2001),

no. 5.

J-18 H. Zhou, D. F. Wong, I. Liu, and A. Aziz, *Simultaneous Routing and Buffer Insertion with Restrictions on Buffer Locations*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **19** (2000), no. 7, 819–824.

Conference papers

C-1 J. Ammerman, N. Petersen, H. A. Andrade, and A. Aziz. "Digital Video Broadcast Tranceiver Deplyment to Xilinx FPGAs Using LabVIEW." In *Proceedings of the Asilomar Conference on Signals, Systems, and Computers*, Monterey, CA. October 2008.

C-2 A. Aziz, F. Balarin, R. Brayton, S. Cheng, R. Hojati, T. Kam, S. Krishnan, R. Ranjan, A. Sangiovanni-Vincentelli, T. Shiple, V. Singhal, S. Tasiran, and H. Wang. "HSIS: A BDD-Based Environment for Formal Verification." In *Proceedings of the ACM Design Automation Conference*, pages 454–459, June 1994.

C-3 A. Aziz, F. Balarin, R. Brayton, and A. Sangiovanni-Vincentelli. "Sequential Synthesis Using `S1S`." In *Proceedings of the IEEE International Conference on Computer-Aided Design*, pages 612–617, November 1995.

C-4 A. Aziz, F. Balarin, M. DiBenedetto, R. Brayton, A. Saldanha, and A. Sangiovanni-Vincentelli. "Supervisory Control of Finite State Machines." In *Proceedings of the Computer Aided Verification Conference*, pages 279–292, July 1995.

C-5 A. Aziz, F. Balarin, V. Singhal, R. Brayton, and A. Sangiovanni-Vincentelli. "The Temporal Logic of Stochastic Systems." In *Proceedings of the Computer Aided Verification Conference*, pages 155–165, July 1995.

C-6 A. Aziz, J. Kukula, and T. Shiple. "Hybrid Verification Using Saturated Simulation." In *Proceedings of the ACM Design Automation Conference*, pages 615–618, June 1998.

C-7 A. Aziz, A. Prakash, and V. Ramachandran. "A Near Optimal Scheduler for Switch-Memory-Switch Routers." In *Proceedings of the ACM Symposium on Parallelism in Algorithms and Architectures*, June 2003.

C-8 A. Aziz, K. Sanwal, V. Singhal, and R. Brayton. "Verifying Continuous Time Markov Chains." In *Proceedings of the Computer Aided Verification Conference*, pages 269–276, July 1996.

C-9 A. Aziz, T. Shiple, V. Singhal, and A. Sangiovanni-Vincentelli. "Formula-Dependent Equivalence for Compositional CTL Model Checking." In *Proceedings of the Computer Aided Verification Conference*, pages 324–337, July 1994.

C-10 A. Aziz, V. Singhal, F. Balarin, R. Brayton, and A. Sangiovanni-Vincentelli. "Equivalences for Fair Kripke Structures." In *Proceedings of the Colloquium on Automata, Languages, and Programming*, pages 364–375. Springer Verlag, July 1994.

C-11 A. Aziz, V. Singhal, G. M. Swamy, and R. Brayton. "Minimizing Interacting Finite State Machines: A Compositional Approach to Language Containment." In *Proceedings of the IEEE International Conference on Computer Design*, pages 255–261, October 1994.

C-12 A. Aziz, S. Tasiran, and R. Brayton. "BDD Variable Ordering for Interacting Finite State Machines." In *Proceedings of the ACM Design Automation Conference*, pages 283–288, June 1994.

C-13 J. Baumgartner, T. Heyman, V. Singhal, and A. Aziz. "Model Checking the IBM Gigahertz Processor: An Abstraction Algorithm for High Performance Netlists." In *Proceedings of the Computer Aided Verification Conference*, pages 72–83, July 1999.

C-14 J. Baumgartner, A. Tripp, A. Aziz, V. Singhal, and F. Andersen. "An Abstraction Algorithm for the Verification of Generalized C-Slow Designs." In *Proceedings of the Computer Aided Verification Conference*, pages 5–19, July 2000.

C-15 S. Bijansky and A. Aziz. "TuneFPGA: Post-Silicon Tuning of Dual-Vdd FPGAs." In *Proceedings of the Design Automation Conference*, July 2008.

C-16 S. Bijansky and A. Aziz. "Adaptive Voltage Tuning for Dual-Vdd ASICs." In *Proceedings of the Austin Conference on Integrated Circuits and Systems*, May 2008.

C-17 R. Brayton, G. Hachtel, A. Sangiovanni-Vincentelli, F. Somenzi, A. Aziz, S. Cheng, S. Edwards, S. Khatri, Y. Kukimoto, A. Pardo, S. Qadeer, R. Ranjan, S. Sarwary, T. Shiple, G. M. Swamy, and T. Villa. "VIS." In *Proceedings of the Formal Methods in CAD Conference*, pages 248–256, November 1996.

C-18 R. Brayton, G. Hachtel, A. Sangiovanni-Vincentelli, F. Somenzi, A. Aziz, S. Cheng, S. Edwards, S. Khatri, Y. Kukimoto, A. Pardo, S. Qadeer, R. Ranjan, S. Sarwary, T. Shiple, G. M. Swamy, and T. Villa. "VIS: A system for Verification and Synthesis." In *Proceedings of the Computer Aided Verification Conference*, pages 428–432, July 1996.

C-19 R. Chaudhry, T. Liu, A. Aziz, and J. Burns. "Area Oriented Synthesis for Pass-Transistor Logic." In *Proceedings of the IEEE International Conference on Computer Design*, pages 160–167, October 1998.

C-20 M. Ganai and A. Aziz. "Improved SAT-based Bounded Reachability Analysis ." In *Proceedings of the VLSI Design Conference*, January 2002.

C-21 M. Ganai and A. Aziz. "Rarity Based Guided State Space Search." In *Proceedings of the Great Lakes Symposium on VLSI*, March 2000.

C-22 M. Ganai, A. Aziz, and A. Kuehlmann. "Enhancing Simulation with BDDs and ATPG." In *Proceedings of the ACM Design Automation Conference*, pages 385–390, June 1999.

C-23 A. Goel, K. Sajid, H. Zhou, A. Aziz, and V. Singhal. "BDD Based Procedures for a Theory of Equality with Uninterpreted Functions." In *Proceedings of the Computer Aided Verification Conference*, pages 244–255, July 1998.

C-24 S. Gupta and A. Aziz. "Multicast Scheduling for Switches with Multiple Input-queues." In *Proceedings of the IEEE Hot Interconnects Conference*, Stanford CA, August 2002.

C-25 J. Kukula, T. Shiple, and A. Aziz. "Techniques for Implicit State Enumeration of EFSMs." In *Proceedings of the Formal Methods in CAD Conference*, pages 469–482, November 1998.

C-26 I. Liu and A. Aziz. "Delay Constrained Optimization by Simultaneous Fanout Tree Construction, Buffer Insertion/Sizing and Gate Sizing." In *Proceedings of the IEEE International Conference on Computer Design*, October 2000.

C-27 I. Liu, A. Aziz, M. Wong, and H. Zhou. "An Efficient Buffer Insertion Algorithm for Large Networks Based on Lagrangian Relaxation." In *Proceedings of the IEEE International Conference on Computer Design*, pages 210–215, October 1999.

C-28 I. Liu, T. Chou, A. Aziz, and D. F. Wong. "Zero-skew Clock Tree Construction by Simultaneous Routing, Wire Sizing, and Buffer Insertion." In *ACM International Symposium on Physical Design*, pages 33–38, April 2000.

C-29 I. Liu, H. Chen, A. Aziz, and D. F. Wong. "Integrated Power Supply Planning and Floorplanning." In *ASP Design Autmation Conference*, January 2001.

C-30 I. Liu, H. Zhou, M. Wong, and A. Aziz. "Meeting Delay Constraints in DSM by Minimal Repeater Insertion." In *Proceedings of the Design Automation and Test in Europe Conference*, pages 436–440, March 2000.

C-31 T. Liu, M. Ganai, A. Aziz, and J. Burns. "Performance Driven Synthesis for Pass-Transistor Logic." In *VLSI Design Conference*, pages 372–377, January 1999.

C-32 T. Liu, K. Sajid, A. Aziz, and V. Singhal. "Optimizing Designs Containing Black Boxes." In *Proceedings of ACM the Design Automation Conference*, pages 113–116, June 1997.

C-33 Y. Luo, T. Wongsonegoro, and A. Aziz. "Hybrid Techniques for Fast Functional Simulation." In *Proceedings of the ACM Design Automation Conference*, pages 664–667, June 1998.

C-34 A. Mehrotra, S. Qadeer, V. Singhal, A. Aziz, R. Brayton, and A. Sangiovanni-Vincentelli. "Sequential Optimisation without State Space Exploration." In *Proceedings of the IEEE International Conference on Computer-Aided Design*, pages 208–215, November 1997.

C-35 B. Mohd, A. Aziz, and E. Schwartzlander. "The Hazard-Free Superscalar Pipeline Fast Fourier Transform Algorithm and Architecture." In *Proceedings of the IFIP International Conference on VLSI*, Atlanta GA, October 2007.

C-36 B. Mohd, H. Saleh, A. Aziz, and E. Schwartzlander. "Contention-Free Switch-Based Implementation of 1024-point Radix-2 Fourier Transform Engine." In *Proceedings of the IEEE International Conference on Computer Design*, Lake Tahoe CA, October 2007.

C-37 B. Mohammad, P. Bassett, J. Abraham, and A. Aziz. "Cache Organization for Embedded Processors: CAM vs. SRAM." In *Proceedings of the IEEE System-on-Chip Conference*, September 2006.

C-38 B. Mohammad, P. Bassett, J. Abraham, and A. Aziz. "Low Power Word-line Logic for SRAM Memory." In *Proceedings of the Austin Conference on Integrated Circuits and Systems*, May 2006.

C-39 B. Mohammad, S. Bijansky, J. Abraham, and A. Aziz. "Adaptive SRAM-based Memory for Low Power and High Yield." In *Proceedings of the IEEE Conference on Computer Design*, October 2008.

C-40 B. Mohammad, K. Lin, P. Bassett, and A. Aziz. "A 65nm Level-1 Cache for Mobile Applications." In *Proceedings of the IEEE International Conference on Microelectronics*, December 2008.

C-41 M. Mohiyuddin, A. Prakash, A. Aziz, and W. Wolf. "Synthesizing Interconnect-Efficient Low Density Parity Check Codes." In *Proceedings of the ACM Design Automation Conference*, San Diego, CA. June 2004.

C-42 M. Mohiyuddin, A. Prakash, X. Wu, and A. Aziz. "A Reconfigurable Architecture and Associated CAD Algorithm for Multirate LDPC Decoding." In *Proceedings of the Asilomar Conference on Signals, Systems, and Computers*, Monterey, CA. October 2005.

C-43 M. Mondal, X. Wu, Y. Massoud, and A. Aziz. "Reliability Analysis for On-chip Networks." In *Proceedings of the IEEE Nano-net Conference*, Lausanne, Switzerland, September 2006.

C-44 M. Mondal, T. Ragheb, X. Wu, Y. Massoud, and A. Aziz. "Provisioning On-Chip Networks under Buffered RC Interconnect Delay Variations ." In *Proceedings of the IEEE International Symposium on Quality Electronic Design*, San Jose CA, March 2007.

C-45 H. Mony, J. Baumgartner, and A. Aziz. "Exploiting Constraints in Transformation-Based Verification." In *Proceedings of CHARME*, Saarbrücken, Germany. October 2005.

C-46 H. Mony, J. Baumgartner, and A. Aziz. "Optimal Constraint-Preserving Netlist Simplification." In *Proceedings of FMCAD*, Portland OR, November 2008.

C-47 R. Panigrahy, A. Nemat, A. Prakash and A. Aziz. "Weighted Random Matching." In *Proceedings of the IEEE High-performance Switching and Routing Workshop*, Tempe AZ, June 2004.

C-48 A. Prakash and A. Aziz. "A Middle Ground Between CAMs and DAGs for High-speed Packet Classification." In *Proceedings of the IEEE Hot Interconnects Conference*, Stanford CA, August 2002.

C-49 A. Prakash and A. Aziz. "OC-3072 Packet Classification Using BDDs and Pipelined SRAMs." In *Proceedings of the IEEE Hot Interconnects Conference*,

Stanford CA, August 2001.

C-50 A. Prakash, A. Aziz, and V. Ramachandran. "Randomized Parallel Schedulers for Switch-Memory-Switch Routers: Analysis and Numerical Studies." In *Proceedings of the IEEE Infocom*, June 2004.

C-51 A. Prakash, S. Sharif, and A. Aziz. An $O(\lg^2 n)$ algorithm for output queuing. In *IEEE Infocom*, New York, NY, June 2002.

C-52 C. Pixley, V. Singhal, A. Aziz, and R. Brayton. "Multi-level Synthesis for Safe Replaceability". In *Proceedings of the IEEE International Conference on Computer-Aided Design*, pages 442–449, November 1994.

C-53 J. Schneider, D. Patent, F. Dankert, S. Gokhale, and A. Aziz "A Wireless Transceiver for USB 2.0". In *Proceedings of the Austin Conference on Integrated Systems & Circuits*, May 2006.

C-54 T. Shiple, A. Aziz, F. Balarin, S. Cheng, R. Hojati, T. Kam, S. Krishnan, V. Singhal, H. Wang, R. Brayton, and A. Sangiovanni-Vincentelli. "Formal Design Verification of Digital Systems." In *SRC TECHCON*, September 1993.

C-55 A. K. Singh, H. Zeineddine, A. Aziz, S. Vishwanath and M. Orshansky. "A Heterogeneous CMOS-CNT Architecture utilizing Novel Coding of Boolean Functions." In *IEEE/ACM Symposium on Nanoscale Architectures*, October, 2007.

C-56 V. Singhal, C. Pixley, A. Aziz, and R. Brayton. "Exploiting Power-up Delay for Sequential Optimization." In *Proceedings of the European Design Automation Conference*, pages 54–59, September 1995.

C-57 S. Srinivasan, P. Chhabra, P. Jaini, A. Aziz, and L. K. John. "Formal Verification of a Snoop Based Cache Coherence Protocol using Symbolic Model Checking." In *VLSI Design Conference*, pages 288–293, January 1999.

C-58 P. Yalagandula, V. Singhal, and A. Aziz. "Automatic Lighthouse Generation for Directed State Space Search." In *Proceedings of the Design Automation and Test in Europe Conference*, pages 237–242, March 2000.

C-59 J. Yuan, K. Schultz, C. Pixley, H. Miller, and A. Aziz. "Modeling Design Constraints and Biasing in Simulation Using BDDs." In *Proceedings of the IEEE International Conference on Computer-Aided Design*, pages 584–589, November 1999.

C-60 J. Yuan, J. Shen, J. Abraham, and A. Aziz. "On Combining Formal and Informal Verification." In *Proceedings of the Computer Aided Verification Conference*, pages 376–387, July 1997.

C-61 X. Wu, A. Prakash, M. Mohiyuddin, and A. Aziz. " Scheduling Traffic Matrices On General Switch Fabrics." In *Proceedings of the IEEE Hot Interconnects Conference*, Stanford CA, August 2006.

C-62 X. Wu, T. Ragheb, Y. Massoud and A. Aziz. "Implementing DSP Algorithms with On-Chip Networks ." In *Proceedings of the ACM/IEEE International Symposium on Networks-on-Chip*, Princeton NJ, May 2007.

C-63 J. Yuan, K. Albin, A. Aziz, and C. Pixley. "Constraint Synthesis for Environment Modeling in Functional Verification." In *Proceedings of the ACM Design Automation Conference*, June 2003.

C-64 J. Yuan, K. Albin, A. Aziz, and C. Pixley. "A Framework for Constrained Functional Verification." In *Proceedings of the IEEE International Conference on Computer-Aided Design*, November 2003.

C-65 J. Yuan, K. Albin, A. Aziz, and C. Pixley. "Simplifying Constraint Solving in Random Simulation Generation." In *Proceedings of the IEEE International Conference on Computer-Aided Design*, November 2002.

C-66 F. Zaraket, J. Baumgartner, and A. Aziz. "Scalable Compositional Minimization via Static Analysis." In *Proceedings of the IEEE International Conference on Computer-Aided Design*, November 2005.

C-67 F. Zaraket, A. Aziz and S. Khurshid. "Sequential Circuits for Relational Analysis." In *Proceedings of the IEEE International Conference on Software Engineering*, Minneapolis MN, May 2007.

C-68 F. Zaraket, J. Pape, A. Aziz, M. Jacome, and S. Khurshid. "COSE: A Technique for Co-optimizing Embedded Systems." In *Proceedings of the IEEE/ACM International Conference on Automated Software Engineering*, Austin TX, September 2007.

C-69 F. Zaraket, A. Aziz and S. Khurshid. "Sequential Circuits for Program Analysis." In *Proceedings of the IEEE/ACM International Conference on Automated Software Engineering*, Atlanta GA, September 2007.

C-70 H. Zhou and A. Aziz. "Buffer Minimization in Pass-transistor Logic." In *International ACM Symposium on Physical Design*, pages 105–110, April 2000.

C-71 H. Zhou, M. Wong, I. Liu, and A. Aziz. "Simultaneous Routing and Buffer Insertion with Restrictions on Buffer Locations." In *Proceedings of the Design Automation Conference*, pages 96–99, June 1999.

Refereed workshop papers

WS-1 A. Aziz, F. Balarin, R. Brayton, and A. Sangiovanni-Vincentelli. "Synthesizing Interacting Finite State Machines." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, May 1995.

WS-2 A. Aziz, R. Brayton, F. Balarin, and V. Singhal. "Timing-Safe Replaceability for Combinational Designs." In *ACM Internation Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pages 121–128, November 1995.

WS-3 A. Aziz, A. Singh, M. Orshansky, and S. Vishwanath. "Realizing Boolean Functions in Nano-technologies: Capacity and Code Design." In *Information Theory and Applications Workshop*, San Diego, February 2007.

WS-4 A. Aziz, S. Tasiran, and R. Brayton. "BDD Variable Ordering for Systems of

Interacting Finite State Machines." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, May 1993. Poster presentation.

WS-5 R. Chaudhry, T. Liu, A. Aziz, and J. Burns. "Area Oriented Synthesis for Pass-Transistor Logic." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, pages 169–176, May 1998.

WS-6 M. Ganai and A. Aziz. "Efficient Coverage Directed State Space Search." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, pages 267–275, May 1998.

WS-7 W. Hung, A. Aziz, and K. McMillan. "Heuristic Symmetry Reduction for Invariant Verification." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, May 1997.

WS-8 I. Liu, A. Aziz, and M. Wong. "Buffering Large Networks by Lagrangian Relaxation." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, May 1999.

WS-9 I. Liu, T. Liu, H. Zhou, and A. Aziz. "Simultaneous PTL Buffer Insertion and Sizing for Minimizing Elmore Delay." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, pages 162–168, May 1998.

WS-10 T. Liu, A. Aziz, and J. Burns. "Performance Driven Synthesis for Pass-Transistor Logic." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, pages 255–259, May 1998. Poster presentation.

WS-11 A. Prakash, R. Kotla, T. Mandal, and A. Aziz. "A Reconfigurable Architecture and Associated Synthesis Methodology for High Speed Packet Classification." In *Proceedings of the ACM/IEEE Workshop on Workshop on Logic Synthesis*, June 2002.

WS-12 R. Ranjan, A. Aziz, R. Brayton, B. Plessier, and C. Pixley. "Efficient BDD Algorithms for FSM Synthesis and Verification." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, May 1995. Poster presentation.

WS-13 J. Yuan, K. Albin, A. Aziz, and C. Pixley. "Simplifying Constraint Solving in Random Simulation Generation." In *Proceedings of the ACM/IEEE Workshop on Workshop on Logic Synthesis*, June 2002. Poster presentation.

WS-14 J. Yuan, K. Shultz, J. Havlicek, K. Albin, and A. Aziz. "A Method for Synthesizing Boolean Constraints." In *Proceedings of the ACM/IEEE Workshop on Workshop on Logic Synthesis*, June 2002. Poster presentation.

WS-15 F. Zaraket, A. Aziz, and S. Khurshid. "Applying a Sequential Circuit Solver to Alloy." In *Proceedings of the First Alloy Workshop*, Portland OR, October 2006.

WS-16 H. Zhou and A. Aziz. "Buffer Minimization in Pass Transistor Logic." In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, pages 155–159, May 1998.

WS-17 H. Zhou, V. Singhal, and A. Aziz. "How Powerful is Retiming?" In *Proceedings of the ACM/IEEE International Workshop on Logic Synthesis*, pages 111–125, May 1998.

Tech reports

TR-1 A. Aziz, F. Balarin, R. Brayton, and A. Sangiovanni-Vincentelli. "Synthesizing Interacting Finite State Machines." Technical Report UCB/ERL M94/96, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1994.

TR-2 A. Aziz, T. Shiple, V. Singhal, R. Brayton, and A. Sangiovanni-Vincentelli. "Formula Dependent Equivalences for Compositional CTL Model Checking." Technical Report UCB/ERL M95/78, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1995.

TR-3 A. Aziz, V. Singhal, and R. Brayton. "Verifying Interacting Finite State Machines: Complexity Issues." Technical Report UCB/ERL M93/52, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1993.

TR-4 A. Aziz, V. Singhal, G. M. Swamy, and R. Brayton. "Minimizing Interacting Finite State Machines." Technical Report UCB/ERL M93/68, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1993.

TR-5 A. Aziz, V. Singhal, G. M. Swamy, and R. Brayton. "Minimizing Interacting Finite State Machines." Technical Report UCB/ERL M93/68, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1993.

TR-6 A. Aziz, S. Tasiran, and R. Brayton. "BDD Variable Ordering for Interacting Finite State Machines." Technical Report UCB/ERL M93/71, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1993.

TR-7 A. Aziz, S. Tasiran, and R. Brayton. "BDD Variable Ordering for Interacting Finite State Machines." Technical Report UCB/ERL M93/71, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1993.

TR-8 C. Pixley, V. Singhal, A. Aziz, and R. Brayton. "Multi-Level Synthesis for Safe Replaceability." Technical Report UCB/ERL M94/31, Electronics Research Lab, 1994.

TR-9 R. Ranjan, A. Aziz, B. Plessier, C. Pixley, and R. Brayton. "Efficient Formal Design Verification: Data Structure + Algorithms." Technical Report UCB/ERL M94, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1994.

TR-10 V. Singhal, C. Pixley, A. Aziz, and R. Brayton. "Delaying Safeness for More Flexibility." Technical Report UCB/ERL M95/5, Electronics Research Lab, Univ. of California, Berkeley, CA 94720, 1995.