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ACES 6.120
Office Hours: MW 10:00-11:00am — ACE 6.120

EE 382M – Synthesis of Digital Systems
Spring 2007
Unique No: 16525
Lecture: MW 11:00-12:30pm — ENS 116

Description:

This course aims to study the use of computers to automate the process of digital design, specifically the problem of design synthesis.

We will begin by reviewing the basic definitions of Boolean logic and digital systems, continued by an in-depth study of optimization techniques for PLAs and general combinational logic.

This will be followed by a survey level treatment of a number of topics in logic synthesis, including logic fault testing, technology mapping, timing analysis, performance optimization, and synthesis for low-power.

Afterwards, we will focus on sequential designs. Specifically, representational issues, flexibility available for synthesis, state assignment and minimization, retiming, and FSM verification will be covered.

Prerequisites:

This course is intended for graduate students with a knowledge of digital design and C programming, and a reasonable degree of mathematical sophistication.

Recommended texts:

1. S. Hassoun, T. Sasao, and R.K. Brayton, "Logic Synthesis and Verification", Kluwer Academic Publishers, 2001.
2. G.D. Hachtel and F. Somenzi, "Logic Synthesis and Verification Algorithms", Kluwer Academic Publishers, 1996.
3. Giovanni de Micheli, "Synthesis and Optimization of Digital Systems", McGraw Hill, 1994.

Format/Evaluation:

Approximately 8 homeworks will be assigned; these will range from devising algorithms to design and synthesis, and will be worth 30% of your grade. There will be two midterms worth a combined 35% of your grade; a substantial final project will constitute the remainder of the grade.

Where does this course fit in?

In conjunction with this course, you might consider taking: *VLSI-1* this is a foundations graduate course; *Computer Architecture*; and/or *CAD for ICs*. After taking this course you might consider taking, *Verification of Digital Systems*, *Fault Tolerant Computing*; and/or *Digital Systems Simulation*.

Web site: All material related to the course is available at
`http://www.ece.utexas.edu/~adnan/syn-07`

Tentative Schedule

	Material
1.17	Role of synthesis in VLSI Design
	Boolean functions
1.22	Representations
1.24	BDDs
	2-level Logic Minimization
1.29	BDDs
1.31	Exact 2-level minimization — Quine-McKluskey
2.5	Heuristic minimization: ESPRESSO
2.5	Heuristic minimization: ESPRESSO
	Multi-level logic minimization
2.7	Multi-level logic: definitions
2.12	Factoring, substitution, elimination
2.14	Factoring, substitution, elimination
2.19	Don't cares and node simplification
2.21	Don't cares and node simplification
2.26	Technology mapping for area
2.28	Technology mapping for area
3.5	Project descriptions & midterm review
3.7	Midterm 1
	Timing
3.19	Technology mapping for performance
3.21	ATPG
3.26	Timing analysis – 1
3.28	Timing optimization – 2
4.2	Timing optmization – 1
4.4	Timing optimization – 2
	Sequential Logic Synthesis
4.9	Representations
4.11	State minimization
4.16	Retiming – 1
4.18	Retiming – 2
	Low power design
4.23	Low power – 1
4.25	Low power – 2
4.30	Midterm 2
5.2	Review/Guest Lecture

NOTE: All departmental, college and university regulations concerning drops will be followed. The University of Texas at Austin provides upon request appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD.