Identification of Feasible Topologies for Multiple-Input DC–DC Converters

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Abstract—This letter studies single-input dc–dc converter topologies that are suitable to be expanded into their multiple-input converter version. The analysis is based on several assumptions, restrictions, and conditions, including the goal of minimizing the total number of components and the use of at least one forward-conducting bidirectional blocking switch in each input leg. These conditions may affect the outcome of the multiple-input converter synthesis and lead to different configurations from those suggested before in the literature. Although simultaneous power delivery from all sources is not required, it should be possible to independently control the power drained from each input with some degree of freedom. The letter lists four rules that must be observed in order to be able to realize a multiple-input converter from its single-input version. These rules are used to identify the only feasible input cell that complies with all assumptions and conditions. Unfeasible input cells are also shown. The letter also identifies some additional feasible input cells if some of the assumptions and conditions are relaxed. These input cells are used to suggest several multiple-input converter topologies. Among them, six topologies, including versions of the single-ended primary inductance converter and the Ćuk converters, are introduced through their circuit schematic.

Index Terms—Converter realization rules, feasible dc–dc converter topologies, independent input power control, input cells, multiple-input converters.

I. INTRODUCTION

THIS LETTER identifies multiple-input dc–dc converters (MICs) feasible topologies, and lists some basic rules that allow determining if a given single-input converter can be expanded into a multiple-input circuit. Multiple-input converters have been proposed as a cost-effective and flexible way to interface various sources and, in some cases, energy-storage devices, with a load. The topologies described in these works can be divided into two categories according to whether the connection between inputs is performed through a magnetic coupling in a transformer or not. Although connecting various inputs through a transformer core, as in [1]–[8], is an acceptable solution for MICs, these topologies will not be considered in this letter because the link between inputs is performed in a trivial way with an intermediate ac–ac conversion. This letter considers converters with only direct dc–dc conversion, such as the ones discussed in [8]–[19].

In the past, proposed MICs with direct dc–dc conversion were based on single-input basic topologies. One of these, a current-sourced MIC based on the boost converter topology, discussed in [8]–[10], will not be considered in this letter because the connection between inputs also occurs in a trivial way through a common output capacitor. Other alternatives are derived from a buck converter [11], [12], or from the buck–boost [10], [13], [14] and the fly-back [15]–[18] converters. More MIC options are suggested in [19].

The discussion in this letter is based on [20] because a broad set of dc–dc converter topologies was introduced in [20] without intermediate transformations into ac. First, the letter explains the assumptions, restrictions, and conditions used in the analysis. Second, based on four basic rules, this letter presents feasible and unfeasible input cells that realize MICs from their single-input versions. Unfeasible input cells create multiple-input topologies that do not comply with at least one of the conditions required in multiport topologies, such as independent power flow control in each leg. The set of rules used to identify feasible input cells may also be used as the basis for a computational method to automatically detect feasible configurations, with an approach similar to the one used in [21]. However, since the analysis shows that feasible topologies are a significant minority of the possible configurations, the computational approach is not required to achieve this letter's goals. Third, the discussion lists single-input topologies in [20] that are suitable to be expanded into MICs. The analysis yields an alternative set of multiple-input converters from those suggested in [19] because the basic configurations derived from [20] are more numerous than those in [19], and because the analysis here does not require simultaneous power drained from each source. In addition, it also simplifies the work in [19]. Finally, the letter introduces some new MIC topologies obtained as a result of the study and verifies their operation with simulations.

II. DISCUSSION

A. Assumptions, Restrictions, and Conditions

The analysis considers several assumptions and restrictions regarding the topology and operation of the MICs. First, to simplify the study, the analysis restricts power in all converter inputs to flow in only one direction: from source to load. Second, this analysis does not include MICs with a trivial connecting point between input legs, such as linking the inputs by paralleling them at the output capacitor or by using an alternating flux in a transformer core. Third, the MIC designs minimize the total number of components by maximizing the number of common components among the inputs, hence reducing the number of components in each individual input cell. The assumption also implies that only the simplest of the topologies among a family of similar converters is included in the

analysis. For example, fly-back converters are not analyzed because they are considered to be derived from buck–boost converters. Minimization of the total number of components may reduce cost in most standard designs. However, reliability can be negatively affected by this assumption. MICs do not necessarily improve reliability as suggested in [14] because common components act as single points of failure for the entire converter. Yet, a system using MICs can improve availability with respect to standard architectures if there are diverse input sources and if the MICs have modular designs. It is also assumed that the converters are operating in continuous conduction mode with ideal components and are trying to regulate some output voltage.

The last assumption is to consider that all input cell switches are forward conducting and bidirectional blocking (FCBB). This assumption is an important difference from [19]. With FCBB, the number of common components among inputs can be maximized, but a restriction appears on the power supplied by the sources because FCBB switches may prevent simultaneous power transfer from all sources to the load—a condition in [19]. It can also be argued that implementation of FCBB functionalities with some devices, such as MOSFETs, may lead to an additional component, a diode, which contradicts the assumption of minimizing the total number of components. However, the option of not using FCBB, such as in [19], requires more components. In addition, the reverse blocking diode added when some switches, such as MOSFETs, are used is already part of the device included when bidirectional power flow is sought—a common functionality implemented in MICs.

The aforementioned assumptions and restrictions imply some conditions. One is that converters with only direct dc–dc conversion are considered here. Hence, forward converters are not included in the discussion. Additional conditions are required to meet operational needs. MICs should be able to operate when the sources at each input leg have different nominal voltages. In the analysis, it is also required that there must be some degree of freedom in controlling the power flow in each input leg, i.e., even if all but one of the inputs are limited in the power that can be drained from the corresponding source, it should still be possible to freely control the power input at each leg within a certain range. With FCBB switches in each input leg, free power control is constrained not only because the sum of all input powers must equal the output power, but also because sources may not deliver power simultaneously.

B. Rules for Identifying Feasible Multiple-Input DC–DC Converter Topologies

All MIC topologies are derived from single-input versions in which the converter is divided into an input stage and an output stage. The MIC is realized by multiplying the number of input stages (i.e., the input cells), and connecting all of them to a common output stage. This section formulates some basic rules that need to be observed when realizing the MIC from the single-input version so that the assumptions,
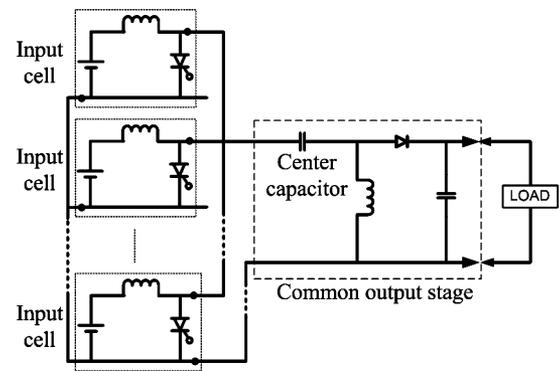
Fig. 1. Unfeasible SEPIC converter with center capacitor in the common output stage.

restrictions, and conditions listed in the previous section are met.

Rule 1—Required Input Cell Components: All feasible input cells must contain at least one independently controlled FCBB switch. This rule is derived from the condition requiring some degree of freedom in the control of the power delivered by each source. Since each input cell includes at least one FCBB switch, the common stage must have at least one dependent switch, i.e., a common diode. This rule does not imply any limitation in the number of passive components. However, the assumption of minimizing the total number of components translates into minimizing the number of components in each input cell. Thus, passive components should be included in each input cell only when it is not possible to have them in the common stage, as it happens with the input inductor in current source converters.

Rule 2—Independent Switches Redundancy: To meet the condition of independent control in each input, the connection of the input cells to the common stage should not lead to redundant switches, i.e., independent controlled switches in parallel. Hence, this rule implies that both ends of the independent switch cannot be connection terminals of the input cell.

Rule 3—Common-Stage Capacitor Voltage: In the case that an MIC's single-input original topology has a center capacitor, such as in the single-ended primary inductance converter (SEPIC) and the Ćuk converters, then the average voltage of the capacitor should not depend on the input voltage. For example, as Fig. 1 indicates, the average voltage in the common-stage center capacitor of a multiple-input SEPIC converter would equal all the input voltages simultaneously. Thus, MIC realization is unfeasible unless the assumption of minimizing the total number of components is relaxed and the center capacitor is instead spread among each input cell. Even when the assumption of maximizing the number of common components is relaxed, some topologies may still be unfeasible if both terminals of the capacitor in each input cell are connection points to the common stage and if each of these capacitors average voltage depends on their respective source voltage.

Rule 4—Source Terminals: Both ends of the input source should not be terminals of the input cell. Otherwise, a short
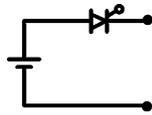
Fig. 2.   Feasible input cell. Connection terminals are marked with the black dots.
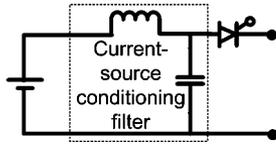
Fig. 3.   Current-source conditioning filter for the feasible input cell in Fig. 2.
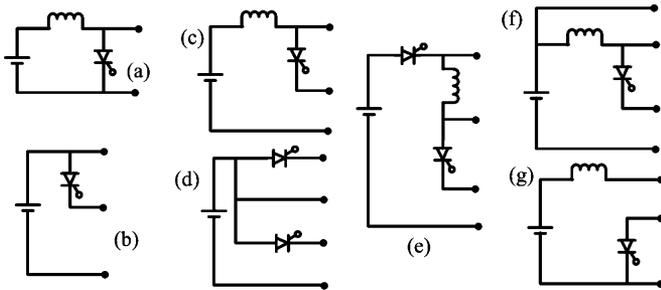
Fig. 4.   Unfeasible cells. Connection terminals are marked with black dots.

Fig. 5.   Additional feasible cells if the assumption of common components maximization is relaxed in the corresponding unfeasible input cells in Fig. 4. Connection terminals are marked with black dots.

circuit would be created at the time of interconnecting input cells with sources with dissimilar voltage.

C. Basic Input Cells

The analysis using the four rules mentioned in Section II-B leads to some always feasible input cells, some always unfeasible input cells, and some alternative input cells that lead to feasible topologies if the assumption of minimizing the total number of components is relaxed and the center capacitor in the common stage is spread into each of the input cells. The input cell that always produces feasible MIC topologies is shown in Fig. 2. This cell is found in voltage source converters, such as the buck converter. Its main disadvantage is that it produces a switched input current that is not suitable for some sources, such as fuel cells. However, this disadvantage may be overcome by adding an input current-source conditioning filter, displayed in Fig. 3.

Unfeasible input cells are more numerous, as indicated in Fig. 4. All these cells violate at least rule 2, as indicated by the presence of input cell terminals that coincides with both terminals of the same switch. Most unfeasible cells for converters with four switches in [20] are not included in Fig. 4 for two reasons. One is that the input cells present the case of an independently controlled switch that is separated from the other components of the input cell, i.e., both switch terminals are connecting points to the common stage. For example, this situation is observed with switch S3 in configuration H2 in [20]. The other reason is that the input cell can be reduced to one of the cases in Fig. 4. For example, the input cell in configuration I1 can be reduced to the input cell in Fig. 4(g).

In reality, many of the unfeasible input cells in Fig. 4 also tend to violate rule 3 because the average voltage of any common-stage center capacitor connected to the input-source terminal, either directly or through an inductor, depends on the input voltage. This observation indicates that a way of making unfeasible cells feasible is to distribute the center capacitor in the common stage into each of the input cells. The result is the cells shown in Fig. 5. These input cells are in correspondence to the equally named input cells in Fig. 4. If diverse input sources are used, placing the center capacitor in each of the input cells has the added advantage of improving converter availability because the center capacitor, an often relatively unreliable component, is no longer a single point of failure.

D. Feasible and Unfeasible Topologies

Based on the analysis, it is possible to identify feasible and unfeasible topologies in [20] that can be expanded into MICs. Among the basic converter topologies—buck, boost, buck–boost, SEPIC, and Ćuk—only the buck and the buck–boost topologies are feasible because they are the only ones that use the only acceptable input cell in Fig. 2. As exemplified in Fig. 4(a), boost, SEPIC, and Ćuk converters cannot be expanded into multiple-input configurations because their input cell violates rule 2, and because the center capacitor in both SEPIC and Ćuk converters violates rule 3. One alternative for both SEPIC and Ćuk converters is to relax the assumption of maximizing the number of common components and place the center capacitor in each of the input cells. In this way, the input cell corresponds to the one shown in Fig. 5(a). The resulting multiple-input SEPIC and Ćuk converters are shown in Figs. 6 and 7, respectively. Both of these topologies have a current-source interface that makes them suitable for any source technology, including those requiring a smooth current profile (e.g., fuel cells), without the need for an additional input filter (see Fig. 3).

From all the configurations suggested in [20], the following are unfeasible: A2 (boost converter), B1, B2, C1, C2, C5 (Ćuk converter), D1–D5, E1, E2, E4, E6, F2, F3, F4, G1(2), G2, G3, G4, G5 (SEPIC converter), H1–H4, I1–I4, I6, J1–J5, K1, K2, K5, L1, L2, M1, M2, and N1–N6. Rule 2 violation is the most common cause of unfeasibility, especially if the single-input converter has four switches.
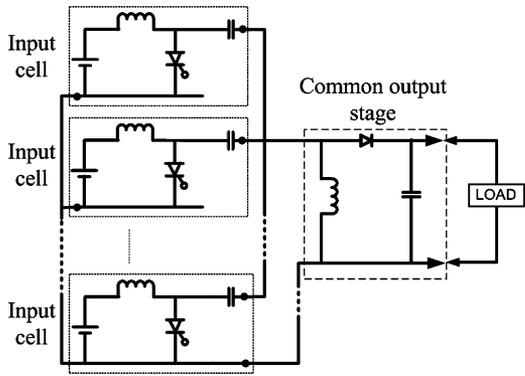
Fig. 6. Multiple-input SEPIC converter.

Fig. 7. Multiple-input Ćuk converter.

Fig. 8. MIC based on configuration D1 in [20].
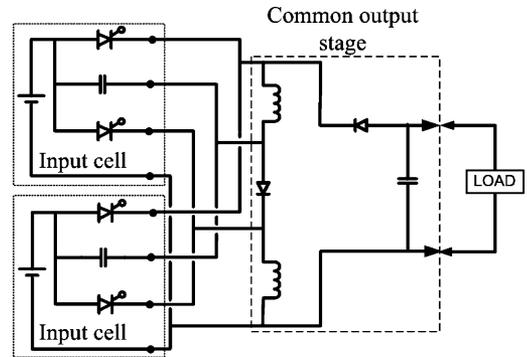
Fig. 9. MIC based on configuration I4(1) in [20].
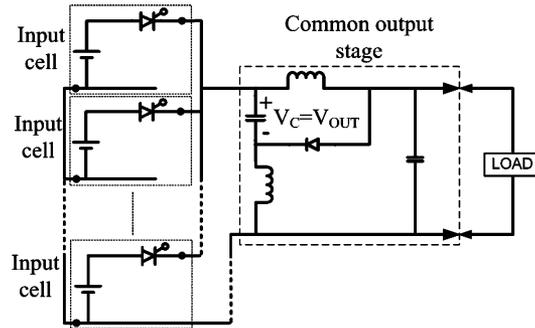
Fig. 10. MIC based on configuration G1(1) in [20].

The feasible configurations in [20] are A1 (buck converter), A5 (buck–boost converter), B5, D6, E3, E5, F1, F5, F6, G1(1), G6, H5, H6, I5, J6, L5, and M5. Some of these feasible configurations are cascades of two simpler topologies, or are feasible topologies with the addition of the current-source conditioning filter in Fig. 3. The cascaded topologies are B5 (buck and boost converters, also suggested in [13]), H5 (buck and buck–boost), H6 (buck–boost and boost), I5 (buck and buck), J6 (buck–boost and buck), L5 (buck–boost and buck–boost), and M5 (buck and boost with additional intermediate filtering). The topologies with the addition of a current-source conditioning filter to a fundamental converter are D6 (buck) and F5 (buck–boost). Other configurations, such as E5 (buck) and F6 (buck–boost), are basic topologies with additional filtering at the output. Finally, configurations E3 and F1 can be reduced to a buck–boost and a buck converter, respectively, because these topologies include redundant branches with inductors and capacitors. Thus, in [20], only configurations A1 (buck), A5 (buck–boost), G1(1), and G6 are fundamental topologies suitable to be expanded into MICs.

The configurations in [20] that can be expanded into MICs if the assumption of minimizing the total number of components is relaxed and the center capacitor is distributed from the common stage into each of the input cells are C1, C5 (Ćuk converter), D1, D2, D4, E2, E4, F3, G3(1), G5 (SEPIC converter), H3(1), I2(1), I3 (1), and I4(1). Figs. 8 and 9 show two examples of these topologies: the MIC derived from D1 using the input cell

in Fig. 5(c) and the MIC derived from I4(1) using the input cell in Fig. 5(d).

The analysis suggests several MIC topologies. Some of them, such as A5 (buck–boost) and B5 (cascade of buck and boost converters), have been previously suggested in the literature [13], [14]. Two MIC topologies not previously suggested and that still achieve total number of component minimization while complying with the rules in Section II-B are obtained from configurations G1(1) and G6 in [20]. Their respective multiple-input versions are shown in Figs. 10 and 11. One advantage of the topology obtained from G1(1) is the high input-to-output voltage conversion ratio at duty cycles close to 0.5. In many cases, such as the multiple-input SEPIC or the MIC derived from G6 in [20], isolated versions of the multiple-input topologies can be obtained by replacing the inductor in the common stage with two coupled inductors.

The analysis was verified by using simulations. Figs. 12–17 depict the simulation results for some of the topologies discussed
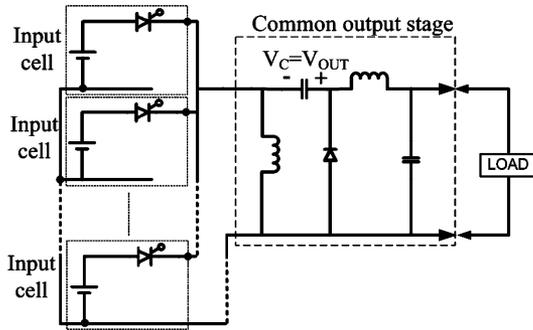
Fig. 11.   MIC based on configuration G6 in [20].
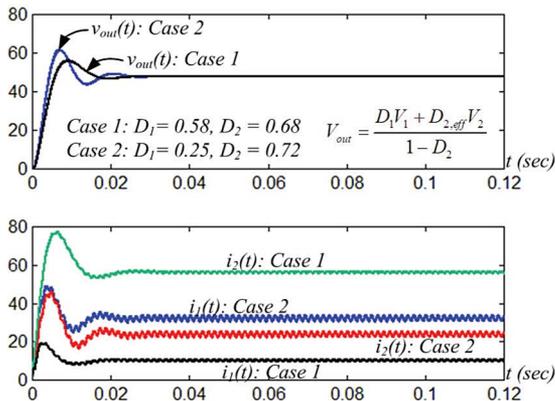
Fig. 12.   Simulation results for a multiple-input SEPIC converter.
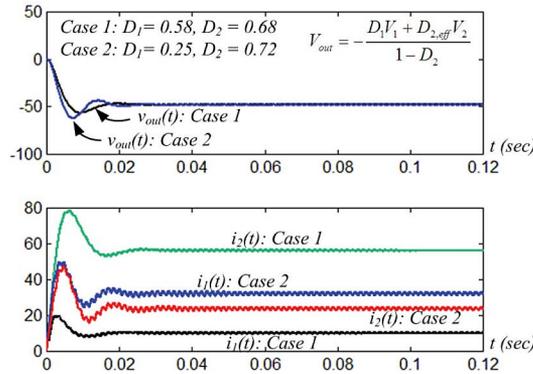
Fig. 13.   Simulation results for a multiple-input Ćuk converter.
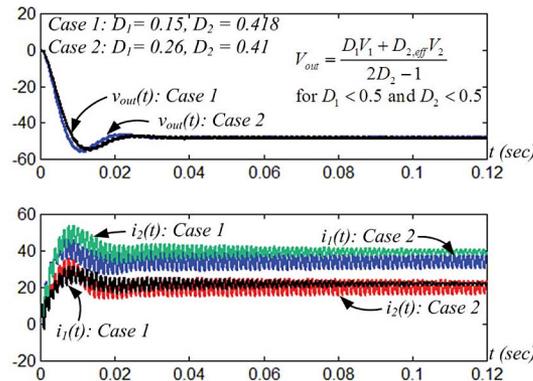
Fig. 14.   Simulation results for an MIC derived from configuration G1(1) in [20].
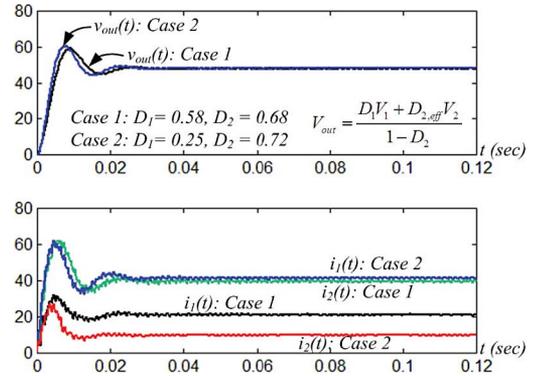
Fig. 15.   Simulation results for an MIC derived from configuration G6 in [20].
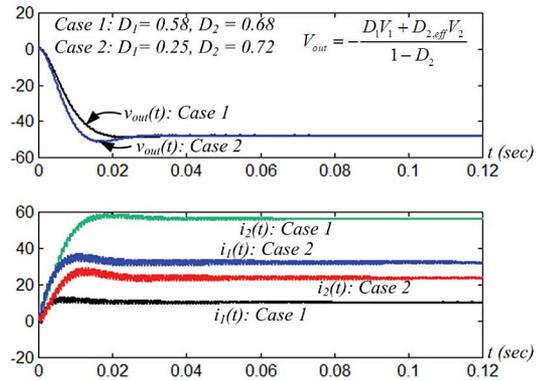
Fig. 16.   Simulation results for an MIC derived from configuration D1 in [20].
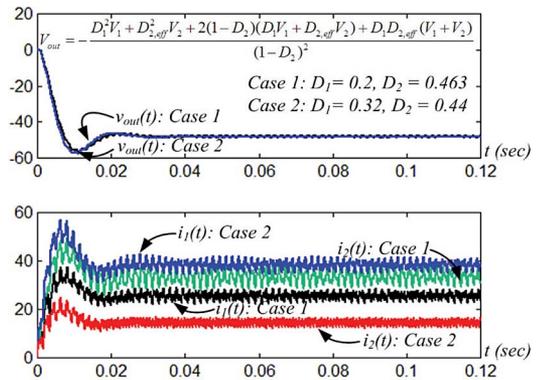
Fig. 17.   Simulation results for an MIC derived from configuration I4(1) in [20].

in this letter. These figures also include the input-to-output voltage relationship that is verified with the simulations. Without loss of generality, only two input cells with input voltages V_1 and V_2 are considered, although a general input-to-output voltage relationship for the SEPIC, Ćuk, and G1(1) MICs can be found in [22]. D_1 and D_2 represent the commanded duty cycles in input legs 1 and 2, respectively, whereas $D_{2,\text{eff}}$ is the portion of the switching period during which the FCBB in leg 2 conducts current. Since it is assumed that $V_2 < V_1$, then $D_2 > D_1$, and $D_{2,\text{eff}} = D_2 - D_1$. To confirm that each input leg can be controlled independently, Figs. 12–17 show that the same output voltage can be achieved with different input currents in each

leg. For all MICs in Figs. 12–17, V_1 is 24 V, $V_2 = 16$ V, the output capacitance is 1500 μF, the switching frequency is 20 kHz, the output voltage is approximately 48 V, and the load is a 2-Ω resistor. For MICs derived from G1(1), I4(1), and G6 in [20], an input filter, like the one shown in Fig. 3, with $L = 500$ μH and $C = 100$ μF, was used. All other inductances in these three MICs equal 300 μH. For the SEPIC, the Ćuk, and the D1 MICs, the input cell capacitances equal 25 μF and all inductances are 800 μH. All other capacitances for G6 and I4(1) MICs are 100 μF.

III. CONCLUSION

This letter discussed the generation of MICs from their respective single-input versions. Based on several assumptions, restrictions, and conditions, the analysis indicates some feasible and unfeasible cells for multiple-input development. The study uses four rules to identify single-input topologies that can be extended into multiple-input circuits. Using an extensive list of single-input dc–dc converters configurations suggested in [20], this letter identified feasible and unfeasible MICs topologies. Finally, six new MIC topologies were introduced through their circuit schematic, including the multiport versions of two classical dc–dc converters: the SEPIC and the Ćuk converters. The behavior of these six MICs is verified with simulations. Future research will study in more detail these six and other MIC topologies suggested in this letter, with and without allowing bidirectional power flow in at least one input leg.

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