Analysis of the Effects of Duty Cycle Constraints in Multiple-Input Converters for Photovoltaic Applications

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Abstract — A multiple-input converter for photovoltaic-powered communication sites is analyzed. The study shows that the duty cycles of a multiple-input converter, which control the power delivered by each source, may have practical limitations when each photovoltaic module attempts to achieve its own maximum power point at the same time. This paper discusses an alternative circuit that has two coupled inductors in a common output stage, which may enable the multiple-input converter to overcome the limited duty cycles. The relationship between the duty cycles and the power supplied by each input is derived mathematically in order to theoretically analyze the effects given by the limitations. Power budgeting with respect to each source is also demonstrated with simulations.

I. Introduction

Photovoltaic (PV) modules are a commonly suggested solution to power telecommunication systems, especially in isolated locations [1]. One advantage of PV modules is increased system availability by providing a diverse power supply. Hence, PV modules may contribute to meeting one of the most important requirements in telecom power systems. However, PV systems have a relatively high cost which impacts their widespread application.

One alternative in order to reduce the financial impact of PV systems cost is to have a modular and scalable design. In this approach, it is not necessary to initially install all the PV modules required to meet the expected load for a site's life, but PV modules could be added as the load grows. Although this goal seems to be trivial as more PV modules are added, practical issues make adding PV modules non-trivial. The main issue is that any given PV module usually stays on the market for only a few years before being discontinued. Thus, it is likely that a different model of solar panels will need to be chosen if a plant's solar generation capacity is to be increased. Moreover, even if the goal is not to increase the plant capacity, the short commercialized life of PV modules affect maintenance and repair planning as most PV manufacturers reserve the right to replace discontinued PV modules with different models of that originally purchased [2], [3].

If the system is designed with a centralized architecture with a single converter for the entire PV array with different PV module models, then the overall performance of the system is that of the PV module model with the worst characteristics. One alternative is to have individual converters for each group of PV modules of the same model. In this way, the varying maximum power point (MPP) of the different PV module models could be tracked and overall performance would not be affected. However, this tends to be a cost ineffective solution.

Another approach to integrate several different PV modules is to use multiple-input converters (MICs) [1]. This method has the advantage of being more cost effective than having separate converter modules for each solar panel, without affecting planning flexibility. However, MICs have limitations on the duty cycles [4]-[6]; with forward-conducting-bidirectional-blocking (FCBB) switches, the duty cycle of each leg is affected by the duty cycles of all other legs with a higher input voltage [7]. Hence, the power budgeting of MICs should be considered carefully in order to achieve MPP for each PV module. Past research on power budgeting was performed on MICs which did not have duty cycle limitations [1] or which had other inputs other than PV modules [8]-[10]. To determine the effects of duty cycle limitations in MICs for PV applications, this paper analyzes a MIC that only has PV modules as power sources. Analysis is conducted with the derivation of equations in order to verify the effects of duty cycle constraints when each module attempts to reach its MPP. MATLAB simulations examine the theoretical analysis and show the effects given by these limitations. The feasibility of MPP tracking with the limited duty cycles is also explored using a proposed circuit which has two coupled inductors in the output stage.

The paper is organized as follows. Section II analyzes the limitations of a multiple-input single ended primary inductor converter (SEPIC) that can both step-up and step-down the input voltage. Section III discusses an alternative circuit to overcome the limited duty cycles and finally, in Section IV, the simulation results and conclusions of the study are discussed.

II. Analysis of a Multiple-Input Converter

As shown in Fig. 1, the analysis is conducted with a multiple-input SEPIC because its buck and boost characteristic allows tracking the entire voltage-current (V-I) or voltage-power (V-P) curve of a PV module.

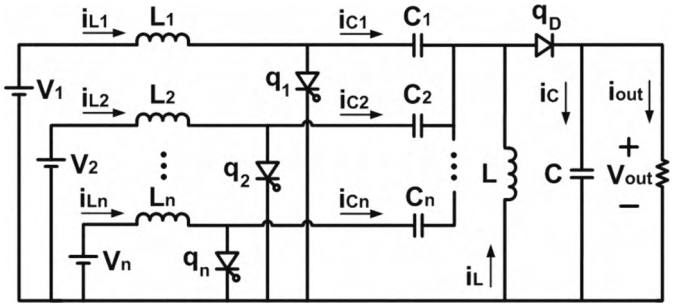

Fig. 1. A multiple-input SEPIC

Assuming ideal components and a continuous conduction mode of operation, the relationship between the input and output can be represented from [8], [11] as

$$V_{out} = \frac{\sum D_{(i)eff} V_{(i)}}{1 - \sum D_{(i)eff}} \tag{1}$$

where $D_{(i)eff}$ is each input's effective duty cycle, i.e., its own duty cycle less than that of the input leg with the next immediate higher input voltage. An example of the characteristics of the switching functions and the existence of an effective duty cycle $D_{(i)eff}$ is shown in Fig. 2 for a two-input converter with FCBB switches. In this figure, q_1 and q_2 represent the control signals of the FCBB switches.

In this study, a two-input SEPIC was considered for the analysis. The dynamic equations resulting from applying Kirchhoff's current law at one node of each capacitor in Fig. 1 are

$$\begin{cases} C_1 \frac{dv_{c1}}{dt} = i_{L1}(1 - q_{1eff}) - q_{1eff}(i_{L2} + i_L) \\ C_2 \frac{dv_{c2}}{dt} = i_{L2}(1 - q_{2eff}) - q_{2eff}(i_{L1} + i_L) \\ C \frac{dv_c}{dt} = \frac{-V_c}{R} + q_D(i_{L1} + i_{L2} + i_L) \end{cases} \tag{2}$$

To simplify the study, it was assumed that all components are ideal and the converter is operating in continuous conduction mode. In addition, it was also assumed that V_1 is higher than V_2 and hence $D_{(i)eff}$ is defined as shown in Fig. 2.

Since average steady-state current through any capacitor is zero, the currents of the averaged model of (2) results in

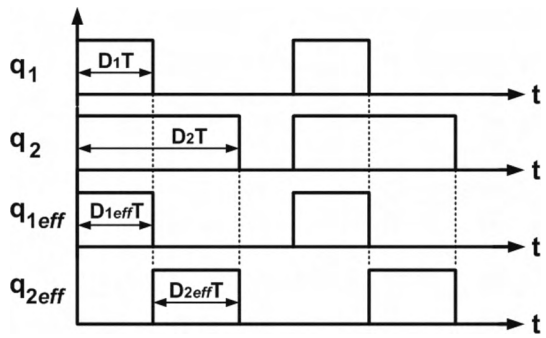

Fig. 2. An example operation of $D_{(i)eff}$
(It is assumed that $V_1 > V_2$)

$$\begin{cases} I_{L1}(1 - D_{1eff}) - D_{1eff}(I_{L2} + I_L) = 0 \\ I_{L2}(1 - D_{2eff}) - D_{2eff}(I_{L1} + I_L) = 0 \\ \frac{-V_c}{R} + D_D(I_{L1} + I_{L2} + I_L) = 0 \end{cases} \tag{3}$$

With the assumption $V_1 > V_2$, the effective duty cycles in (3) can be substituted by

$$\begin{cases} D_{1eff} = D_1 \\ D_{2eff} = D_2 - D_1 \\ D_D = 1 - D_{2eff} - D_{1eff} = 1 - D_2 \end{cases} \tag{4}$$

When (4) is substituted in (3), it yields

$$\begin{cases} I_{L1}(1 - D_1) - D_1(I_{L2} + I_L) = 0 \\ I_{L2}(1 - (D_2 - D_1)) - (D_2 - D_1)(I_{L1} + I_L) = 0 \\ \frac{-V_c}{R} + (1 - D_2)(I_{L1} + I_{L2} + I_L) = 0 \end{cases} \tag{5}$$

The first two equations of (5) can be combined into

$$(I_{L1} + I_{L2})(1 - D_2) = I_L D_2 \tag{6}$$

When the third equation of (5) is compared with (6), a relationship of I_L and I_{out} can be verified as follows.

$$I_L = \frac{V_c}{R} = I_{out} \tag{7}$$

As shown below, (6) and (7) can be used to represent I_{out} with the currents from each input.

$$I_{out} = \frac{(I_{L1} + I_{L2})(1 - D_2)}{D_2} \tag{8}$$

When V_{out} is multiplied to both sides of (8), the output power can be derived as

$$P_{out} = I_{out} V_{out} = \frac{(I_{L1} + I_{L2})(1 - D_2)}{D_2} V_{out} \tag{9}$$

To analyze the relationship between the output power and the duty cycles of each input, (1) uses the definitions shown in (4) to derive V_{out} in the double-input case as

$$\begin{aligned} V_{out} &= \frac{D_{1eff} V_1 + D_{2eff} V_2}{1 - (D_{1eff} + D_{2eff})} \\ &= \frac{D_1 V_1 + (D_2 - D_1) V_2}{1 - D_2} \end{aligned} \tag{10}$$

The output power P_{out} can be represented with the input voltages and currents when (10) substitutes V_{out} in (9).

$$P_{out} = \frac{(I_{L1} + I_{L2})(D_1 V_1 + (D_2 - D_1) V_2)}{D_2} \tag{11}$$

With the definitions of the input and output power,

$$\begin{cases} P_1 = I_{L1}V_1 \\ P_2 = I_{L2}V_2 \\ P_{out} = \frac{{V_{out}}^2}{R} = P_1 + P_2 \end{cases} \quad (12)$$

the power supplied by each input can be derived as

$$P_1 = \frac{D_1\left(\frac{{V_{out}}^2}{R} - \frac{V_1 V_{out} D_2}{R(1-D_2)}\right)}{(D_2 - D_1)\left(\frac{V_2}{V_1} - 1\right)} \quad (13)$$

$$P_2 = P_{out} - P_1 \quad (14)$$

Equation (13) and (14) indicate that the power supplied by each input is not only affected by its own duty cycle, but also by those of the other inputs. Fig. 3, computer representations conducted with MATLAB, supports the previous theoretical analysis; as shown, the values of P_1 and P_2 vary with the values of both D_1 and D_2. For instance, in order to attain 200 watts for P_1 and 160 watts for P_2, the values of D_1 and D_2 can be set as 0.30 and 0.73 respectively.

Moreover, (13) and (14) establish the fact that the MPP cannot be tracked if the required effective duty cycles in both input legs are more than 0.5. For example, when both inputs need 0.6 of effective duty cycle to achieve MPP, required D_2 becomes 1.2 – according to (4) – which is an impossible value. This example depicts the theoretical limitation that seems to occur when both inputs of a two-input converter may seem to demand a sum of effective duty cycles over 1.0. When the simulation is extended to a three-input case, the maximum effective duty cycle of each input leg should be limited below 0.33 in order to avoid limitations, or even less if one of three inputs requires an effective duty cycle above this value.

Since the control of the power supplied by each input leg is affected by the duty cycles of the other input legs, the equivalent resistance seen by each source is also affected by other inputs. As indicated in (12) and represented in Fig. 4, the total output power is the sum of the power provided by each input. To calculate the equivalent resistance seen from each source, the circuit in Fig. 4 can be divided into two circuits which are shown in Fig. 5. Equation (15) and (16) show the calculated equivalent resistance in terms of duty cycles in both inputs.

$$R_{eq1} = \frac{(1-D_2)V_1 R}{D_1 V_{out}} \quad (15)$$

$$R_{eq2} = \frac{(1-D_2)V_2 R}{(D_2 - D_1)V_{out}} \quad (16)$$

In order to achieve the MPP, the equivalent resistance should be designed to meet the point where the PV module produces maximum power. Fig. 6 shows an example of the equivalent resistance that implies maximum power, i.e., at the current (4.9 A) and voltage (26 V), the output power (127.4 W) becomes the greatest. In this example, the equivalent resistance is 5.31 ohms. It is also possible to find different matching resistances for different PV modules connected at different inputs to attain maximum power with a MIC. This point is introduced and discussed in the following section.

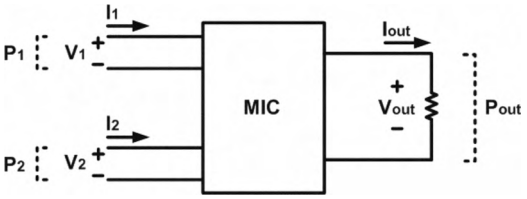

Fig. 4. Simplified schematic of two-input SEPIC

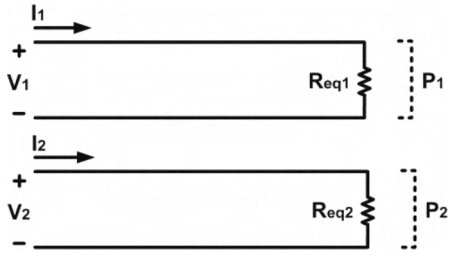

Fig. 5. Equivalent resistance seen by each source

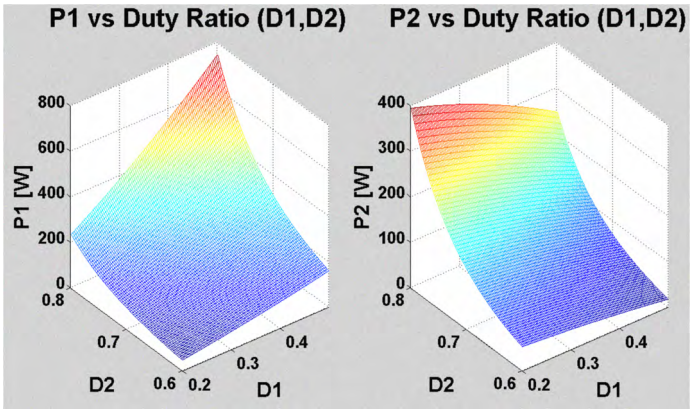

Fig. 3. Simulation results showing P_1 and P_2 as the functions of D_1 and D_2 (It is assumed that V_1 = 30.3 V, V_2 = 16.8 V, and R = 10 Ω)

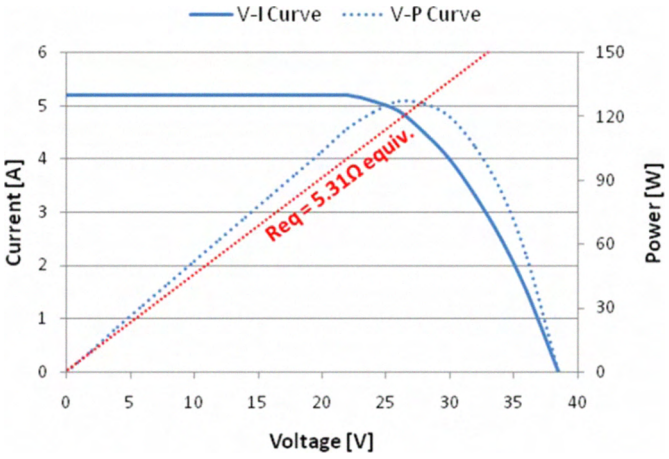

Fig. 6. An example V-I and V-P curve of a PV module

III. Discussion of a Design Alternative

If all inputs of a MIC in Fig. 1 achieve MPP for a given load resistance, the output voltage will be univocally determined by the sum of all input powers at each respective MPP. All input currents and voltages will be fixed because they only depend on each PV module physical characteristics and operating conditions. Hence, both I_{L1} and I_{L2} are fixed, and equal

$$I_{L1} = \frac{D_1}{(1-D_2)}\frac{V_{out}}{R} \tag{17}$$

$$I_{L2} = \frac{D_{2eff}}{(1-D_2)}\frac{V_{out}}{R} \tag{18}$$

Hence, D_1 and D_2 can be obtained by solving the system of algebraic linear equations given by (10) and (17) or (18). As a result,

$$D_1 = \frac{I_{L1}}{I_{L1}+I_{L2}+I_{out}} \tag{19}$$

$$D_2 = \frac{I_{L1}+I_{L2}}{I_{L1}+I_{L2}+I_{out}} \tag{20}$$

Since I_{out} will tend to be zero as R approximate infinity, D_2 will approximate 1 for very large values of R. Thus, in theory, it would always be possible to achieve the desired duty cycles to reach MPP in all inputs. In practice, however, the duty cycle D_2 could be higher than the maximum recommended duty cycle which is about 0.85 for converters for current source interface as a SEPIC or boost, as high duty cycles could lead to control sensitivity and stability issues. Therefore, although theoretically it would always be possible to achieve the required duty cycles to reach MPP in all inputs, in practice, there is a limitation.

One simple alternative circuit to overcome duty cycle limitations in multiple-input SEPICs is shown in Fig. 7. The proposed MIC uses two coupled inductors to isolate the input and output stages. This solution may achieve the required output level as a sum of the maximum power from each source without exceeding the limited duty cycle in any of the input legs.

As same as the analysis conducted in Section II, a two-input SEPIC was considered for the analysis of the proposed circuit. With the coupled inductors, the output voltage $V_{out,n}$ becomes

$$V_{out,n} = \frac{N_2}{N_1}\left(\frac{D_{1,n}V_1 + D_{2eff,n}V_2}{1-D_{2,n}}\right) \tag{21}$$

Since the equivalent resistances and input powers of both non-isolated and isolated multiple-input SEPIC are the same when the MPP is achieved, the output powers are the same as well. Moreover, the output voltages – (10) and (21) – become equal when the same load resistance is used for both cases. Hence,

$$\frac{D_1V_1 + D_{2eff}V_2}{1-D_2} = \frac{N_2}{N_1}\left(\frac{D_{1,n}V_1 + D_{2eff,n}V_2}{1-D_{2,n}}\right) \tag{22}$$

Equation (23) also stands since the input current of both cases are equal when the equivalent resistances are the same. For instance, the input current for leg #1 and #2 in both cases are

$$\frac{D_1}{1-D_2} = \frac{N_2}{N_1}\left(\frac{D_{1,n}}{1-D_{2,n}}\right) \tag{23}$$

$$\frac{D_{2eff}}{1-D_2} = \frac{N_2}{N_1}\left(\frac{D_{2eff,n}}{1-D_{2,n}}\right) \tag{24}$$

When (23) and (24) are used to solve for the duty cycles, $D_{1,n}$ and $D_{2,n}$ for the isolated MIC in Fig. 7 are equal to

$$D_{1,n} = \frac{nD_1}{1+(n-1)D_2} \tag{25}$$

$$D_{2,n} = \frac{nD_2}{1+(n-1)D_2} \tag{26}$$

where n is N_1/N_2. As shown in (25) and (26), the proposed MIC gives another factor – the ratio of N_1 to N_2 – to the value of duty cycles. This is an advantage because the level of equivalent resistance can be controlled by not only the duty cycles of each input, but also by the ratio given by the number of turns in the windings of two coupled inductors; i.e., by controlling the turns ratio, the new duty cycles may be smaller providing a solution to overcome control limitations.

A numerical example is used in the following to demonstrate the validity of the theoretical analysis. This example is summarized in Table I. When two different PV modules are connected to a MIC, the required equivalent resistances to achieve MPP are different for each input [12], [13]. For the MIC that has no coupled inductors, the required duty cycles to reach MPP can be calculated using (19) and (20). On the other hand, the required duty cycles of MIC with coupled inductors can be determined by applying (25) and (26). For the calculation, it was assumed that $N_1:N_2$ equals 1:2 or 1:3, V_1 = 41 V, V_2 = 17.1 V, and R = 120 Ω. The duty cycles of both MICs were set to meet the equivalent resistance to achieve MPP for each connected PV module. As shown in Table I, D_2 in the case without coupled inductors is too large

TABLE I
Comparison in Duty Cycles between Two MICs

Input Number	Model	Maximum Power	V_{MPP}	I_{MPP}	$R_{eq,MPP}$	R_{LOAD}	D_1:D_2 without coupled inductors	D_1:D_2 with coupled inductors ($N_1:N_2$ = 1:2)	D_1:D_2 with coupled inductors ($N_1:N_2$ = 1:3)
1	SPR-220-BLK [12]	220 W	41 V	5.37 A	7.64 Ω	120 Ω	0.46:0.86	0.40:0.76	0.36:0.68
2	NE-80EJE [13]	80 W	17.1 V	4.67 A	3.66 Ω				

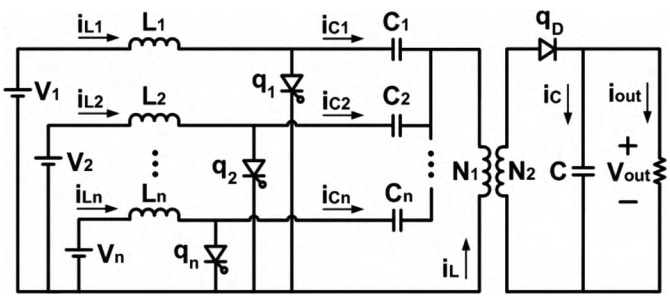

Fig. 7. Proposed multiple-input SEPIC

for practical purposes. However, the duty cycles of a MIC become smaller when coupled inductors are placed in common output stage. This result can be extended to other cases which have duty cycle constraints and the possibility of dividing an inductor into coupled inductors. By changing the turns ratio, MICs may have smaller duty cycles corresponding to the MPP and hence can provide a solution for the practical duty cycle limitations.

IV. Conclusion

A study of duty cycle constraints in MICs for PV applications was presented. The analysis used a multiple-input SEPIC to show that the limited duty cycles in many MIC topologies may practically prevent MPP tracking in all inputs. This is because the power supplied from each input is not only affected by its own duty cycle but also the duty cycles of all other inputs. The results of mathematical derivation and computer simulation support the theoretical analysis.

This paper also discussed a solution that may overcome the practical duty cycle limitations of MICs by replacing the inductor in the common output stage with two coupled inductors which enable the MIC to have one more design factor to facilitate reaching the equivalent resistance seen by each source. The coupled inductors also provide the flexibility of choosing the smaller values for duty cycles to achieve MPP, which may be a way to avoid exceeding practical duty cycle limits.

An example was used to demonstrate the theoretical analysis. The calculation results showed that the proposed MIC may achieve MPP with smaller values of duty cycles, which can be an answer to the practical limitations driven by input legs' duty cycle interdependencies. This example shows that the proposed MIC is suitable for use as a high-performance DC-DC converter for various kinds of PV modules that require different maximum power operating points in various conditions.

References

[1] B. Le and A. Kwasinski, "Analysis of a flexible and rugged photovoltaic-based power system," in *Rec. INTELEC 2008,* pp. 1-7.

[2] http://solartechpower.com/web1/doc/warranty.pdf [Jul. 1, 2009].

[3] http://www.wholesalesolar.com/pdf.folder/module%20pdf%20folder/KDWarranty.pdf [Jul. 1, 2009].

[4] A. Kwasinski and P.T. Krein, "Multiple-input dc-dc converters to enhance local availability in grids using distributed generation resources," in *Proc. APEC 2007*, pp.1657-1663.

[5] A. Kwasinski and P.T. Krein, "Stabilization of constant power loads in Dc-Dc converters using passivity-based control," in *Rec. INTELEC 2007,* pp.867-874.

[6] A. Kwasinski, Feasibility multiple-input converters See March issue of the power electronics transactions

[7] A. Kwasinski and P.T. Krein, "A Microgrid-based Telecom Power System using Modular Multiple-Input DC-DC Converters," in *Rec. INTELEC 2005,* pp.515-520.

[8] N.D. Benavides and P.L. Chapman, "Power budgeting of a multiple-input buck-boost converter," *IEEE Transactions on Power Electronics*, vol.20, no.6, pp. 1303-1309, Nov. 2005.

[9] Y.-M. Chen, Y.-C. Liu, F.-Y. Wu, and Y.-E. Wu, , "Multi-input converter with power factor correction and maximum power point tracking features," *Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE* , vol.1, no., pp.490-496 vol.1, 2002.

[10] M. Veerachary, "Multi-input integrated buck-boost converter for photovoltaic applications," *Sustainable Energy Technologies, 2008. ICSET 2008. IEEE International Conference on* , vol., no., pp.546-551, 24-27 Nov. 2008.

[11] S.H. Choung and A. Kwasinski, "Multiple-input DC-DC converter topologies comparison," *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE* , vol., no., pp.2359-2364, 10-13 Nov. 2008.

[12] http://www.sunstoresolar.com/documents/Sunpower220PVData.pdf [Jul. 1, 2009].

[13] http://www.gogreensolar.info/specs/sharp.80w.pdf [Jul. 1, 2009].