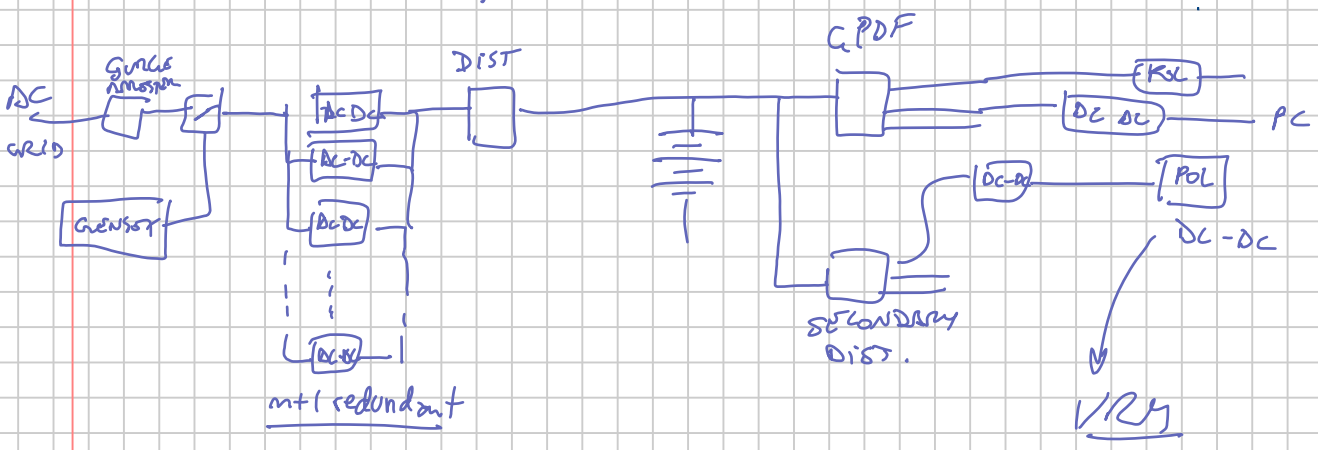
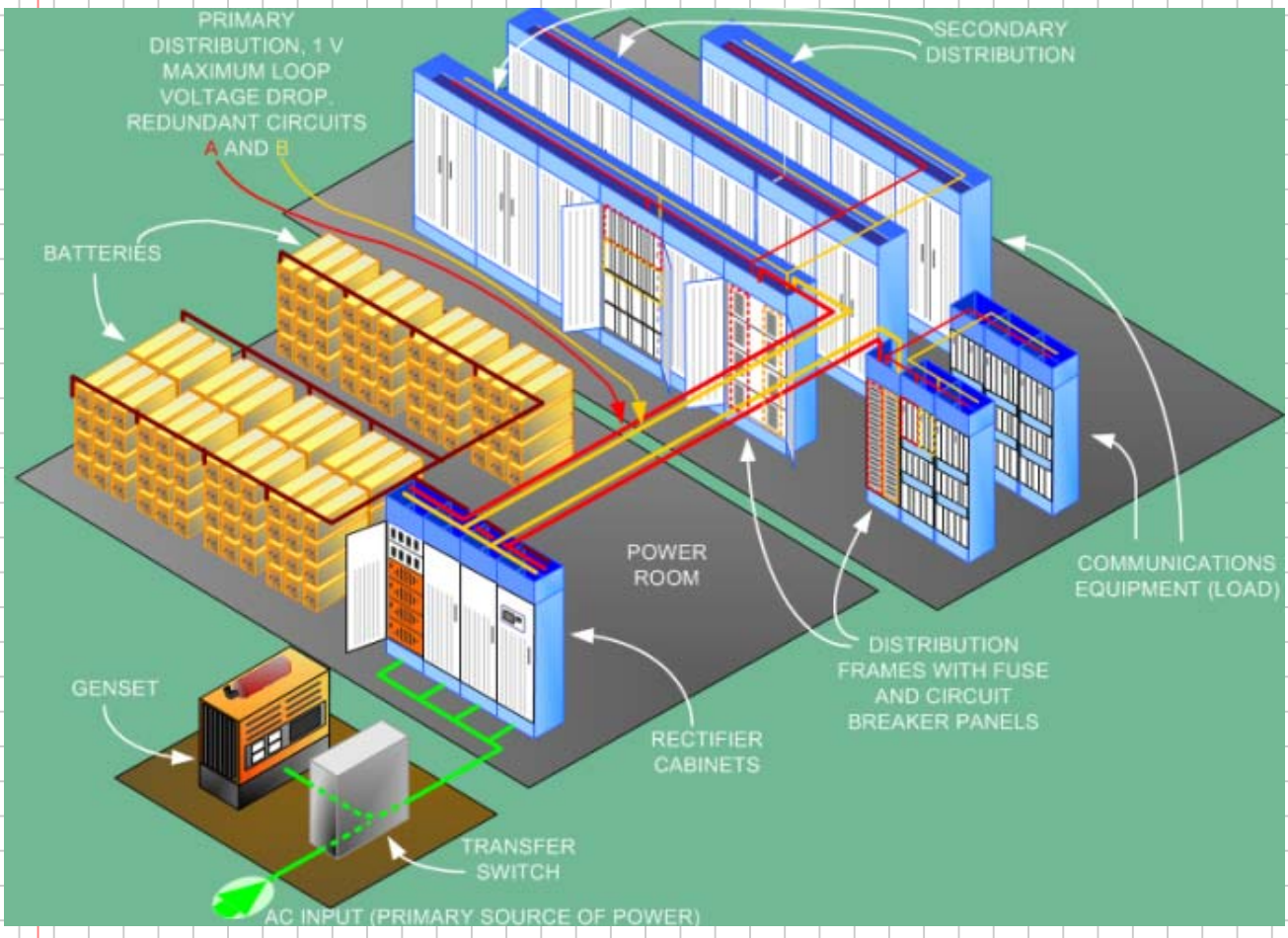
Real components

Note Title 9/12/2007

Real components

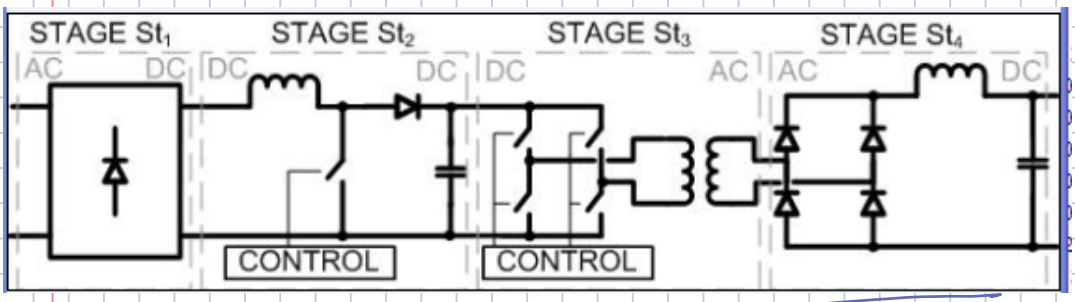
Consider a telecom power systems





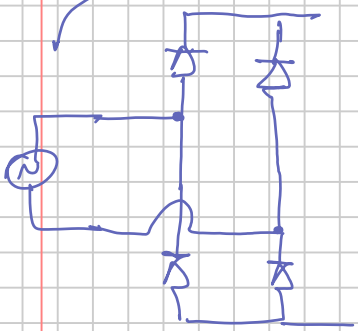
(See ppt)

Rectifier



→ DC-DC boost → PFC

DC-DC Buck → Line condition converter



Distributed architecture

Cascade of converters → Improves efficiency (primary distribution at a higher voltage)

POL regulation → Improve voltage regulation and dynamic response

→ handling of wide load variations

→ less expensive

Other systems with similar architectures

→ Microgrids

→ Most renewable-powered systems

→ hybrid and electric vehicles

Real components → loads

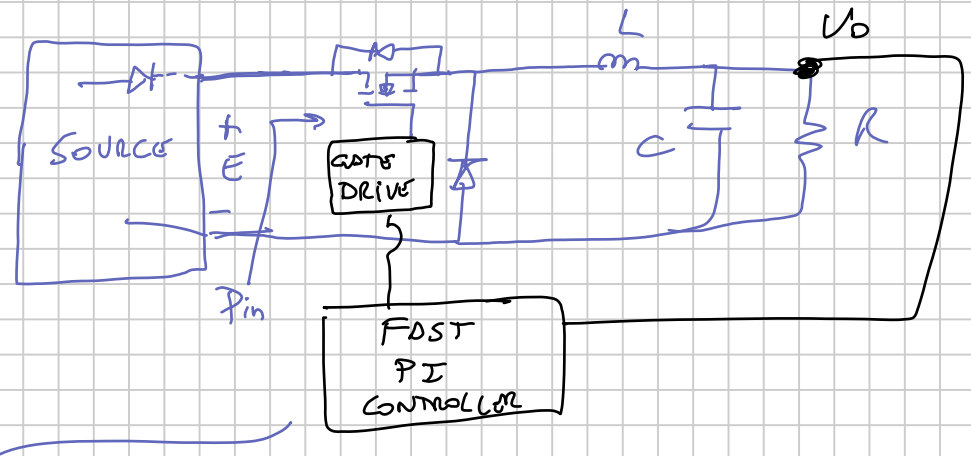
↓

POL ⇒ Constant power load

↳ VRMs

Lets see first constant power loads

Assume a dc-dc buck converter acting as a POL converter



Since the controller is fast, $V_o \simeq$ constant → regardless of changes in the input

If V_o is constant, $\frac{V_o^2}{R} = P_{OUT}$ is constant

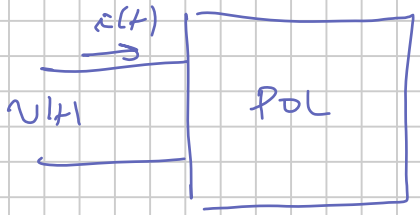
Assuming there is no losses in the buck converter

$$P_{in} = P_{OUT}$$

$$\Downarrow$$

$$P_{in} = \text{constant}$$

Real POL converters:



$$\begin{cases} i(t) = 0 & \text{for } v(t) \le V_{th} \\ i(t) = \dfrac{P_L}{v(t)} & \text{for } v(t) > V_{th} \end{cases}$$

Small signal behavior

$$\delta i(t) = \left.\frac{\partial i}{\partial v}\right|_{V_o} \delta v(t) = -\frac{P_L}{V_o^2}\,\delta v(t)$$

$$\frac{\delta v(t)}{\delta i(t)} = \delta z = -\frac{V_o^2}{P_L} < 0$$

↓ dynamic impedance

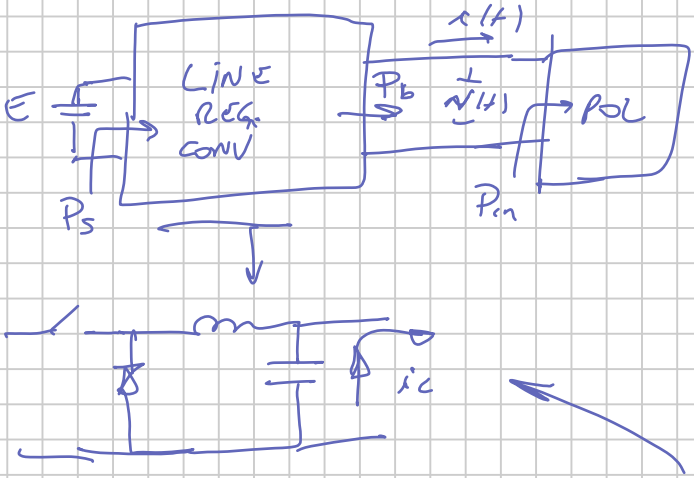
Assume that v drops $\longrightarrow \delta v(t) < 0$

$\downarrow \delta z < 0$

$\delta i(t) > 0 \longrightarrow$ input current increases

$\Downarrow$

destabilizing action



$i_c = C\frac{dv_c}{dt} \longrightarrow dv_c < 0$ (discharging)

As i_c increases the capacitor discharges, so v_c drops more making i_c to increase and the effect is reinforced $\Rightarrow$ voltage collapse

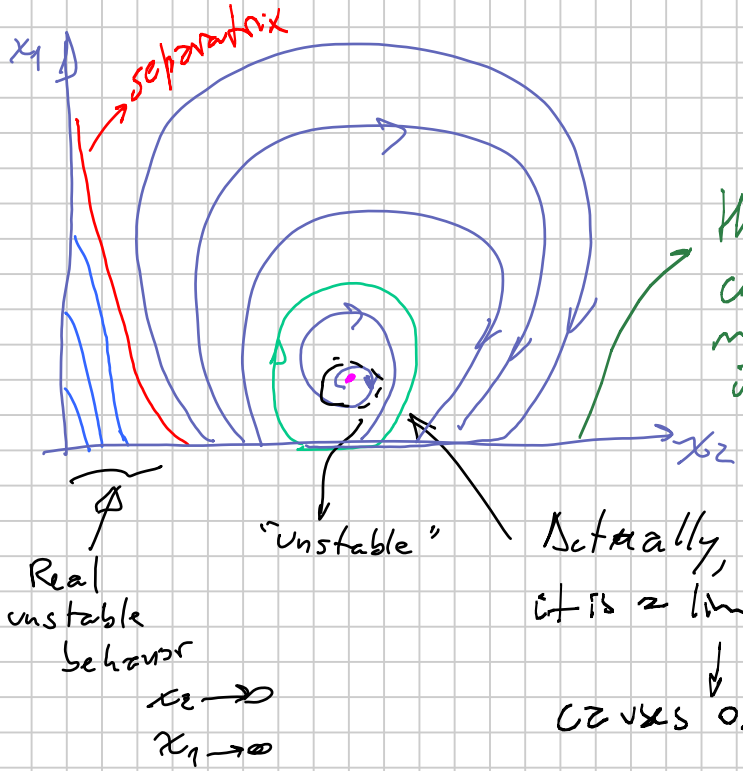
Global behavior → Assuming lossless converters

In reality, since $P_s = P_b = P_{in} = P_L$ (steady state) all extra power acquired during transient cannot be dissipated

↳ Extra power $\Rightarrow$ extra energy

$\Downarrow$

remains oscillating between the line reg. conv. L and C



$d = D = \text{constant}$

Having this constraint that makes $x_1 \geq 0$ is very important in order to determine CPL behavior

Real unstable behavior

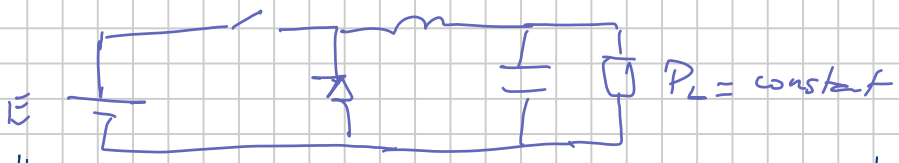
$x_2 \to \infty$

$x_1 \to \infty$

Actually, it is a limit cycle

causes oscillations

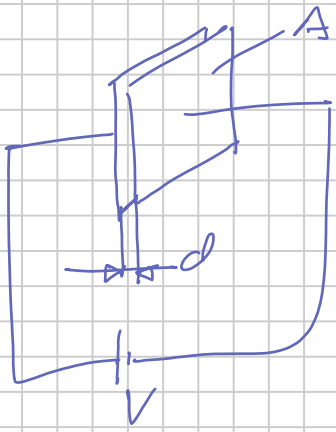
This is in the buck regulating converter but same effect happens with any dc-dc converter



We will be back here when we discuss controls

Real capacitors

Ideal capacitor



$C = \frac{\varepsilon A}{d}$ → only depends on material and geometry

$Q = CV \longrightarrow i = C\frac{dv}{dt}$

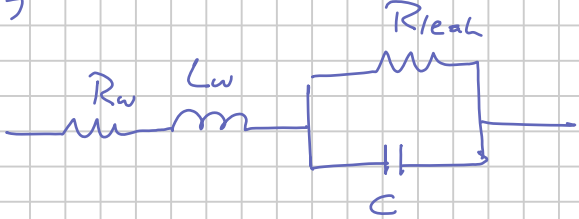
$U = \frac{1}{2}CV^2$

Capacitor types

- ceramic
- tantalum
- Metalic plastic film → polymer "film"
- electrolytic } polarized
- Ultracapacitors

From Lewis's book

Capacitor eq. model



$$Z(\omega) = R_w + j\omega L_w + \frac{1}{\frac{1}{R_{leak}} + j\omega C}$$

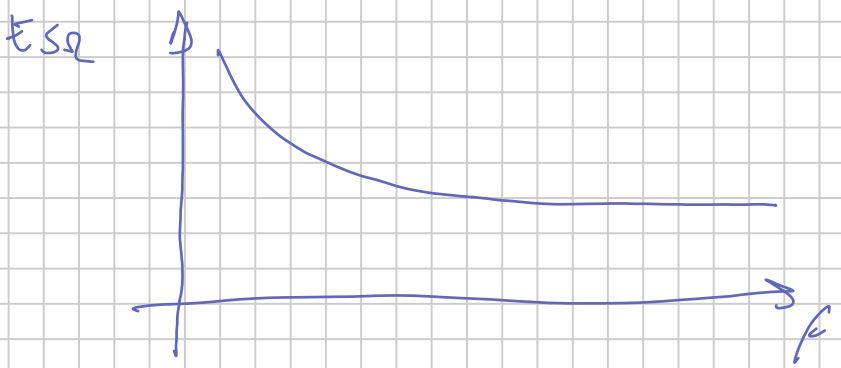
$$Z(\omega) = R_w + j\omega L_w + \frac{R_{leak}}{1 + j\omega C R_{leak}}$$

$$Z(\omega) = R_w + j\omega L_w + \frac{R_{leak} - j\omega C R_{leak}^2}{1 + \omega^2 C^2 R_{leak}^2}$$

↓ Usually $R_{leak} \to M\Omega$, then $\omega^2 C^2 R_{leak}^2 \gg 1$

$$Z(\omega) = R_w + \underbrace{\frac{1}{\omega^2 C^2 R_{leak}}}_{ESR(\omega)} + \frac{1}{j\omega C} + j\omega L_w$$

$ESR(\omega) \longrightarrow$ Function of ω

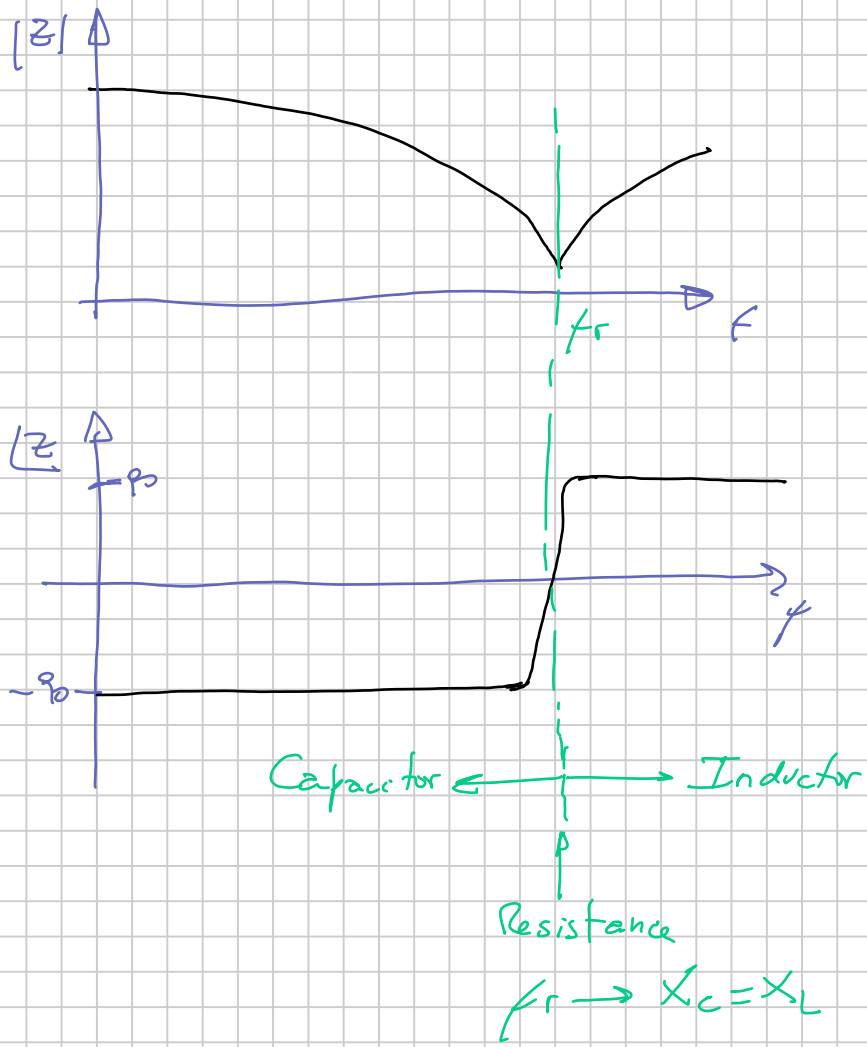


$$\tan\delta = \frac{ESR(\omega)}{X_c(\omega)} \cong \frac{1}{\omega R_{leak} C}$$

If $R_{leak} = \rho \frac{d}{A}$

$$\tan\delta = \frac{1}{\omega \rho \frac{d}{A} \varepsilon \frac{A}{d}} = \frac{1}{\omega \rho \varepsilon} \longrightarrow \text{Independent of geometry}$$

Frequency behavior



fr can be improved (made larger) by using // combinations

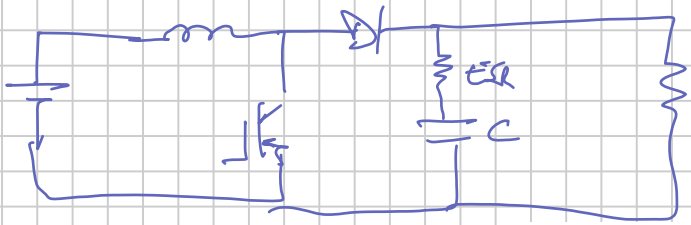
Film → high freq
mica → " "
Ceramic → " "
Electrolytic → low freq, "high" ESR
Tantalum → better than electrolytic
OS-con → A type of electrolytic

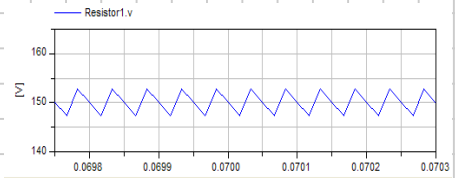
Effect of ESR

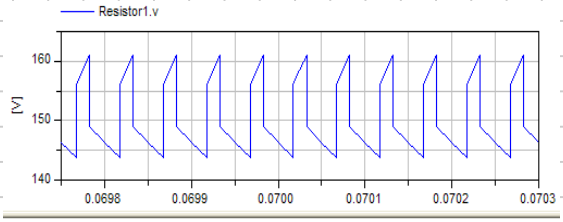
- obvious → losses → heat
  - ↳ A larger capacitor may be needed to provide a larger

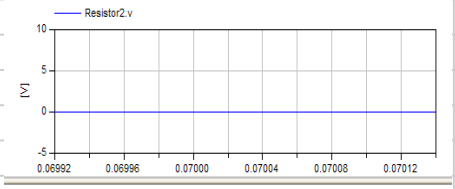
dissipation area.

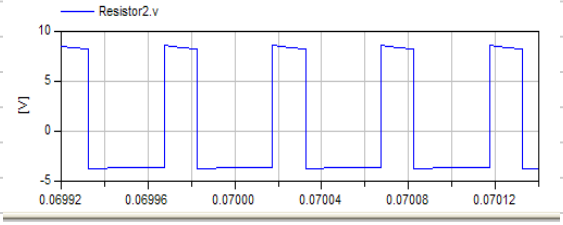
- ESR jump

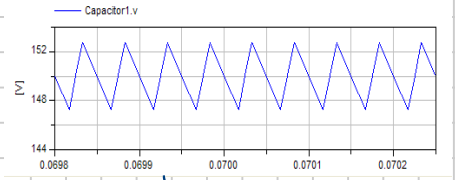


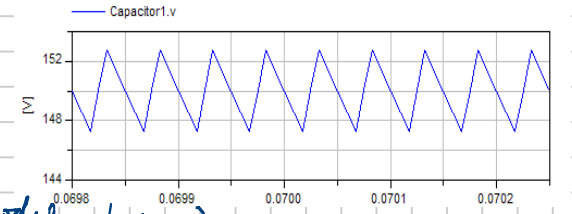




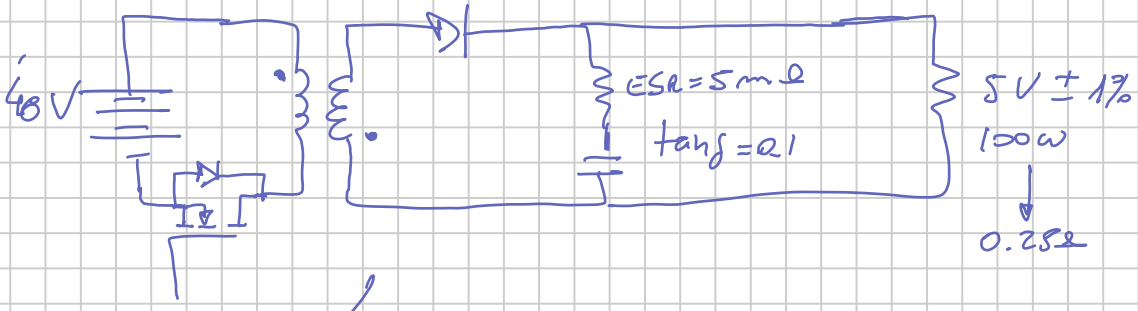






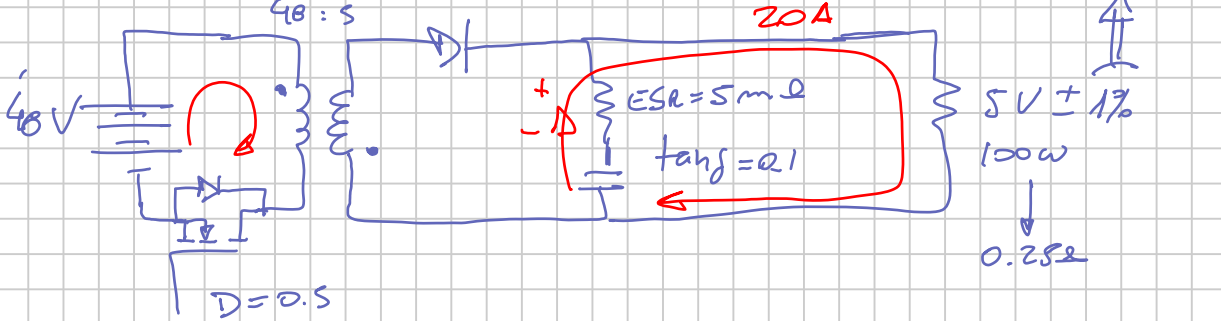


Let's see what happens with real capacitors in voltage regulation modules (VRMs)
↳ A constant power load

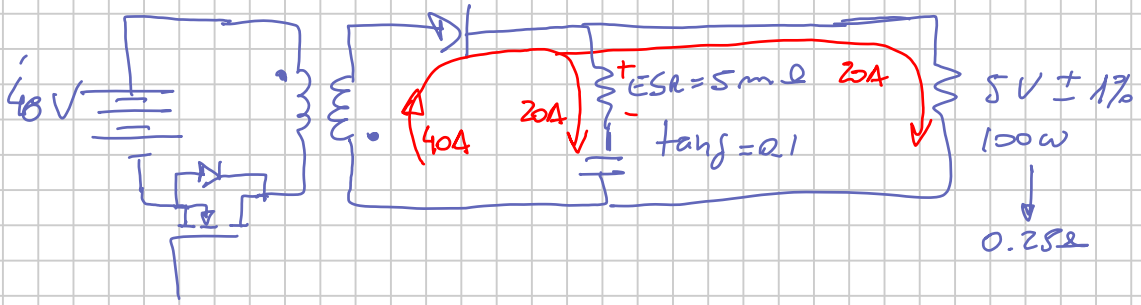


FLY Back

When switch is on

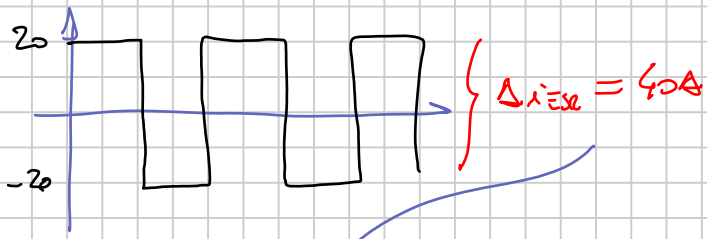


when the switch is off



$$\Delta V_{load} = \Delta V_c + \Delta V_{ESR}$$

$$\Delta V_{ESR} = \Delta i_{ESR} \cdot ESR$$



$$\Delta V_{ESR} = 40 \cdot 0.05 = 0.2$$

Condition can not be met.

VRM → let's see voltage regulation modules and microprocessors as loads.

CPU → Faster clock speeds

→ More transistors → (cmos)

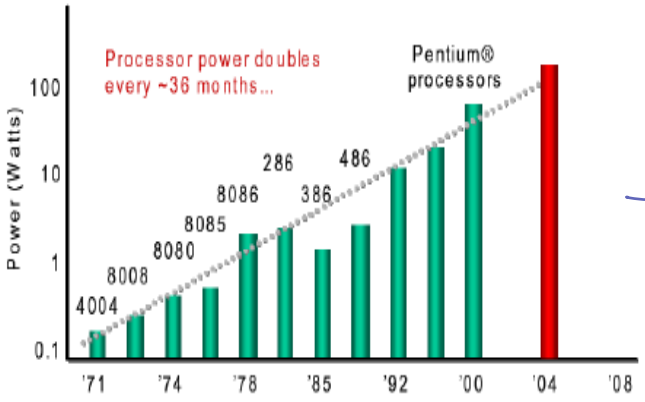
↳ Moore's law → # transistors 2× every 2 years

$P_{cpu} = A_V \, f \, C \, V_{dd}^2$ (coming from $U_{cap} = \frac{1}{2} C V_{dd}^2$)

- f → frequency
- C → capacitance of all gates
- V_{dd} → dc voltage
- A_V → Activity factor → "how many of all gates we are using"
- P_{cpu} → ↳ energy

Power consumption issues → As size reduces, C increases

↳ As the CPU speed increases, f increases

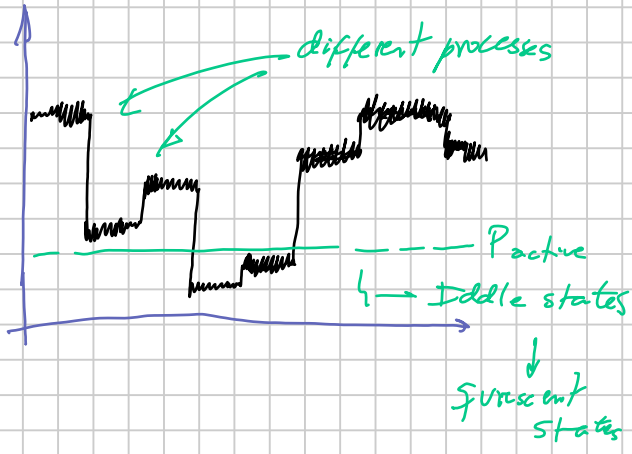


→ > Power → > heat

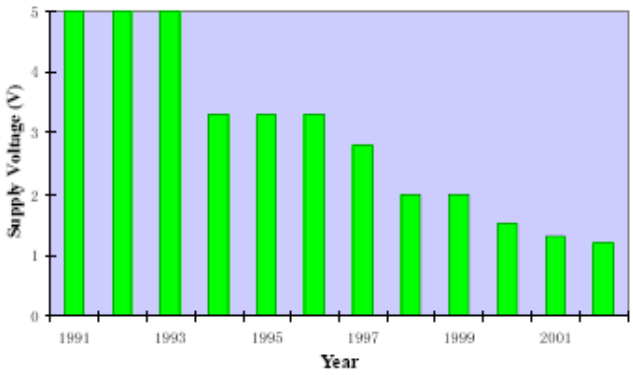
Fig. 1.3. Historical data on the increase in power for Intel CPUs.

R. Mahajan, R Nair, V Wakharkar, J Swan, John Tang and G Vandentop, "Emerging Directions for Packing Technologies", Intel Technology Journal Vol.6 Issue 2, May 16, 2002.

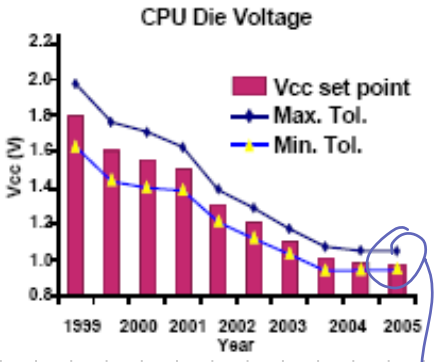
Some solutions → Manage CPU activity (A_V)

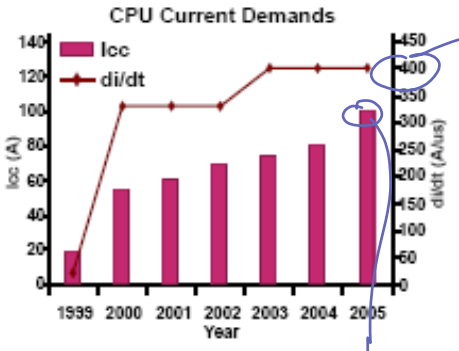


Reduce voltage → (P depends on V_{cc}^2 so voltage reduction has big impact)



(Based on data from *Intel Technology Symposium 2000*, by Dr. Anthony J. Stratakos, Volterra)



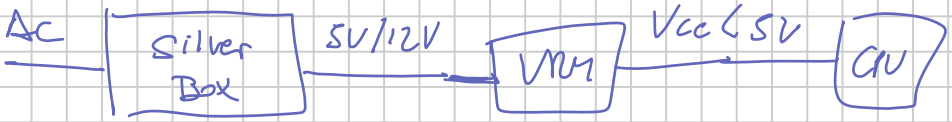


400A @ 1usec

>100A

tighter tolerable @ 1V

Typicall architecture

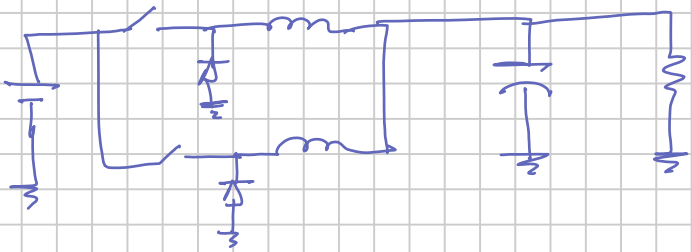


1st VRM topology → buck

↳ As power increases → high thermal demand on MOSFETS & inductor

↳ size (same power density)

Solutions → Use of multiphase Buck



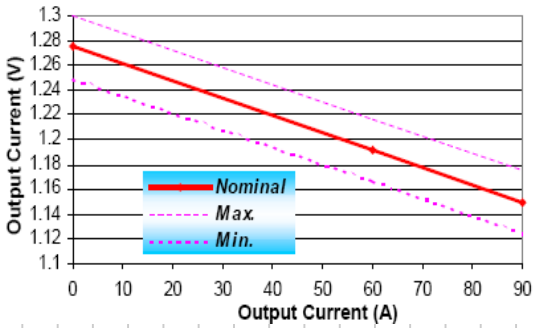
Increased voltage from 5V to 12V

Other problems → Fast load changes (slew rate)

several Amps./μsec

↳ overshoots → shorter life

↳ Undershoots → "blue screens"



→ Power dissipation and distribution

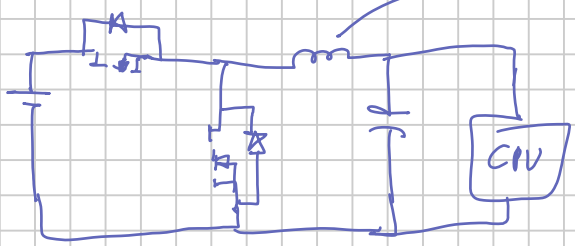
And of course → efficiency,

OSCON Caps → output caps → most expensive component

↳ used to filter ripple and handling load

Space → To minimize parasitic impedance VRM needs to be close to the CPU (takes CPU space)

Simplest VRM → Synchronous buck



Need to be small to improve transient response

↓

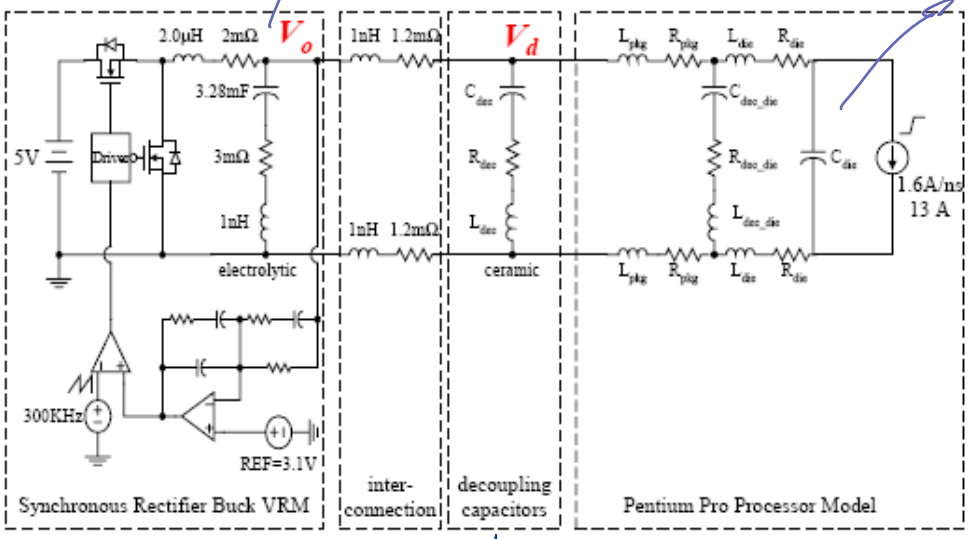
otherwise it may not be able to follow fast changes in CPU.

↓

Synchronous because MOSFET with low r_{dson} is more efficient than a diode

Multichannel interleaving improves transient issues

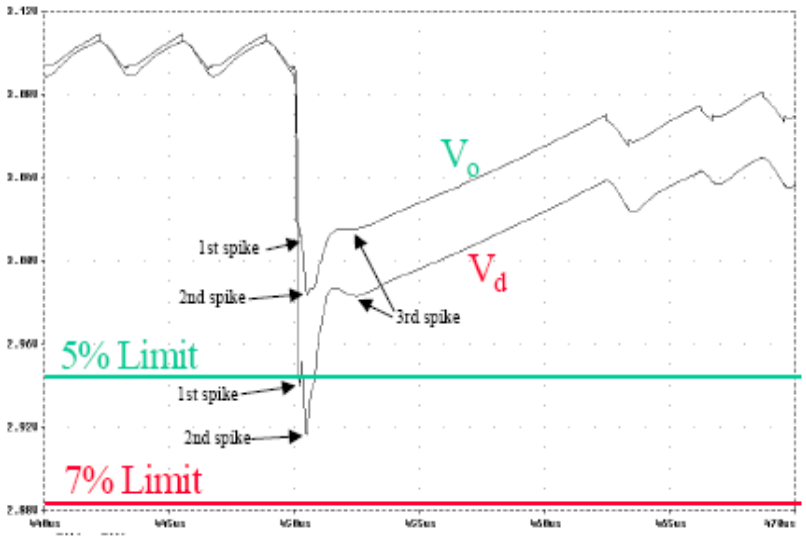
as low as

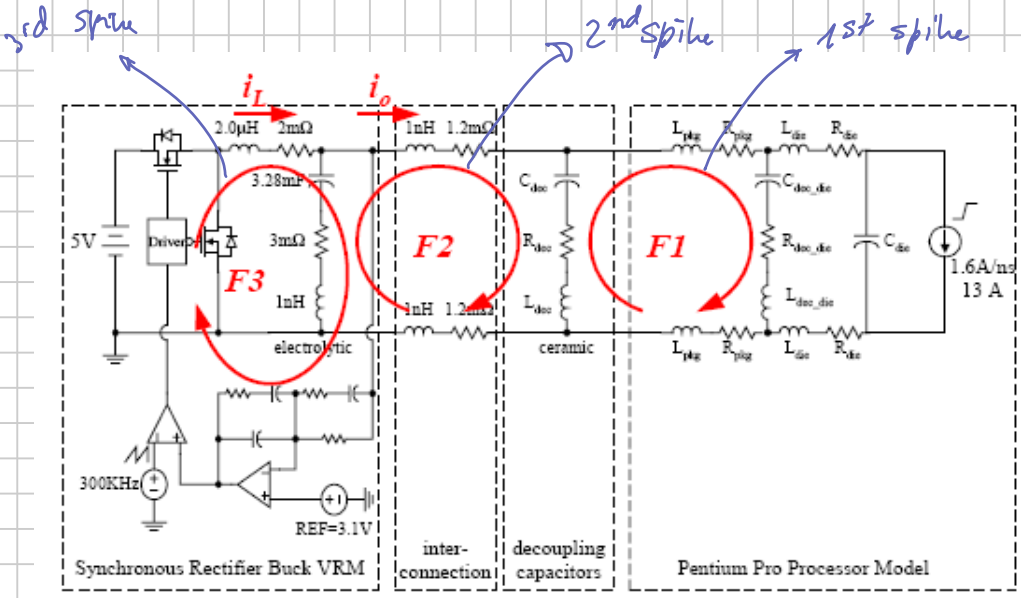


packaging caps

↳ Filter high frequency noise

Transients:





$f_1 > f_2 > f_3$

For smaller capacitance → larger inductor slew rate → smaller inductance

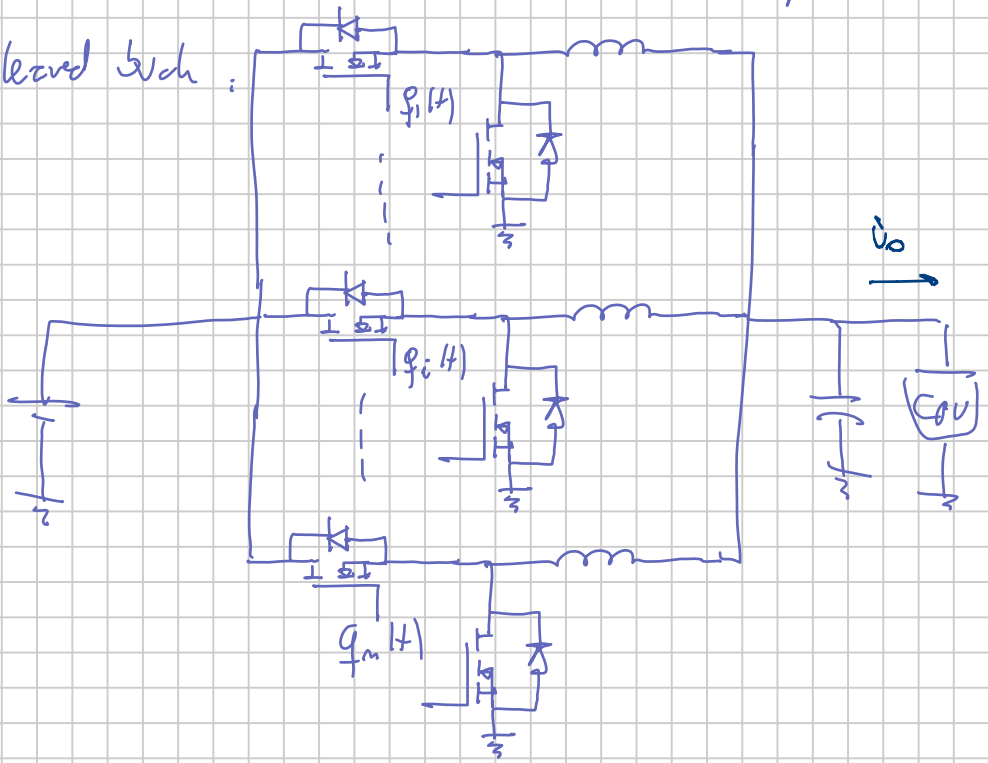
But → smaller inductance → larger inductor current ripple

↓

larger output voltage ripple

(more EMI, more losses in caps)

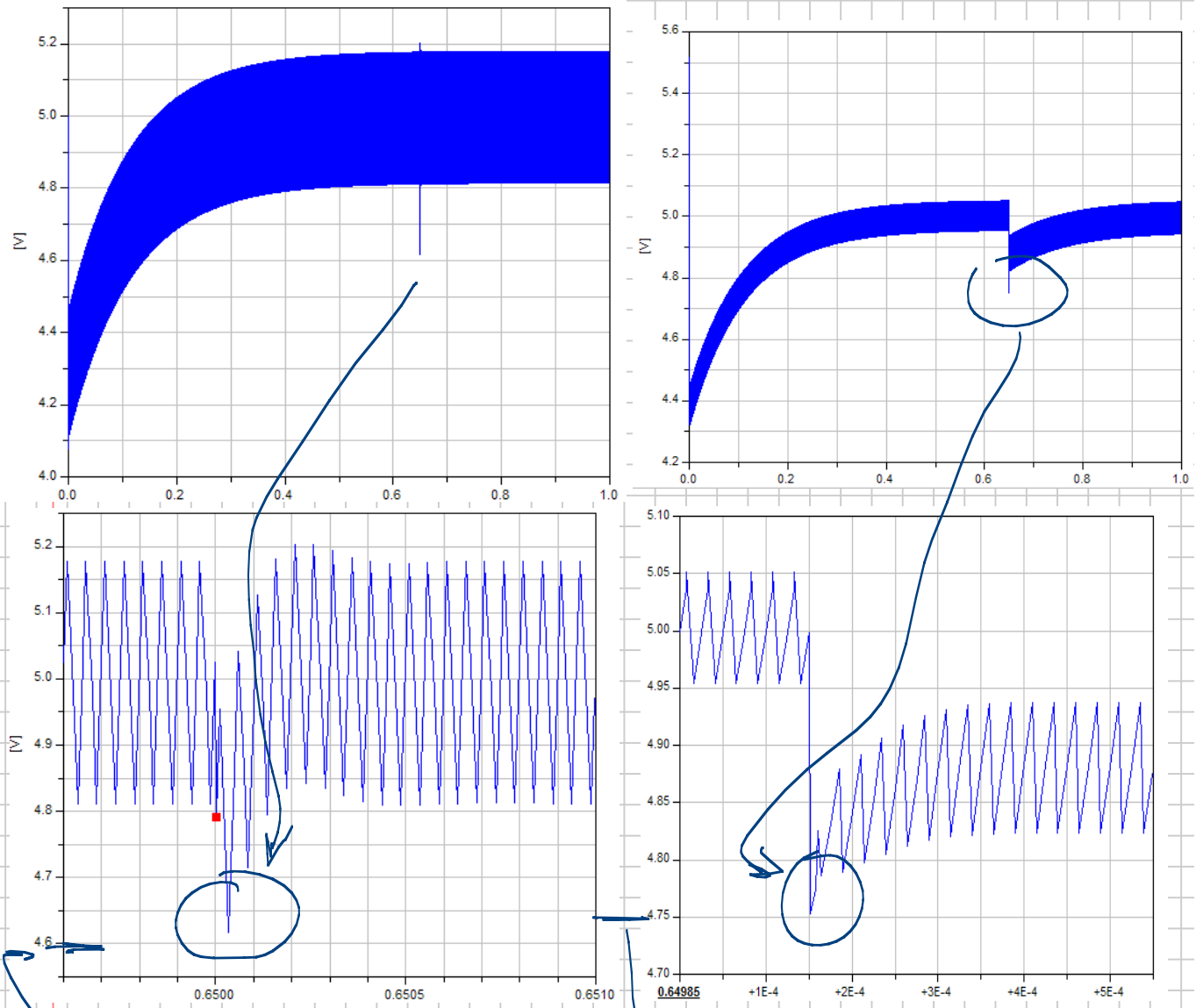
Solution: interleaved buck:



$$f_i(t) = f_1\left(t + i\frac{2\pi}{n}T\right)$$

$E = 12V, C = 3mF, L = 10\mu H, R_c = 0.025, i_L = 10,20A$

$k_i = 5, k_p = 0.5$ $\quad \Delta I = 10A/\mu sec$



Better than

Assume 2 phases:

$$\begin{cases} L\dot{x}_{11} = f_{11}(t)\,E - x_2 \\ L\dot{x}_{12} = f_{12}(t)\,E - x_2 \\ C\dot{x}_2 = x_{11} + x_{12} - i_o \end{cases}$$

$$\frac{di_o}{dt} = \dot{x}_{11} + \dot{x}_{12} - C\ddot{x}_2$$

Slow rate required by microprocessor

$\dot{x}_{11} = \frac{1}{L}(f_{11}E - x_2)$ $\quad \dot{x}_{12} = \frac{1}{L}(f_{12}E - x_2)$

$$\frac{di_o}{dt} = \frac{1}{L}(f_{11} + f_{12})E - \frac{2}{L}x_2 - C\ddot{x}_2$$