Condensed CV
Lizy Kurian John

EDUCATION: *(Year, Degree, Institution, major)*

1993	PhD	The Pennsylvania State University, Computer Engineering
1989	MS	The University of Texas at El Paso, Computer Engineering
1984	BS	The University of Kerala, India, Electronics and Communication

EXPERIENCE: *(Institution, rank(s), beginning and ending dates for each rank)*

The University of Texas at Austin	Cullen Trust for Higher Education Endowed Prof	2018 - present
The University of Texas at Austin	B. N. Gafford Professor in Electrical Engr	2009 - 2018
The University of Texas at Austin	Professor and Centennial Teaching Fellow	2007-2009
The University of Texas at Austin	Assoc Professor and Centennial Teaching Fellow	2001-2007
The University of Texas at Austin	Assistant Professor	1996-2001
The University of South Florida	Assistant Professor	1993-1996

HONORS AND AWARDS:

2020 Supervisor of UT Austin ECE Top Achiever Award Winner Ph. D Student
2019 IEEE MICRO Editor In Chief (2019-now)
2019 Facebook Research Award
2020 ARM Research Award
2018 Intel Research Award
2018 Supervisor, UT Austin Jacome Outstanding Dissertation Prize Winner
2017 HPCA Hall of Fame
2016 Best Paper Award, ACM Design Automation Conference (DAC)
2015 Best Paper Award, IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
2015 Best Paper Runner Up, IEEE International Conference on Parallel Processing (ICPP)
2012 ISCA Hall of Fame
2011 **Outstanding Engineering Alumnus of the Pennsylvania State University**, Computer Science &Engr dept
2011 Best Paper Nominee, IEEE/ACM Supercomputing Conference (SC'11)
2011 Best Paper Nominee, IEEE/ACM Micro conference (MICRO '11)
2011 **IEEE MICRO TOP PICKS 2010** ''Coordinating DRAM and Last-Level-Cache Policies with the Virtual Write Queue''
2010 Best Paper Nominee, IEEE Intl Symp on High Performance Computer Architecture (HPCA)
2009 IEEE Fellow
2009 Best Paper Award, IEEE International Conference on Parallel Processing (ICPP)
2008 IBM Faculty Partnership Award
2005 IBM University Partnership Award (2001, 2002, 2003, 2004, 2005, 2007, 2008, 2009)
2002 Advisor of the George H. Mitchell Undergraduate Student Achievement Award winner
2001 IBM Austin Center for Advanced Studies (CAS) Fellow (2001, 2002, 2003)
1999 Best Paper Award, IEEE International Performance Conference on Computing and Communication (IPCCC)
1996 NSF CAREER Award
1996 Oak Ridge Junior Faculty Enhancement Award

UT Austin Awards:
2004 TEXAS Alumni Association (Texas EXES) Teaching Award
2001 Engineering Foundation Faculty Award, College of Engineering, UT Austin
1999 Halliburton, Brown and Root Engineering Foundation Young Faculty Award, College of Engr

Other Honors:
1989 Graduate School Marshal for the December 1989 commencement at The University of Texas at El Paso
1977 National Talent Search Scholarship, NCERT INDIA, 1977-1984
1984 3rd Rank in the Kerala University B.Sc. Engineering Degree Exam

1979 Ist Rank, 1st out of 70,462 students in the Kerala University Pre Degree Exam, India
1977 2nd rank, 2nd out of 275,554 students in the Kerala State Higher Secondary School Exam, India

Keynotes/Plenary Talks:

2019 Keynote, The 17th International System-on-Chip (SoC) Conference, October 2019, Irvine, CA
2018 Keynote, IEEE Women in Engineering International Leadership Summit, August 8, 2018
2017 Keynote, IEEE Min-Move held with IEEE Parallel Architectures and Compilation (PACT) Conference
2017 Keynote, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)
2015 Invited Talk, Samsung SARC Technical Forum, "Machine Learning for Power Modeling and Prediction"
2015 Keynote, Huawei Strategic Workshop, China, "Many Big, Many Little: Who will crunch all the Big Data?
2014 Keynote Speech, BPOE Workshop in conjunction with ACM ASPLOS, Salt Lake City, Utah
2013 Invited Speech, ACM Supercomputing Conference, Performance Evaluation for Large Scale Systems: (Host: Bill Kramer, UIUC)
2011 Keynote, ACM International Conference on Performance Engineering (ICPE), Karlsruhe, Germany
2008 Keynote, IBM Center for Advanced Studies (CAS) Conference
2004 Keynote, Workshop on Commercial Workload Characterization (CAECW), Held with HPCA 2004, Spain

PATENTS: 13 US patents granted, + Pending US, Korea, China, Japan filings

Patent citations:
465 (total); 212 (cited in patents); 156 (non-patent lit); 96(legal)

1. U. S. Patent # 10,437,648, Guided Load Balancing of Graph Workloads on Heterogeneous Clusters, October 8, 2019
2. U. S. Patent 10,296,465, Processor Using a Level 3 Translation Lookaside Buffer implemented in OffChip or Die-Stacked Dynamic Random Access Memory, May 21, 2019
3. U.S. Patent 10,261,915, Intelligently Partitioning Data Cache to Allocate Space for Translation Entries, April 16, 2019
4. U. S. Patent 9,235,397, Method and Apparatus for increasing task execution speed, January 12, 2016 **(Samsung and UT joint)**
5. U. S. Patent 9,038,039, Apparatus and Method for Accelerating Java Translation, May 19, 2015 **(Samsung and UT joint)**
6. U. S. Patent 8,359,597, "Workload-guided application scheduling in multi-core system based at least on application branch transition rates, Jan 22, 2013
7. US Patent 8,250,350, "Computer System with non-volatile write-protected memory based operating system and secure system architecture, Aug 21, 2012 **(Texas Digital and Multimedia Systems)**
8. US Patent 8,230,407, "Apparatus and method for accelerating Java translation", July 24, 2012 **(Samsung and UT joint)**
9. US Patent 8,214,629, Computer system with secure instantly available applications using non-volatile write-protected memory", July 3, 2012 **(Texas Digital and Multimedia Systems)**
10. US patent 8,041,931, "Branch prediction apparatus, systems, and methods", Granted Oct 18, 2011 **(Patent has been licensed by UT)**
11. U S Patent 7,370,183,"Branch Predictor comprising a split branch history shift register". **(Patent has been licensed by UT.)**
12. U S Patent 7,107, 434, " System, Method and Apparatus for Allocating Hardware Resources using Pseudo Random Sequences". **(Patent has been licensed by UT.)**
13. U S Patent 5,867,422 " Computer Memory Chip with field Programmable Memory Cell Arrays", Granted Feb 1999. **(Licensed to a major FPGA Manufacturer.)**

BOOKS AUTHORED:

1. Digital Systems Design Using VHDL, Charles Roth and Lizy K. John, 3rd edition (Cengage Publishers, 2017)
2. Digital Systems Design Using Verilog, Charles Roth, Lizy K. John, and Byeong Kil Lee, Cengage Publishers, 2014, 581 pages)

3. Digital Systems Design Using VHDL, Charles Roth and Lizy K. John, 2nd edition (Thompson Engineering, 2006-2007, 580 pages)

BOOKS EDITED:

1. Computer Performance Evaluation and Benchmarking, CRC Press, 2005 (289 pages) (with L. Eeckhout)
2. Workload Characterization of Emerging Computer Applications, Kluwer Academic Publishers, 2001, ISBN 0-7923-7315-4
3. Workload Characterization for Computer System design, edited by L. K. John and A. M. Maynard, Kluwer Academic Publishers, 2000, 209 pages, ISBN 0-7923-7777-x.
4. Workload Characterization: Methodology and Case Studies, edited by L. John and A. M. Maynard, IEEE Computer Society, 153 pages, ISBN 0-7695-0452-3

PUBLICATIONS SUMMARY:

- Approximately 300 Publications
- 24 IEEE Transactions, 5 ACM Transactions
- 9 ISCA Papers (Member ISCA Hall of Fame 2012)
- 9 HPCA Papers (Member HPCA Hall of Fame 2017)
- H-index: 49 (31 since 2015)
- I-10 index: 162 (88 since 2015)
- 9300+ Citations (3600+ since 2015)
- 7 MICRO Papers
- 3 undergraduate Textbooks
- 4 Edited Books
- 16 Book Chapters

RESEARCH CONTRIBUTION SUMMARY:

Lizy John is a leader in the areas of performance/power modeling of computer systems, and workload characterization. She has contributed to the design and evaluation of microprocessors with her innovative methodologies for early design stage power and performance evaluations. She has done extensive workload characterization efforts which have led to memory hierarchy enhancements, accelerators and reconfigurable fabrics for Java, media and now machine learning workloads. She has also created proxy benchmarks for pre-silicon performance evaluation, synthetic proxies for database, Java and web server workloads, performance-event based power models, automatically generated stress benchmarks for finding realistic maximum power, maximum voltage droop, etc. Her research developed methodologies to characterize applications at an abstract level, which allowed to identify the generic properties of the application in terms of its memory access behavior, locality, branch behavior, instruction level parallelism, etc. Utilizing the abstract metrics of program behavior, a machine-independent program behavior model was generated. Her group's workload characterization led to program similarity/dissimilarity studies and clustering techniques that have been used in benchmark selection and subsetting by the SPEC, a consortium of companies such as IBM, Intel, Oracle, HP, etc. Currently, she is working on emerging workloads including big data and machine learning workloads, trying to create meaningful and manageable benchmarking strategies for these types of contemporary and emerging workloads.

Memory System: Lizy John's joint work with IBM resulted in several contributions to cache partitioning and DRAM policies that influenced IBM POWER8 and POWER9 memory systems and a series of 5 papers in key venues. A key component in the design was a hardware reuse distance profiler to dynamically monitor locality and adaptively make changes to cache partitioning. This profiler was implemented in the POWER systems. Jeff Stuecheli, her Ph. D student was the chief nest architect for POWER8, nest architect being the system level architect. The following works are indicative of the contributions: DRAM page mode scheduling (Micro 11, best

paper nominee), cache partitioning (ICPP2009 best paper award), Elastic refresh (Micro 2010), virtual write queue [ISCA2010].

1. D. Kaseridis, J. Stuecheli, and L. K. John, "Bank-Aware Dynamic Cache Partitioning for Multicore Architectures", Proceedings of the International Conference on Parallel Processing (ICPP), September 2009, Vienna Her work on last level cache management policies has had significant impact on the IBM POWER series cache and DRAM management policies. Jeff Stuecheli is IBM Power 8 Nest Architect. (**Won 2009 ICPP Best Paper Award**).
2. D. Kaseridis, J. Stuecheli, L. K. John, Minimalist open-page: A DRAM page-mode scheduling policy for the many-core era, Proceedings of ACM/IEEE MICRO 2011, (158 citations), **Best Paper Nominee**
3. D. Kaseridis, J. Stuecheli, J. Chen, and L. K. John, "A Bandwidth-aware Memory-subsystem Resource Management using Non-Invasive Resource Profilers for Large CMP Systems", Proceedings of IEEE High Performance Computer Architecture (HPCA) Symposium, 2010, pp. 93 – 103
4. J. Stuecheli, D. Kaseridis, H. C. Hunter, L. K. John, "Elastic Refresh: Techniques to Mitigate Refresh Penalties in High Density Memory", Proceedings of the Annual International Symposium on Microarchitecture (MICRO-2010), December 2010 (126 cites)
5. J. Stuecheli, D. Kaseridis, D. Daly, H. Hunter, L. K. John, "The Virtual Write Queue: Coordinating DRAM and Last-Level Cache Policies", Proceedings of the International Symposium on Computer Architecture (ISCA) 2010, pp. 72-82. (144 cites) **Was selected as IEEE Micro TOP PICKS**

Early contributions in Decoupled Computer Architectures:
ISCA 92 – L. Kurian (John), P. T. Hulina and L. D. Coraor, "Memory Latency Effects in Decoupled Architectures", This paper showed that when accesses and execute operations are decoupled using queues, often times the queues are empty rather than full because of the lack of balance between the access and execute streams. This led to the following work which proposed multiple load queues and more effective way of decoupling access and execute. HPCA 1995 – L. K. John, V. Reddy, P. Hulina and L. Coraor, "Program Balance and its Impact on High Performance RISC Architectures", This paper pointed out that the emerging Superscalar architectures are heavily imbalanced in their access-vs-compute capability and proposed using multiple load/store queues in order to enhance memory access capabilities, balance access/execute tasks and also suggested decoupling them to increase overlap.

Java acceleration: She made significant contributions to the acceleration of Java workloads that are ubiquitous in mobile platforms. Her group was the one of the first to provide detailed insights to performance bottlenecks of Java execution and proposed architectural support for acceleration. She developed a dynamic hardware translation engine for converting Java bytecodes to RISC instructions [R. Radhakrishnan, R. Bhargava, and L. K. John, "Improving Java Performance using Hardware Translation", Proceedings of the International Conference on Supercomputing (ICS 2001)]. This was one of the earliest Java acceleration engines which are now common in most mobile phones. Furthermore, acceleration engines were created for mobile phones in collaboration with Samsung resulting in 3 US Patents 8,230,407, 9,038,039 and 9,235,397. Another related paper:

R. Radhakrishnan, N. Vijayakrishnan, L. K. John, A. Sivasubramaniam, J. Rubio, and J. Sabarinathan, "Java Runtime Systems: Characterization and Architectural Implications", **IEEE Transaction on Computers**, Feb 2001, Vol.50, No. 2, pp. 131-146. (104 citations)

Power modeling

Prof. John was one of the first to show how power models can be built using performance metrics as a proxy. She showed how a processor power model can be built with just 2 performance counters. Google Scholar shows that her SIGMETRICS 2003 paper on this topic has been cited 313 times. Her "trickle down" power estimation research developed a methodology to estimate power of the system including memory and disk utilizing events at the core. This work [ISPASS 2007] has 218 citations. Recently her team has developed a cross-platform performance/power model using machine learning, which won the DAC Best Paper award in 2016. Prof. John's research in performance evaluation and workload characterization has had a profound impact on academia and the industry. Digital power meters that use processor events as a proxy has become very common now including in processors from Intel, AMD and Samsung.

1. Tao Li and Lizy Kurian John, "Run-time Modeling and Estimation of Operating System Power Consumption", In Proceedings of the International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), 2003, pp. 160-171. (313 citations)
2. William Lloyd Bircher and Lizy K. John, Complete System Power Estimation: A Trickle-Down Approach Based on Performance Events, ISPASS (IEEE International Symposium on Performance Analysis of Systems and Software) April 2007 (218 citations)
3. Lloyd Bircher and Lizy K. John, Complete System Power Estimation using Processor Performance Events, **IEEE Transactions on Computers**, Vol. 61, No. 4, pp. 563-577, April 2012 (229 citations)
4. W. Lloyd Bircher and Lizy K. John, " Analysis of Dynamic Power management on Multi-Core Processors", Proceedings of the International Conference on Supercomputing (ICS), 2008, pp/ 327-338, (37 accepts/ 140 submissions) (93 citations)
5. Wooseok Lee, Sunwoo, A. Gerstlauer, and L. K. John, "PowerTrain: A Learning-based Calibration of McPAT Power Models", ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2015
6. W. Lloyd Bircher, M. Valluri, J. Law and L. John, "Runtime Identification of Microprocessor Energy Saving Opportunities", International Symposium on Low Power Electronics and Design (ISLPED), Aug 2005, pp. 275-280. (Acceptance rate: 53 accepted/233 submissions = 23%) (128 citations)
7. Jian Chen and Lizy K. John, "Efficient Program Scheduling for Heterogeneous Multicore Processors", Proceedings of the 46th Design Automation Conference (DAC) July 2009 (161 citations)
8. Sudhanva Gurumurthi, Anand Sivasubramaniam, Mary Jane Irwin, Narayanan Vijaykrishnan, Mahmut Kandemir, Tao Li, and Lizy Kurian John, "Using Complete Machine Simulation for Software Power Estimation: The SoftWatt Approach", In Proceedings of the 2002 International Symposium on High Performance Computer Architecture (HPCA), Feb 2002, pp. 141-150. (Acceptance rate: 26 accepted/130 submissions = 20%) (274 citations)

Use of Machine Learning in Performance/Power/Reliability Evaluation

Estimating the power and thermal characteristics of a processor is essential for designing its power delivery system, packaging, cooling, and power/thermal management schemes. Power models that estimate the power consumption of each functional unit/hardware component from first principles are slow and tedious to build. Dr. John's research used machine learning can be used to create power models that are fast and reasonably accurate, and to calibrate analytical models that estimate power. Dr. John's research also crafted a very important application for machine learning - to create max power stressmarks. Manually developing and tuning so called stressmarks is extremely tedious and time-consuming while requiring an intimate understanding of the processor. Dr. John's research created a framework that uses machine learning for the automated generation of stressmarks. Yet another application for machine learning in Dr. John's research is in cross-platform performance and power prediction. If one model is slow to run real-world benchmarks/workloads, is it possible to predict/estimate the performance/power by using runs on another platform? Are there correlations that can be exploited using machine learning to make cross-platform performance and power predictions?

1. Xinnian Zheng, Lizy K. John, and Andreas Gerstlauer, Accurate Phase Level Cross-Platform Power and Performance Estimation, DAC 2016 **(Best Paper award)**
2. Arun Nair, Stijn Eyerman, Lizy K. John, Lieven Eeckhout, A First-Order Mechanistic Model for Architectural Vulnerability Factor, ACM International Symposium on Computer Architecture (ISCA) 2012, pp. 273-284
3. Karthik Ganesan and Lizy K. John. MAximum Multicore POwer (MAMPO) - An Automatic Multithreaded Synthetic Power Virus Generation Framework for Multicore Systems, **Best paper finalist** in the SuperComputing Conference (SC 2011), Seattle, WA, Nov 2011
4. Youngtaek Kim, Lizy Kurian John, "Automated di/dt stressmark generation for microprocessor power delivery networks," *International Symposium on Low Power Electronics and Design(ISLPED)*, pp. 253-258, Aug. 2011.

5. Arun Arvind Nair, Lizy Kurian John, and Lieven Eeckhout, " AVF Stressmark: Towards an Automated Methodology for Bounding the Worst-Case Vulnerability to Soft Errors", Proceedings of the Annual International Symposium on Microarchitecture (MICRO-2010), December 2010
6. K. Ganesan, Jungho Jo, W. Lloyd Bircher, D. Kaseridis, Zhibin Yu, and Lizy K. John, SYMPO: A Systematic Approach for Escalating System-Level Power Consumption using Synthetic Benchmarks", Proceedings of the 19th International Conference on Parallel Architectures and Compilation Techniques (PACT), Vienna, Austria, September 11-15, 2010.
7. A. Joshi, L. Eeckhout, L. K. John, and C. Isen, "Automated Microprocessor Stressmark Generation", Proceedings of the IEEE International High Performance Computer Architecture (HPCA) Symposium, 2008, pp. 229-239.

Pre-silicon performance evaluation

Modern microprocessors contain hundreds of millions of transistors and are built using millions of lines of VHDL/Verilog code. Pre-silicon estimation of performance and power of such designs for real-world workloads is important to identify good design points early in the design process. Lizy John applied workload characterization to create abstract models of workloads and synthetic test sequences, which became very instrumental in pre-silicon performance/power modeling. Her research has been able to create synthetic clones of real applications and benchmarks which act as performance/power proxies but without any functionality. The IBM POWER processor performance models have been validated using the synthetic benchmark approach created by her research. Lockheed Martin found these techniques useful to clone proprietary applications. The Semiconductor Research Consortium funded her research to develop pre-silicon design evaluation techniques. AMD, Freescale and Intel found these techniques extremely valuable in early stage design evaluation.

1. Lieven Eeckhout, Robert Bell Jr., Bastiaan Stougie, Koen De Bosschere, Lizy K. John, "Control Flow Modeling in Statistical Simulation for Accurate and Efficient Processor Design Studies", Proceedings of the International Symposium on Computer Architecture (ISCA), Munich, Germany, June 2004, pp. 350-361. (Acceptance rate: 31accepted/217 submissions = 14%) (150 citations)
2. Robert H. Bell, Rajiv R. Bhatia, Lizy John, Jeff Stuecheli, Ravel Thai, John Griswell, Paul Tu, Louis Capps, Anton Blanchard, "Automatic Testcase Synthesis and Performance Model Validation for High-Performance PowerPC Processors", Proceedings of the International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2006, pp. 154-165. (Acceptance rate: 24 accepted/81 submissions = 30%)
3. Robert H. Bell, Jr. and Lizy K. John "Improved Automatic Test case Synthesis for Performance Model Validation", 19th ACM International Conference on Supercomputing (ICS), June 2005, pp. 111-120. (91 citations)
4. Zhibin Yu, Lieven Eeckhout, Tao Li, Lizy K. John, , "GPGPU-MiniBench: Accelerating GPGPU Micro-Architecture Simulation", IEEE Transactions on Computers, 2015, Vol. 64, Issue 11, pp. 3153-3166
5. Arun Nair, Stijn Eyerman, Jian Chen, Lizy John, Lieven Eeckhout, "Mechanistic Modeling of Architectural Vulnerability Factor", **ACM Transactions on Computer Systems**, 2015, Vol. 32, Issue 4
6. Karthik Ganesan and Lizy K. John, Automatic Generation of Miniaturized Synthetic Proxies for Target Applications to Efficiently Design Multicore Processors, **IEEE Transactions on Computers**, Vol. 63, No. 4, pp. 833-846, April 2014

Performance Impact of Emerging Workloads and Contemporary Programming Paradigms:

Workload characterization and identification of bottlenecks allows computer architects to design computer systems that yield high performance, energy-efficient operation and reliability. Many emerging workloads contain thick software stacks with several layers of complex software accessing databases or various libraries and interacting with complex hardware. The suitability of various hardware features for the specific requirements of the software cannot be visualized intuitively any more. Understanding the nature of programs and the workload behavior leads to the design of improved computer architectures. Lizy John's research group focuses on workload characterization of

emerging application domains and emerging processor architectures. In past research, Lizy John has characterized Java workloads, multimedia workloads, smart phone apps, data base workloads (SQL and NoSQL) and identified bottlenecks during the execution of these types of workloads. The Java characterization work led to architectural enhancements for accelerating Java leading to multiple publications and 3 patents (jointly with Samsung).

1. R. Radhakrishnan, N. Vijayakrishnan, L. K. John, A. Sivasubramaniam, J. Rubio, and J. Sabarinathan, "Java Runtime Systems: Characterization and Architectural Implications", **IEEE Transaction on Computers**, Feb 2001, Vol.50, No. 2, pp. 131-146 (104 citations)
2. Deepu Talla, Lizy John, and Doug Burger, "Bottlenecks in multimedia processing with SIMD style extensions and architectural enhancements", **IEEE Transactions on Computers**, Volume 52, Number 8, ISSN 0018-9, Aug 2003, pp. 1015-1031 (147 citations)
3. R. Radhakrishnan, N. Vijaykrishnan, L. K. John and A. Sivasubramaniam, "Architectural Issues in Java Runtime Systems", Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA-2000), Toulouse, France, Jan 2000, pp. 387-398. (Acceptance rate: 35 accepted/163 submissions = 21%) (62 citations)
4. L. Tao, L. K. John, N. Vijayakrishnan, A. Sivasubramaniam, A. Murthy, and J. Sabarinathan, "Using Complete System Simulation to Characterize SPECjvm98 Benchmarks", Proceedings of the ACM International Conference on Supercomputing (ICS 2000), Santa Fe, New Mexico, May 2000, pp. 22-33. (Acceptance rate: 33 accepted/122 submissions = 28%) (61 citations)

Benchmarking:

Selecting benchmarks have largely remained an art. However, Dr. John's research demonstrated the use of clustering methodology and benchmark characterization techniques to understand similarity and dissimilarity between benchmarks and to create a suite that achieves the highest coverage of the design space. Her techniques were sought by SPEC, the industry standard computer performance evaluation corporation (www.spec.org) in the creation of the SPEC 2006CPU benchmark suite (See Henning's article Computer Architecture News, March 2007, pp. 119). She showed how principal component analysis (PCA) and clustering can be used to select benchmarks increasing the coverage of the workload space the suite covers. Her group's research received the best paper award at the 2006 SPEC workshop. Her technique was again sought by SPEC for creation of their 2017 SPEC CPU benchmark suite. Her work is cited frequently; for example, her 2005 ISPASS paper on program similarity has been cited 170 times and her 2007 ISCA paper on benchmark clustering is cited 226 times.

1. A. Phansalkar, A. Joshi and L. K. John, " Analysis of Redundancy and Program Balance in SPEC CPU 2006", ISCA 2007, San Diego, June 2007, pp. 412-423 (46 accepts/204 submissions) (226 citations)
2. J H Ryoo, S. Quirem, and L. K. John, "GPGPU Benchmark Suites: How well Do They Sample the Performance Spectrum", IEEE International Conference on Parallel Processing (ICPP) 2015 (Best Paper Runner Up)
3. Reena Panda, Shuang Song, Joseph Dean and Lizy K. John, Wait of a Decade: Did SPEC CPU 2017 Broaden the Performance Horizon", Proceedings of the IEEE High Performance Computer Architecture (HPCA) Symposium, Vienna, February 2018
4. Aashish Phansalkar, Ajay Joshi, Lieven Eeckhout, and Lizy K. John, "Measuring Program Similarity", Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 05), April 2005, pp. 10-20. (Acceptance rate: 27 accepted/92 submissions = 29%) (170 citations)
5. H. Nguyen and L. John, "Exploiting SIMD Parallelism in DSP and Multimedia Algorithms Using the AltiVec Technology", Proceedings of the ACM International Conference on Supercomputing (ICS 99), Greece, June 1999, pp. 11-20. (Acceptance rate: 57 accepted/180 submissions = 32%) (119 citations)
6. Ajay Joshi, Aashish Phansalkar, Lieven Eeckhout, and Lizy K. John, "Measuring Benchmark Similarity Using Inherent Program Characteristics", **IEEE Transactions on Computers**, Vol. 55, No. 6, June 2006, pp. 769-782. (152 citations)
7. Kenneth Hoste, Aashish Phansalkar, Lieven Eeckhout, Andy Georges, Lizy K. John and Koen De Bosschere, "Performance Prediction based on Inherent Program Similarity", Proceedings of Parallel Architectures and Compilation Techniques (PACT), Sept. 2006. (165 citations)

8. R. Bhargava, L. K. John, B. L. Evans, and R. Radhakrishnan, "Evaluating MMX Technology using DSP and Multimedia Applications", Proceedings of the IEEE Symposium on Microarchitecture (MICRO-31), Dallas, Texas, Dec 1998, pp. 37-46. (Acceptance rate: 28 accepted/108 submissions = 26%) (140 citations)
9. Byeong Kil Lee and Lizy K. John, "NpBench: A Benchmark Suite for Control Plane and Data Plane Applications for Network Processors", ICCD 2003, pp. 226-233. (Acceptance rate: 61 accepted/233 submissions = 26%) (75 citations)

Architectural Enhancements:

She has conducted in-depth workload characterization in fields such as multimedia and Java processing. Her Micro 98 paper on MMX has 140 citations and her 2003 IEEE Transactions paper devising the MediaBreeze architecture has 147 citations. When the industry was focusing on exploiting more parallelism in the SIMD part of the code, her workload characterization showed that the serial code on the host processor was the bottleneck. Acceleration techniques for the serial part of the code were devised in the MediaBreeze architecture. Her student who worked on the MediaBreeze architecture (Deepu Talla) is now VP at NVIDIA. Her workload characterization has continually exposed bottlenecks which were quite non-intuitive. She was part of the TRIPS project [6] and has done work on innovative basic building blocks such as the 10-transistor static energy recovery adder [5] (cited 277 times) to a reconfigurable interconnect [4] (88 citations).

1. R. Bhargava, L. K. John, B. L. Evans, and R. Radhakrishnan, "Evaluating MMX Technology using DSP and Multimedia Applications", Proceedings of the IEEE Symposium on Microarchitecture (MICRO-31), Dallas, Texas, Dec 1998, pp. 37-46. (Acceptance rate: 28 accepted/108 submissions = 26%) (140 citations)
2. Muhammad Umar Farooq, Khubaib, and Lizy K. John Store-Load Branch (SLB) Predictor: A Compiler Assisted Branch Prediction for Data Dependent Branches The 19th IEEE International Symposium on High Performance Computer Architecture (HPCA), 2013
3. Deepu Talla, Lizy John, and Doug Burger, "Bottlenecks in multimedia processing with SIMD style extensions and architectural enhancements", **IEEE Transactions on Computers**, Volume 52, Number 8, ISSN 0018-9, Aug 2003, pp. 1015-1031 (147 citations)
4. Lizy Kurian John and Eugene B. John, "A Dynamically Reconfigurable Interconnect for Array Processors", **IEEE Transactions on VLSI**, March 1998, Vol. 6, No. 1, pp. 150-157. (88 citations)
5. R. Shalem, E. John and L. K. John, "A Novel Low Power Static Energy recovery Full Adder Cell", Proceedings of the 1999 IEEE Great Lakes Symposium on VLSI, Michigan, March 1999, pp. 380-383. (277 citations)
6. D. Burger, S. Keckler, K. S. McKinley, M. Dahlin, L.K. John, C. Lin, C. R. Moore, J. Burrill, R. G. McDonald, W. Yoder and the TRIPS team, "Scaling to the End of Silicon with EDGE architectures", **IEEE Computer**, July 2004, pp. 44-55. (452 citations)

SERVICE TO PROFESSION:

IEEE MICRO Editor in Chief (2019-)
ACM Transactions on Architecture and Code Optimization (TACO), Associate Editor, 2014-2019
ACM TACO Editor–in-Chief Search Committee Member, 2020
ACM TACO Editor–in-Chief Search Committee Member, 2008
IEEE TCCA Executive Committee Member (2018-)
ICPP (International Conference on Parallel Processing) Program Co-Chair, 2020
ACM SIGMICRO Vice Chair, 2006-08
ACM SIGMICRO Member at large, 2005-2006
ACM SIGMICRO Public Relations Director 2002-03, 2001-02
Associate Editor, IEEE Transactions on Sustainable Computing, 2016-2019
Associate Editor, IEEE Transactions on Computers, 2009-2014
Associate Editor, IEEE Transactions on VLSI, 2003-07
Associate Editor, IEEE Computer Architecture Letters, 2016-2019

Associate Editor, IEEE MICRO, 2005-2018
Editorial Board, International Journal on Embedded Systems, 2005-14

Founded the IEEE International Symposium on Workload Characterization (IISWC)
Co-founded IEEE International Symposium on Performance Analysis of Systems and Software (lSPASS)

SPEC Dissertation Award Committee Chair, 2016
IEEE Fellows Selection Committee (Computer Society), 2015
IEEE Fellows Selection Committee (Computer Society), 2013
DOE Panelist/Proposal reviewer, various years, 2010-2014
NSF Panelist/Proposal reviewer, various years 1997-2015
Steering Committee Member, SPEC RESEARCH, 2013-2014
Steering Committee Member, SPEC RESEARCH, 2012-2013
Steering Committee Member, SPEC RESEARCH, 2011-2012
Steering Committee Member, SPEC RESEARCH, June 2010-2011
Member, Industrial and Professional Advisory Council (IPAC), Penn State College of Engineering, 2008-2015
Member, IEEE Senior Member Selection Panel, October 2007
Member, External Advisory Board, ECE Department, UT El Paso, 2008-
Member, External Advisory Board, University of North Texas, 2008-
Steering Committee, SPEC workshops, 2005-2007
Registration Chair - ACM International Symposium on Microarchitecture, MICRO-31, Dallas, TX, Dec 1998
Travel Awards Chair, International Symposium on Parallel Architectures and Compilation techniques (PACT 2003)
Reviewer for Addison Wesley (1997)
Kluwer Academic Publishers Book Proposal Reviewer, 2001

General Chair

ACM International Conference on Performance Engineering (ICPE) 2015
IEEE International Symposium on Workload Characterization (IISWC) 2005
IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 05
IEEE Intl Workshop on Workload Characterization (WWC), 1998-2005

Steering Committee Chair

IISWC (IEEE International Symposium on Workload Characterization), 2005-2007
ISPASS (IEEE International Symposium on Performance of Software and Systems), 2008-2013

Program Committee Chair ISCA 2021, ICPP 2020, ICPP 2013 Performance Track, **ACM** ICPE 2012 Program co-Chair (SPEC side)**,** SPEC Workshop 2006, Program co-chair**,** ISPASS 2004 (IEEE International Symposium on Performance Analysis of Systems and Software), ICCD Architecture track 1999 etc.

Technical Program Committee Member, ISCA 2015, SC'15, ISCA 2012, IPSASS'12, SC '11, ICS'11, PACT 2010, PACT 2009, VEE 2008, SC'2007, HPCA 2005, HPCA 2002, MICRO TOP PICKS 2006, MICRO TOP PICKS 2009, etc

Steering Committee Member, IISWC (IEEE International Symposium on Workload Characterization), 2007-present, ISPASS (IEEE International Symposium on Performance of Software and Systems), 2001-present, Workshop on Workload Characterization (WWC) (Since inception 1998 till it became IISWC 2006)

UT Austin Service: Information Technology Committee Chair (2019-2020), ECE Faculty Search Committee co-Chair (2019-2020), UT Austin Financial Aid Committee Chair 2012-2013, Cockrell School Honors Committee Chair and member various years, ECE Faculty Evaluation committee, ECE faculty search committee, Computer Architecture track Ph. D Coordinator, ECE Appeals committee, various years, Circuit design program Minority Liaison 2006-2009, Computer Engineering Ph. D coordinator 2007-2014

Local Schools Service: Technology Club Organizer, Spelling Coach, Science Fair Judge, Speaker, etc.

GRANTS AND CONTRACTS: (Co-principal investigators (if any), title of grant, sponsoring agency, total dollar value, beginning and ending dates)

1. Novel Computing Paradigms for Partial Differential Equations, $488,375, Exon Mobil, July 2019 – Dec 2021 (co-PI)
2. Intel Corporation, "Miniaturized Proxies of Industry Standard Benchmarks for Pre-silicon Evaluation", $240K, June 2017-June 2020
3. **National Science Foundation (NSF),** "Predictive Modeling for Next Generation Heterogeneous System Design", $1 Million, Oct 2018-Sept 2021 (Co-PI)
4. Samsung GRO Grant, "Learning Based Thermal Modeling", $99K, Oct 2018-Sept 2019. (Co-PI)
5. **NSF,** "Improving Research Reproducibility using Proxy benchmarks", $214K, Oct 2017-Sept 2019 (Sole PI)
6. **NSF,** SPX: "Computing in Situ and In Transit for Hierarchical Numerical Algorithms", $800K, Sept 2017-Aug 2020 (Co-PI)
7. Samsung Austin Research Center, "Trace Snippets for RTL Power Modeling", $99,990, Dec 2016-June 2018 (Sole-PI)
8. Intel Corporation, "Power-Aware System Compilation", $300K, Oct 2013-Sep 2016, (Co-PI)
9. Oracle Corporation, "A Methodology to Identify Application Memory Access Patterns for Efficient Hierarchical Memory Subsystem", $97,283, June 2015-May 2016 (Sole PI)
10. Samsung GRO Grant, "Adaptive Energy-Efficient Designs for Next Generation Smart Phone CPUs", $99,985, Sep 2015-Aug 2016 (Co-PI)
11. Samsung GRO Grant, "Scalable Network/System Co-Simulation For Power and Performance Aware Network of Systems Design", $99,985, Sep 2015-Aug 2016 (Co-PI)
12. Huawei Corporation, "Big Data Workload Energy Characterization", $110,000, June 2014-May 2015 (Sole PI)
13. Oracle Corporation, "A Methodology to Generate Miniature Proxies for Database workloads", $60,000, Jan 2014-Dec 2016
14. Semiconductor Research Consortium (SRC), "Workload characterization for Big Data", $240,000, Sep 2013-Aug 2016 (Sole PI)
15. **NSF,** XPS: "Algorithms and Architectures for Multiresolution Applications", $749,801, Sep 2013-Aug 2015
16. AMD Corporation, "Decomposition of Large Data Analytics into Hierarchical Models", $50,000, June 2013-May 2015
17. Oracle Corporation, "A Methodology to Identify Application Memory Access Patterns for Efficient Hierarchical Caching", $60,000, June 2013-May 2014.
18. **NSF,** SHF: "Sustainable and Reliable Multicore and Many-Core Computing via Cross-Layer Solutions", $300,000, Sep 2012-Aug 2015 (Co-PI)
19. Semiconductor Research Consortium (SRC), "Multi-dimensional Modeling, Design and Exploration of Multi-core SoCs", $345K, May 2012-April 2015 (Co-PI)
20. AMD Corporation, "Automatic Generation of Multicore Proxy Workloads and Stressmarks", $50K, April 2012-March 2013 (Sole-PI)
21. AMD Corporation, "Multicore Stressmarks", $50K, April 2011-March 2012 (Sole-PI)
22. **NSF**, SHF: Small: "Workload Characterization and Benchmark Synthesis for Emerging Computing Systems", $425,000, Sept 2011-Aug 2015.
23. AMD Corporation, "Stress-testing Multicore Processors for Worst-Case Power Consumption and Voltage Emergencies", $50,000, April 2010-March 2011 (Sole-PI)
24. Semiconductor Research Consortium (SRC), "Power Consumption Based Multicore Task Scheduling and Load Balancing", $360,000, April 2011-March 2014 (Co-PI)

25. Lockheed Martin, "Performance Cloning for Dissemination of Proprietary Applications to Hardware Vendors", $100,000, 2008-2009 (Sole PI)
26. Sun Microsystems, "Benchmark Synthesis for Performance and Power Modeling", $45,000, 2008-2009 (Sole PI)
27. IBM Faculty Award, Workload Characterization, $15,000, 2008-2009 (Sole PI)
28. **NSF**, Collaborative Research Archer: "Seeding a Community Based computing Infrastructure for Computer Architecture Research and Education", $67,631, 2008-2010 (Co-PI)
29. AMD Corporation, "Computer Architecture Research", $8,000, Dec 2007-Dec 2008 (Sole PI)
30. Semiconductor Research Consortium (SRC), "Automatic Benchmark Synthesis for Validation of Performance and Power Models of High-Performance Processors", $330,000, April 2008-March 2011 (Co-PI)
31. NSF, "Simplifying Performance Evaluation using Workload Characterization", $300,000, Sep 2007-Aug 2011 (Sole PI)
32. AMD Corporation, "Computer Architecture Research", $5000, Nov 2006-Nov 2007 (Sole PI)
33. IBM Faculty Partnership Award, $25,000, June 2007 (Sole PI)
34. IBM Center for Advanced Studies (CAS) Faculty Partnership Award, $7500, June 2006 (Sole PI)
35. AMD Corporation, "Computer Architecture Research", $5,000, Nov 2005 (Sole PI)
36. Samsung Corporation, "Java Accelerators", $128,000, Feb 2005-Aug 2006 (Sole PI)
37. IBM Center for Advanced Studies (CAS) Faculty Partnership Award, $25,000, June 2005(Sole PI)
38. **NSF,** "Statistical Techniques for Computer Performance Evaluation", $200,000, 2004-2008 (Sole PI)
39. AMD Corporation, "Computer Architecture Research", $5,000, Jan 2005 (Sole PI)
40. IBM Performance Evaluation Research, $500, Dec 2004 (Sole PI)
41. IBM Center for Advanced Studies (CAS) Faculty Partnership Award, "Statistical Techniques in Performance Evaluation and Benchmarking", $25,000, July 2004 (Sole PI)
42. Hewlett Packard, "Computer Architecture Research", $800, June 2004 (Sole PI)
43. Intel Corporation, "Performance Impact of Emerging Workloads on Intel Processors", $35,000, March 2004 (Sole PI)
44. AMD Corporation, "Research in Computer Architecture and Workload Characterization", $3000, Dec 2003 (Sole PI)
45. IBM Faculty Partnership Award Project: "Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads", $25,000, June 2003 (Sole PI)
46. Intel Corporation, "Performance Impact of Emerging Workloads on Intel Processors", $35,000, May 2003 (Sole PI)
47. IBM Shared University Research (SUR) grant, $60,000, 2002
48. IBM Faculty Partnership Award- "Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads", $25,000, June 2002 (Sole PI)
49. AMD Corporation, "Research in Computer Architecture and Workload Characterization", $5,000, May 2002 (Sole PI)
50. Intel Corporation, "Performance Impact of Emerging Workloads on Intel Processors", $35,000, March 2002 (Sole PI)
51. Motorola Corporation, "Development and Characterization of Control-Plane Network Workloads", $50,000, Jan 2002
52. AMD Corporation, "Computer Architecture Research", $5000, Dec 2001 (Sole PI)
53. IBM Shared University Research (SUR) Grant, $100,000, 2001
54. **NSF,** "Designing Microprocessors and Computer Systems for Emerging Workloads", $265,000, 2001-2004 (Sole PI)

55. IBM Faculty Partnership Award- "Effectiveness of Out of Order Microarchitectural techniques for web server workloads", $30,000, May 2001 (Sole PI)
56. Tivoli Corporation, "Understanding and Optimizing e-Business workloads and the underlying infrastructure", Aug 2000 (Sole PI)
57. IBM Center for Advanced Studies Partnership Award- "Effectiveness of Out of Order Microarchitectural Techniques for web server workloads", $25,000, March 2000 (Sole PI)
58. **NSF CAREER Award-** "Improving the Access-Execute Balance and Concurrency in High Performance Processor"s, $315,000, 1996-2000 (Sole-PI)
59. UT Co-op Book Subvention Grant, $2500, Aug 1999 (Sole-PI)
60. DELL-LARIAT grant- "Characterization of Multimedia Application and Analysis of their Performance Impact", $32,127, July 1999 (Sole-PI)
61. Intel Corporation, Workshop on Workload Characterization, $4000, July 1999 (Sole-PI)
62. Intel Corporation, Computer hardware grant- "Characterization of Multimedia Workloads and Analysis of their Performance Impact", $4,181, July 1999(Sole-PI)
63. Intel Corporation, "Web Server Characterization Studies on the Pentium Platforms", $15,320, Dec 1998
64. DARPA, TRIPS: "The Tera-op Reliable Intelligently adaptive Processing System Implementation for Polymorphous Computing Architectures (PCA)", $7,617,912, 2003-2005 (Co-PI)
65. DARPA, TRIPS: "The Tera-op Reliable Intelligently adaptive Processing System", $3,027,480, June 2001-May 2003 (Co-PI)
66. State of Texas Advanced Technology Program (ATP) Grant, "High Performance MultiMedia Processors", $157,800, Jan 2000 - Dec2001 (PI)
67. **NSF,** "Impact of Contemporary Programming Paradigms and Workloads", $356,314, 1998-2001
68. State of Texas Advanced Technology Program (ATP) Grant, "High Performance Digital Signal Processors", $134,640, Jan 1998-Dec 1999 (Co-PI)
69. IBM- SUR Grant- "End-to-End Measurement, Modeling and Simulation of Parallel/Distributed Computer Systems", $100K, Oct 1997
70. **NSF** CISE Infrastructure Grant, Developing a Design Automation Infrastructure, $373,524, 1995-19 (Co-PI)

PH.D. SUPERVISIONS COMPLETED:

Shuang Song	May 2020	Distributed Graph Processing (Facebook)
Jiajun Wang	May 2019	Data Reuse Optimization (Google)
Michael LeBeane	Aug 2018	Optimizing Communication for Clusters of GPUs (AMD)
Reena Panda	Dec 2017	Proxy Benchmarks for Emerging Workloads (Apple)
Wooseok Lee (0.5)	May 2018	Power Aware Mobile Systems (Samsung)
Xinnian Zheng (0.5)	May 2017	Learning Based Performance Modeling (NVIDIA)
Jee Ho Ryoo	May 2017	Heterogeneous Memory Systems (Oracle)
M. Faisal Iqbal	Aug 2013	Multicore Communication Processors
Youngtaek Kim	May 2013	Stressmarks for Voltage Emergencies (Intel)
M. Umar Farooq	Dec 2013	Value Based Branch Prediction (ARM)
Arun Arvind Nair	May 2012	Modeling of Soft Errors (AMD)
Karthik Ganesan	Dec 2011	Automatic Generation of Synthetic Workloads for Multicore Systems (Oracle)
Jian Chen	May 2011	Resource Management for Efficient Single-ISA Heterogeneous Computing (Intel)
Ciji Isen	May 2011	The Use of Memory State Knowledge to Improve Computer Memory System Organization (AMD)
Jeff Stuecheli	May 2011	Ccordinated Memory Scheduling (IBM)
Dimitris Kaseridis	May 2011	Memory-subsystem Resource Management for the Many-core Era (ARM Corporation)
Lloyd Bircher	Dec 2010	Predictive Power Management for Multi-Core Processors (AMD)

Ajay Joshi	Dec 2007	Constructing Adaptable and Scalable Synthetic Benchmarks for Microprocessor Performance Evaluation (ARM)
Aashish Phansalkar	May 2006	Similarity Analysis and Benchmark Subsetting (Employed at Intel)
Rob Bell Jr.	Dec 2005	Automatic Workload Synthesis for Early Design Studies and Performance Model Validation (IBM, Samsung)
Byeong Kil Lee	Aug 2005	Network Processor Design: Benchmarks and Architectural Alternatives (Employed at Texas Instruments)
Shiwen Hu	Dec 2005	Effective Adaptive Computing Environment Management via Dynamic Optimization, (Freescale)
Yue Luo	Aug 2005	Improving Sampled Microprocessor Simulation (Microsoft)
Madhavi Valluri	May 2005	A Hybrid-Scheduling Approach for Energy-Efficient Superscalar Processors (Employed at IBM)
Juan Rubio	Aug 2004	Exploring the Potential of a Hierarchical Computing Model for a Commercial Server (IBM Austin Research Lab)
Tao Li	Aug 2004	OS-aware Architecture for Improving Microprocessor Performance and Energy Efficiency, (Professor University of Florida)
Ravi Bhargava	Aug 2003	Instruction History Management for High-Performance Microprocessors (Employed at AMD)
Deepu Talla	Aug 2001	Architectural Techniques to Accelerate Multimedia Applications on General-Purpose Processors, August 2001 (Vice President at NVIDIA)
Ramesh Radhakrishnan	Aug 2000	Microarchitectural Techniques to Enable Efficient Java Execution (Strategic Technology Office, Dell)

M.S. SUPERVISIONS COMPLETED: *(Name, year, major department, name of institution (May want to add another column for titles.)*

Abigail Dowd	May 2020	Electrical and Computer Engineering
Snehil Verma	May 2020	Electrical and Computer Engineering
Harsh Gugale	May 2020	Electrical and Computer Engineering
Jim Xavier	May 2020	Electrical and Computer Engineering
Bagus Hanindhito	May 2020	Electrical and Computer Engineering
Shuang Song	Dec 2019	Electrical and Computer Engineering
Jiajun Wang	Dec 2018	Electrical and Computer Engineering
Sarbartha Banerjee	May 2018	Electrical and Computer Engineering
Yashwant Marathe	May 2018	Electrical and Computer Engineering
Alex Schulyak	Dec 2016	Electrical and Computer Engineering
Joseph Whitehouse	May 2016	Electrical and Computer Engineering
Jee Ho Ryoo	May 2014	Electrical and Computer Engineering
Darshan Gandhi	May 2014	Electrical and Computer Engineering
Abhishek Tondon	Dec 2013	Electrical and Computer Engineering
Don Owen	May 2013	Electrical and Computer Engineering
Ankita Garg	May 2013	Computer Sciences
Bhargavi Narayanasetty	May 2011	Electrical and Computer Engineering
Chaitanya Nayak	May 2011	Electrical and Computer Engineering
Rengarajan	2010	Electrical and Computer Engineering
Karthik Ganesan	Dec 2008	Electrical and Computer Engineering
Rajiv Bhatia	Aug 2008	Electrical and Computer Engineering
Justin Friesenhahn	Dec 2007	Electrical and Computer Engineering
Jason Matalka	Aug 2006	Electrical and Computer Engineering
Kathryn Stacer	May 2006	Electrical and Computer Engineering
Lloyd Bircher	May 2006	Electrical and Computer Engineering
Diego Vila	May 2006	Electrical and Computer Engineering
Brijesh Patel	2005	Electrical and Computer Engineering
Jenson Lam	2005	Electrical and Computer Engineering
Brian Gaide	2005	Electrical and Computer Engineering
Jignesh Gondalia	2005	Electrical and Computer Engineering

Saket Kumar	May 2004	Electrical and Computer Engineering
Michael Arunkumar	Dec 2003	Electrical and Computer Engineering
Michael Lance Karm	Dec 2003	Electrical and Computer Engineering
Patrick James Peters	Dec 2003	Electrical and Computer Engineering
Mike Clark	May 2003	Electrical and Computer Engineering
Anand Sunder Rajan	2003	Electrical and Computer Engineering
James Yang	2002	Electrical and Computer Engineering
Ravi Bhargava	Aug 2000	Electrical and Computer Engineering
Vikram Godbole	May 2000	Electrical and Computer Engineering
Sanjeev Ghai	May 2000	Electrical and Computer Engineering
Srikanth Kannan	May 2000	Electrical and Computer Engineering
Jyotsna Sabarinathan	Dec 1999	Electrical and Computer Engineering
Jody Joyner	Dec 1999	Electrical and Computer Engineering
Juan Rubio	May 1999	Electrical and Computer Engineering
Poorva Murarka	May 1999	Electrical and Computer Engineering
Purnima Vasudevan	May 1999	Electrical and Computer Engineering
Roy Shalem	Aug 1998	Electrical and Computer Engineering
Dachih-Tang	Aug 1998	Electrical and Computer Engineering
Yin Teh	Dec 1997	Electrical and Computer Engineering
Ramesh Radhakrishnan	Aug 1997	Computer Science and Engineering
Vijay Kammila	Dec 1996	Computer Science and Engineering
Vinod Reddy	Dec 1996	Computer Science and Engineering
Amudha Muthiah	Dec 1996	Computer Science and Engineering
Raghuveer Reddy	May 1995	Computer Science and Engineering