Lizy Kurian John

Cullen Trust for Higher Education Endowed Professor
Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, TX 78712
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EDUCATION: (*Institution, major, degree, dates)*

The Pennsylvania State University	Computer Engineering	Ph.D.	August 1993
The University of Texas at El Paso	Computer Engineering	M.S.	December 1989
The University of Kerala, India	Electronics and Communication Engineering	B.S.	August 1984

PROFESSIONAL REGISTRATION:

Texas Professional Engineer (PE) License, Since 2001

CURRENT AND PREVIOUS ACADEMIC POSITIONS: (*Institution, rank(s), beginning and ending dates for each rank)*

The University of Texas at Austin	Truchard Foundation Chair In Engineering, ECE	Sep 2022 – date
The University of Texas at Austin	Oden Institute Affiliate Faculty	Aug 2023 – date
The University of Texas at Austin	Cullen Trust for Higher Education Endowed Professorship No. 3	Sep 2018 – Aug 2022
University of Sydney	Research Affiliate (Visiting Researcher), Comp Sci	July 2022– Aug 2022
Stanford University	Visiting Professor	Sep 2021-May 2022
The University of Texas at Austin	B. N. Gafford Professor in Electrical Engineering	Fall 2009 - Summer 2018
The University of Texas at Austin	Professor and Centennial Teaching Fellow	Fall 2007-Summer 2009
The University of Texas at Austin	Associate Professor and Centennial Teaching Fellow	Fall 2001-Summer 2007
The University of Texas at Austin	Assistant Professor	Fall 1996-Summer 2001
The University of South Florida, Tampa	Assistant Professor	Fall 1993-Summer 1996

OTHER PROFESSIONAL EXPERIENCE: (*Name of company, position, beginning and ending dates)*

Penn State, Electrical Engineering Dept	Research Assistant	8/90 - 8/93
Penn State, Electrical Engineering Dept	Teaching Assistant	1/90 - 5/90
University of Texas at El Paso, Electrical Engineering Dept	Teaching Assistant	8/88 -12/89
Indian Space Research Organization, Trivandrum, India	Scientist/Engineer	8/84 - 8/88

CONSULTING: (*Names of companies, beginning and ending dates)*

Ceremorphic	April 2021- present
Texas Digital and Multimedia Systems	May 2008-present
EcoViv Inc.	June 2008-June 2015
SmoothStone	June 2008-June 2011

HONORS AND AWARDS:

- **Joe J. King Professional Engineering Award, Cockrell School of Engineering, UT Austin, 2023**
- **Best Paper Award, IEEE Field Programmable Custom Computing Machines (FCCM) 2022**
- **Fellow of the Association for Computing Machinery (ACM) (Class of 2020)**
- **Fellow of the National Academy of Inventors (NAI) (Class of 2020)**
- Supervisor of Student Winner of Top Achievement Award (S. Song), ECE, UT Austin, May 2020
- ELATES Fellow, Drexel University, 2019-2020
- Cullen Trust for Higher Education Endowed Professor No. 3, 2018-2022
- Supervisor of Student Reena Panda who won the Jacome Prize for Outstanding Dissertation in UT ECE, May 2018
- Graduate Fellowship for Ph. D Student S. Song 2018-2019, UT Austin
- **HPCA Hall of Fame, 2017**
- **Best Paper Award,** DAC 2016 (53rd DAC) (2 awards out of nearly 700 submissions), June 2016
- Best Paper Nominee, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2017
- Graduate Fellowship for Ph. D Student R. Panda 2017-2018, UT Austin
- **Best Paper Runner Up,** IEEE International Conference on Parallel Processing (ICPP), 2015
- **Best Paper Award**, IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), 2015
- SPEC Dissertation Award Honorable Mention, won by student Karthik Ganesan (2012)
- **ISCA Hall of Fame, 2012**
- **Best Paper Nominee**, Paper with student Karthik Ganesan, Supercomputing Conference (SC) 2011 (1 of 4 nominees), Nov 2011
- **Best Paper Nominee**, Paper with students Jeff Stuecheli and Dimitris Kaseridis, IEEE/ACM MICRO conference, 2011 (1 of 4 nominees), December 2011
- **Best paper award nominee**, (1 of 4 nominees), IEEE High Performance Computer Architecture (HPCA) 2010 (VBBI Paper)
- **IEEE MICRO TOP PICKS 2010** ''Coordinating DRAM and Last-Level-Cache Policies with the Virtual Write Queue''
- **Outstanding Engineering Alumnus of the Pennsylvania State University**, 2011

- **IEEE Fellow,** Class of 2009
- B. N. Gafford Professor in Electrical Engineering, September 2009-2018
- Graduate Fellowship for Ph. D Student 2010-2011, UT Austin
- **Best Paper Award**, IEEE International Conference on Parallel Processing (ICPP) 2009
- SPEC Benchmark workshop 2006, The K. Dixit award for best paper won by student Ajay Joshi
- TEXAS EXES Teaching Award, Feb 2004
- Engineering Foundation Faculty Award, College of Engineering, UT Austin, Fall 2001
- UT Austin Engineering Foundation Centennial Teaching Fellowship in Electrical Engineering No. 2, Sept 2000- present
- Halliburton, Brown and Root Engineering Foundation Young Faculty Award, College of Engineering, UT Austin, Fall 1999
- IBM Austin Center for Advanced Studies (CAS) or University Partnership Award- 2001-2008
- Best Paper Award, Computer Track, IEEE International Performance Conference on Computing and Communication, Feb 1999
- Elevated to Senior Membership of IEEE (Electrical and Electronics Engineers), 1997
- National Science Foundation CAREER Award, 1996-2001
- $1000 award for being Advisor of the student who won the University Level George H. Mitchell Undergraduate Student Achievement Award, April 2002 (Student Pattabi Seshadri won the $2000 award)
- Oak Ridge Junior Faculty Enhancement Award, 1996-1997
- Outstanding Young Investigator, College of Engineering, University of South Florida, 1995-1996
- Outstanding Undergraduate Teaching Award, University of South Florida, Tampa, 1994-1995.
- Best Paper Award, ASEE Gulf Southwest Conference, March 1998
- Graduate School Fellowship, awarded by the Graduate School, The Pennsylvania State University, 1991-1992
- George Krutilek Fellowship awarded by the Graduate School, The University of Texas at El Paso, 1988-1989
- Graduate School Marshal for the December 1989 commencement at The University of Texas at El Paso
- Schellenger Research Scholarship awarded by the Electrical Engineering Department, Univ. of Texas El Paso, Summer 1989
- Selected by NCERT (National Council of Educational Research and Training), New Delhi, Govt. of India, on the basis of a National Examination, for the National Talent Search Scholarship for 1977-1984
- 3rd Rank in the Kerala University B.Sc. Engineering Degree Exam, 1984
- Ist rank (Ist out of 70,462 students) in the Kerala University Pre-Degree Exam, India, 1979
- 2nd rank in the state of Kerala (2nd out of 275,554 students) in the Kerala State Higher Secondary School Exam, India, 1977

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:

- ACM, Fellow, 2020
- National Academy of Inventors (NAI), Fellow 2020
- IEEE Fellow, Class of 2009
- Senior Member, IEEE, 1997- 2008
- Member, IEEE Computer Society, 1989-present

- Member, ACM (Association of Computing Machinery), ACM - SIGARCH, since 1990
- Member ACM SIGMICRO since 2001
- Member Eta Kappa Nu (Class of 1989), Tau Beta Pi (Class of 1989), Phi Kappa Phi (Class of 1992)

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES:

- **Editor-In-Chief,** IEEE MICRO, 2019-2023
- **Executive Committee member, IEEE Technical Committee on Computer Architecture (TCCA), 2019 - 2022**
- **Editorial Board,** Associative Editor, IEEE MICRO, 2005 - 2018
- **Associate Editor**, IEEE Computer Architecture Letters, 2016 – 2018
- **Associate Editor**, IEEE Transactions on Computers, 2009 – 2014
- **Associate Editor**, IEEE Transactions on Sustainable Computing, 2016-2019
- **Associate Editor**, ACM Transactions on Architecture and Code Optimization (TACO), 2016-2018
- **Associate Editor,** IEEE Transactions on VLSI, 2003 December-August 2007
- **Editorial Board**, International Journal on Embedded Systems, 2005-2014
- **Member**, National Science Foundation Workshop on Computer Performance Evaluation Techniques, December 2001, Austin TX
- **Member**, National Science Foundation Proposal Review Panel, 2017, 2000, 1998, 1997
- **Member,** DOE Office of Science Proposal Review Panel, May 2010, 2014

EXTERNAL ACADEMIC REVIEW BOARDS:

- Member, Industrial and Professional Advisory Council (IPAC), Penn State College of Engineering, 2008-2016
- Member, External Advisory Board, ECE Department, UT El Paso, 2008-2012
- Member, External Advisory Board, University of North Texas (UNT), 2008-2012
- External Reviewer for Ph. D Program, Rochester Institute of Technology 2013

UNIVERSITY COMMITTEE ASSIGNMENTS:

University-	**Information Technology Committee Chair**	**2019-2020**
	Member, Faculty Council	2020-2022
	Member, Financial Aid Committee	2020-2021
	Member, Graduate Assembly	2019-2022
	Information Technology Committee Vice Chair & Chair Elect	2018-2019
	Information Technology Committee	2017-2018
	Information Technology Committee	2016-2017
	University Financial Aid Committee co-chair	2012-2013
	University Financial Aid Committee Member	2011-2012
	Circuit Design Master's Program Minority Liaison	2007 -
	Circuit Design Master's Program Minority Liaison	2006
	Circuit Design Master Program Minority Liaison	2005
College-	Cockrell School of Engineering Honors Committee Member	2014-2015
	Cockrell School of Engineering, Honors Committee Chair	**2010-2014**
	College of Engineering Honors Committee, Member	2005-2008
	College of Engineering Hocott Awards Committee	2006, 2007, 2008
	College of Engineering Equal Opportunity in Engineering Committee	2005-08
	College of Engineering Honors Committee	2004-05
	College of Engineering Equal Opportunity in Engineering Committee	2004-05
	College of Engineering Honors Committee	2003-04
	College of Engineering Equal Opportunity in Engineering Committee	2003-04
	College of Engineering Honors Students Committee	2002-03

Departmental-	ECE Senior Faculty Recruiting Committee co-Chair	2019-2020
	ECE Junior Faculty Recruiting Committee (Chair: Jeff/Dimakis)	2018-2019
	ECE Faculty Evaluation Committee (Chair: Julien)	2018-2019
	ECE Faculty Evaluation Committee	2017-2018
	Senior Faculty Search Committee (Chair: Shakkottai)	2017-2018
	ACSES Track Ph. D Coordinator	2013-2018
	ECE Faculty Evaluation Committee	2016-2017
	Faculty Search Committee (Chair Ed Yu)	2016-2017
	Faculty Search Committee (Chair Ed Yu)	2015-2016
	ECE Faculty Evaluation Committee	2014-2015
	ECE Faculty Evaluation Committee	2013-2014
	ECE Faculty Evaluation Committee	2012-2013
	Faculty Search Committee (Chair Ed Yu)	2012-2013
	ECE Faculty Evaluation Committee	2012-2013
	ECE Faculty Expectations Committee	2012-2013
	Computer Engineering Ph. D Coordinator	2011-2012
	Computer Architecture and Embedded Processing Track Ph. D Coordinator	2011-2012
	Faculty Search Committee (Chair de Veciana)	2010-2011
	Faculty Search Committee (Chair Al Bovik)	2011-2012
	Computer Architecture and Embedded Processing Track Ph. D Coordinator	2011-2012
	Computer Engineering Ph. D Coordinator	2010-2011
	Computer Engineering Ph. D Coordinator	2011
	ECE Faculty Evaluation Committee	2011-2012
	ECE Faculty Expectations Committee	2009-2010
	Computer Engineering Ph. D Coordinator	2008-2009
	Computer Engineering Ph. D Coordinator	2007-2008
	Computer Engineering Ph. D Coordinator Curriculum Reform Subcommittee	2008
	ECE ABET Committee	2003-2007
	ECE Appeals Committee	1999-2003
	ECE Awards Committee	2001-04
	ECE Hiring Subcommittee, Computer Architecture Position	2001-06
	Department of ECE, Appeals Committee	April 2000-Mar 2001, April 2001-March 2002
	Department of ECE, Computer Engineering Faculty Committee	September 1996-present
	Department of ECE Subcommittee on Computer Engineering Graduate Admissions	1997-2006
	Department of ECE, Graduate Studies Committee,	September 1996-present
	Department of ECE, Undergraduate Software Curriculum Committee	Sept 1996-2001
	Department of ECE, Undergraduate Digital Systems Curriculum Committee	Sept 1996-2001

PROFESSIONAL ACTIVITIES:

- Editor In Chief, IEEE MICRO, 2019-now
- Editor In Chief Selection Committee, ACM Transactions on Architecture and Code Optimization (TACO) 2020
- Member, HIPEAC (High Performance and Embedded Architecture and Compilation), European Union, 2016-present
- SPEC Dissertation Award Committee Chair, 2016
- IEEE Fellows Selection Committee (Computer Society), 2018
- IEEE Fellows Selection Committee (Computer Society), 2017
- IEEE Fellows Selection Committee (Computer Society), 2015
- IEEE Fellows Selection Committee (Computer Society), 2013
- DOE Proposal Reviewer, 2022
- DOE Panelist, 2014
- NSF Panelist, 1997, 2013, 2017, 2022
- Steering Committee Member, SPEC RESEARCH, 2013-2014
- Steering Committee Member, SPEC RESEARCH, 2012-2013
- Steering Committee Member, SPEC RESEARCH, 2011-2012
- Steering Committee Member, SPEC RESEARCH, June 2010-2011
- Search Committee Member, ACM Transactions on Architecture and Code Optimization (TACO) Editor in Chief Search, 2008-2009

OTHER COMMITTEES/POSITIONS:

- MODSIM Organizing Committee, 2022, 2023
- HPCA Test of Time Award, 2022, 2023,
- ISCA 50th Anniversary Committee, ISCA 2023
- Special Issue Editor, Microprocessor at 50, IEEE Micro, 2021
- Guest Editor, IEEE MICRO Special Issue on Computing with Memristors. Co-guest edited with Dr. Swartzlander. Sep/October 2018.
- Member, IEEE Senior Member Selection Panel, October 2007
- ACM SIGMICRO Vice Chair, 2006-2008
- ACM SIGMICRO Member at large, 2005-2008
- Steering Committee, SPEC workshops, 2005-date
- Steering Committee, IISWC, 2005-present
- Steering Committee, ISPASS, 2000-present
- ACM SIGMICRO Public Relations Director 2002-03, 2001-02
- Travel Awards Chair, IEEE International Symposium on Parallel Architectures and Compilation techniques (PACT 2003)

- Tutorials/Workshop Chair, IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS, March 2003
- 2000 IEEE International Conference on Computer Design, Special Sessions Chair
- Finance Chair, IEEE Workshop on Workload Characterization, 1998-2004
- Finance Chair, IEEE International Performance Conference on Computing and Communication, (IPCCC 2000)
- Panel Chair, IEEE International Performance Conference on Computing and Communication, Feb 1999
- Registration Chair - IEEE International Symposium on Microarchitecture, MICRO-31, Dallas, TX, Dec 1998

OTHER WORKSHOPS ORGANIZED:

1. 1st Workshop on Integrating Design and Design Automation into Undergraduate Computer Science and Engineering Curriculum.
   For: University Faculty from around the country.
   Partially funded by: The National Science Foundation
   August 5-8, 1996 Tampa, Florida, 33620.

2. 2nd Workshop on Integrating Design and Design Automation into Undergraduate Computer Science and Engineering Curriculum.
   Partially funded by: National Science Foundation
   August 4-7, 1997 Tampa, Florida, 33620.

WORKSHOP SESSIONS/SEMINARS/TUTORIALS ORGANIZED:

1. Workshop Session on High Performance Processors organized at: Workshop title: IEEE Computer Society 1996 Annual Workshop on VLSI
   Held: Nov. 3-6, 1996
   Location: Clearwater, Florida

2. Half-day Tutorial Presentation:
   At the Workshop of Microelectronic Systems Education, July 1997, Arlington, Virginia. Tutorial Topic: Rapid Prototyping using FPGAs, July 23, 1997

3. Half-day Seminar presented:
   In the AUSTIN INNOVATION SERIES, Aug 27, 1997 at IBM, Austin
   Topic: Improving the Memory Access Performance of Programs

STEERING COMMITTEE CHAIR

- IISWC (IEEE International Symposium on Workload Characterization), 2005-2007
- ISPASS (IEEE International Symposium on Performance of Software and Systems), 2008-2013

STEERING COMMITTEE MEMBER

- ISCA (ACM International Symposium on Computer Architecture) Steering Committee Member, 2021-2022
- IEEE TCCA (Technical Committee on Computer Architecture) Executive Committee Member, 2019-2022
- IISWC (IEEE International Symposium on Workload Characterization), 2007-present
- ISPASS (IEEE International Symposium on Performance of Software and Systems), 2001-present
- WWC (Since inception 1998 till it became IISWC 2006)

GENERAL CHAIR

- ACM International Conference on Performance Engineering (ICPE) 2015
- IEEE International Symposium on Workload Characterization (IISWC) 2005
- IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 05
- IEEE Intl Workshop on Workload Characterization (WWC), 1998-2005

PROGRAM CHAIR

- HiPEAC 2023 Program Chair
- International Symposium on Computer Architecture (ISCA) 2021
- International Conference on Parallel Processing (ICPP) 2020 Program Co-Chair
- International Conference on Parallel Processing (ICPP) 2013 Performance Track Chair
- International Workshop on Performance Analysis of Workload Optimized Systems (FastPath) 2014
- International Workshop on Performance Analysis of Workload Optimized Systems, FastPath 2013
- ACM International Conference on Performance Engineering (ICPE) 2012 Program co-Chair
- SPEC Workshop 2006, Program co-chair
- ISPASS 2004 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)
- ICCD 1999 Architecture Track Program co-chair IEEE International Conference on Computer Design (ICCD)
- ISPASS 2000 Workload Characterization Track IEEE International Symposium on Performance of Software and Systems (ISPASS)
- WWC (Workshop on Workload Characterization), 1998-2004
- ODES 2003-2005 (Optimizations for DSP and Embedded Systems Workshop), (held in conjunction with the CGO symposium) (co-chair)

PROGRAM COMMITTEE MEMBER

1. ACM Architectural Support for Programming Languages and Operating Systems (ASPLOS) Conference 2023

2. IEEE High Performance Computer Architecture (HPCA) Symposium 2024
3. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2023
4. International Symposium on FPGA, ISFPGA 2023
5. CloudMICRO 2021
6. ACM International Symposium on Field Programmable Gate Arrays FPGA 2022
7. ACM International Symposium on Field Programmable Gate Arrays (FPGA) 2021
8. ACM Architectural Support for Programming Languages and Operating Systems (ASPLOS) Conference 2021
9. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2020
10. IEEE High Performance Computer Architecture Symposium (HPCA) 2020
11. ACM International Symposium on on Field Programmable Gate Arrays (FPGA) 2020
12. IEEE International Symposium on Workload Characterization (IISWC) 2019
13. IEEE International Conference on Microarchitecture (MICRO 2019)
14. IEEE High Performance Computer Architecture Symposium (HPCA) 2019
15. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2019
16. IEEE High Performance Computer Architecture Symposium (HPCA) 2018
17. IEEE International Symposium on Workload Characterization (IISWC) 2018
18. IEEE International Parallel and Distributed Symposium (IPDPS) 2018
19. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2017
20. IEEE High Performance Computer Architecture Symposium (HPCA) 2017
21. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2017
22. IEEE International Parallel and Distributed Symposium (IPDPS) 2017
23. ACM International Conference on Performance Engineering ICPE 2016
24. IEEE Workshop on Emerging Parallel and Distributed Runtime Systems and Middleware (IPDRM), 2016
25. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2015
26. ACM Supercomputing, SC'15, Performance Track, 2015
27. International Workshop on High-Performance Big Data Computing (HPBDC) 2015
28. IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing, (CCGrid) 2014
29. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2012
30. IEEE High Performance Computer Architecture (HPCA) Symposium 2012
31. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2012
32. Network and Parallel Computing (NPC) 2011
33. Supercomputing 2011 (Performance track)
34. ICS (International Conference on Supercomputing), 2011
35. IEEE Conference on Parallel Architectures and Compilation techniques (PACT) 2010
36. SPEC WOSP/SIPEW 2010
37. IEEE MICRO TOP PICKS 2009
38. IEEE International Conference on Computer Design (ICCD) 2009
39. SPEC Workshop 2009
40. Virtual Execution Environments (VEE) 2008
41. IEEE Parallel Architectures and Compilation techniques (PACT) 2009
42. IEEE International Parallel and Distributed Processing Symposium, 2009
43. SPEC Workshop 2008
44. IEEE International Conference on Computer Design (ICCD) 2008

45. 2007 Supercomputing Conference, Performance Track
46. IEEE MICRO TOP PICKS 2006
47. IEEE Symp on High Performance Computer Architecture (HPCA 2005)
48. IEEE-Symp on High Performance Computer Architecture (HPCA 2002)
49. Parallel Architectures and Compilation techniques (PACT 2003)
50. IEEE-International Symposium on Microarchitecture (MICRO-33), 2000
51. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2001)
52. IEEE International Performance Conference on Computing and Communication (IPCCC 2000)
53. IEEE International Conference on Computer Design, Architecture Track (ICCD 1999)
54. IEEE International Performance Conference on Computing and Communication (IPCCC 1999)
55. 1998 IEEE International Conference on Computer Design (ICCD), Architecture Track
56. International Performance and Dependability Symposium (IPDS), held along with DSN 2002
57. North Atlantic Test Symposium, 1997
58. Workshop on Workload Characterization (1998-2004)
59. MoBS workshop 2005 (held with ISCA)
60. Value Prediction Workshop, 2004
61. MRE 2004 (Managed RunTime Environment), 2003 (held with CGO)
62. INTERACT-6, Workshop on Interaction between Architectures and Compilers, in conjunction with IEEE-International Symposium on High Performance Computer Architecture (HPCA-8), 2002
63. Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design 2001)
64. Workshop on Decoupled Access Execute Architectures (MEDEA) in conjunction with PACT2001
65. Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design ICCD 2000)
66. Workshop on Decoupled Access Execute Architectures (in conjunction with PACT 2000)
67. Workshop on Media Processors and Digital Signal Processors, Nov 1999 (in conjunction with 32nd IEEE International Symposium on Microarchitecture Micro-32)
68. Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design 1999)

EXTERNAL REVIEW COMMITTEE (ERC) MEMBER

1. ACM/IEEE International Symposium on Computer Architecture (ISCA) 2019
2. ACM International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2017
3. IEEE High Performance Computer Architecture Symposium, HPCA 2017
4. ACM/IEEE International Symposium on Microarchitecture (Micro) 2016
5. IEEE High Performance Computer Architecture Symposium, HPCA 2016
6. ACM/IEEE International Symposium on Microarchitecture (Micro) 2015
7. IEEE High Performance Computer Architecture Symposium, HPCA 2015

TECHNICAL REVIEWER:

(Technical reviewer for several journals, conferences, and workshops, various years, including but not limited to)

HPCA, ISCA, ASPLOS, MICRO, IEEE Micro Top Picks
ACM TACO
ACM TOMACS
IEEE Transactions on Computers
IEEE Transactions on Parallel and Distributed Systems
The Computer Journal
The Journal of VLSI
Microprocessors and Microsystems
IEE Journal of Computers and Digital Techniques
IEEE Computer
IEEE Micro Magazine
IEEE Concurrency
IEEE/ACM International Symposium on Computer Architecture (ISCA)
IEEE Intl High Performance Computer Architecture Symposium (HPCA)
IEEE International Symposium on Microarchitecture (MICRO)
PACT (Parallel Architectures and Compilation Techniques) Conf., 2001
IEEE Workshop on Hardware Support for Objects and Microarchitectures for Java (in conjunction with IEEE International Conference on Computer Design)
IEEE International Performance Conference on Computing and Communication 1999, 2000
IEEE Workshop on Workload Characterization
Workshop on Media Processors and Digital Signal Processors, Nov 1999 (in conjunction with IEEE Micro-32)
IEEE International Conference on Computer Design (ICCD) 1998, 1999
North Atlantic Test Symposium 1997
Reviewer for McGraw Hill 2001-2002
Reviewer for McGraw Hill, 2000
Reviewer for Prentice Hall USA (1995), Prentice Hall UK (1999)
Reviewer for Addison Wesley (1997)
Kluwer Academic Publishers Book Proposal Reviewer, 2001
Reviewer for IEEE Computer's Special Issue on Billion Transistor Processors, 1997
Member, Focus Group on IEEE Spectrum and its Web Site, Tammadge Market Research Group, May 1998

OTHER ACTIVITIES:

1. Robotics Club, West Lake High School, Eanes ISD, Team Mentor, 2016-2017
2. **Technology Club Founder and Organizer**: St. Ignatius Martyr School, Austin, TX, 2012-2013
3. **Elementary School PSIA Math Coach, 2012**
4. **Elementary School PSIA Spelling Coach, 2011**
5. **Elementary School PSIA Spelling Coach, 2010**
6. **Judge**: Texas High School State Science and Engineering Fair, April 2001
7. **Judge:** Florida High School Science Fair, 1994

PUBLICATIONS:

- Approximately 300 Publications
- 24 IEEE Transactions, 5 ACM Transactions
- 9 ISCA Papers (Member ISCA Hall of Fame, Class of 2012)
- 9 HPCA Papers (Member HPCA Hall of Fame, Class of 2017)
- 7 MICRO Papers
- H-index: 57 (29 since 2018)
- I-10 index: 189 (92 since 2018)
- 11430+ Citations (3355 since 2018)
- 3 co-authored undergraduate Textbooks
- 4 Edited Books
- 16 Book Chapters
- 16 US Patents

Refereed Archival Journal Publications

1. Fernando Mosquera, Krishna Kavi, Gayatri Mehta, Lizy John, Guard Cache: Creating Noisy Side Channels, IEEE Computer Architecture Letters (CAL), 2023

2. Luis Armando Quintanilla Villon, Zachary Susskind, Alan T. L. Bacellar, Igor Dantas Dos Santos Miranda, Leandro Santiago de Araujo, Priscila Machado Vieira Lima, Mauricio Breternitz Jr., Lizy K. John, Felipe Maia Galvao Franca, and Diego Leonel Cadette Dutra, A conditional branch predictor based on weightless neural networks", Neurocomputing, July 2023

3. Aman Arora, Tanmay Anand, Aatman Borda, Rishabh Sehgal, Bagus Hanindhito, Pierre Emmanuel Gaillardon, Jaydeep Kulkarni and Lizy John, CoMeFa: Deploying Compute-in-Memory on FPGAs for Deep Learning Acceleration, ACM Transactions on Reconfigurable Systems (TRETS), 2023 (Accepted)

4. Aman Arora, Andrew Boutros, Daniel Raucj, Aishwarya Rajen, Aatman Borda, Seyed Alireza Damghani, Samidh Mehta, Sangram Kate, Pragnesh Patel, Kenneth B. Kent, Vaughn Betz, and Lizy K. John, "Koios 2.0: Open-Source Deep Learning Benchmarks for FPGA Architecture and CAD Research" Accepted for publication in the Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023

5. Aman Arora, Moinak Ghosh, Samidh Mehta, Vaughn Betz, and Lizy K. John, Tensor Slices: FPGA Building Blocks for the Deep Learning Era, ACM Transactions on Reconfigurable Systems (TRETS), Vol. 15, No. 4, December 2022, *doi = {10.1145/3529650}*

6. Rahul Mathur, Jaydeep Kulkarni, Lizy K. John, Thermal-Aware Design Space Exploration of 3D Systolic ML Accelerators, IEEE Journal of Exploratory Solid-State Computational Devices and Circuits, 2021

7. Mochamad Asri, Dhairya Malhotra, Jiajun Wang, George Biros, Lizy K. John and Andreas Gerstlauer, Hardware Accelerator Integration Tradeoffs for High Performance Computing: A

Case Study of GEMM Acceleration in N-Body Methods, IEEE Transactions on Parallel and Distributed Systems (TPDS), August 2021, pp. 2035-2048.

8. Shuang Song, Xu Liu, Qinzhe Wu, Andreas Gerstlauer, Tao Li, and Lizy K. John, “State Late or Finish Early: A Distributed Graph Processing System with Redundancy Reduction”, Proceedings of the VLDB Endowments (PVLDB). 2018

9. Muhammad Faisal Iqbal, Muhammad Zahid, Durdana Habib, and Lizy Kurian John, Efficient Prediction of Network Traffic for Real-Time Applications Journal of Computer Networks and Communications, Volume 2019, Article ID 4067135, 11 pages, https://doi.org/10.1155/2019/4067135

10. J. Wang and Lizy K. John, SelSMAP: A Selective Stride-Masking Prefetching Scheme for Cloud and Big Data Applications, **ACM Transactions** on Architecture and Code Optimization (TACO), 2019, http://doi.acm.org/10.1145/3274650

11. Han, Rui, Lizy Kurian John, and Jianfeng Zhan. "Benchmarking Big Data Systems: A Review." IEEE Transactions on Services Computing, May/June 2018, Vol. 11, Issue 3, pp. 580-597, ISSN: 1939/1374, DOI: 10.1109/TSC.2017.2730882

12. Xinnian Zheng; Lizy K. John; Andreas M Gerstlauer , "LACross: Learning-based Fine-grained Analytical Cross-Platform Performance and Power Prediction", International Journal of Parallel Programming (IJPP), preprint Jan 2017

13. Zhuoran Zhao, Andreas Gerstlauer, Lizy K. John, "Source-Level Performance, Energy, Reliability, Power and Thermal (PERPT) Simulation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 2, pp. 299-312, Feb 2017

14. Faisal Iqbal and Lizy K. John, Dynamic Core Allocation and Packet Scheduling in Multi Core Network Processors”, IEEE Transactions on Computers, 2016

15. Zhibin Yu, Lieven Eeckhout, Tao Li, Lizy K. John, , “GPGPU-MiniBench: Accelerating GPGPU Micro-Architecture Simulation”, IEEE Transactions on Computers, 2015, Vol. 64, Issue 11, pp. 3153-3166

16. Arun Nair, Stijn Eyerman, Jian Chen, Lizy John, Lieven Eeckhout, “Mechanistic Modeling of Architectural Vulnerability Factor”, **ACM Transactions on Computer Systems**, 2015, Vol. 32, Issue 4

17. Youngtaek Kim, Sanjay Pant, Srilatha Manne, Michael Schulte, Lloyd Bircher, Madhu Saravana Sibi Govindan, and Lizy K. John, “Automating Stressmark Generation for testing Processor Voltage Fluctuations”, **IEEE Micro**, July/August, pp. 66-75, 2013

18. Karthik Ganesan and Lizy K. John, Automatic Generation of Miniaturized Synthetic Proxies for Target Applications to Efficiently Design Multicore Processors, **IEEE Transactions on Computers**, Vol. 63, No. 4, pp. 833-846, April 2014

19. Jian Chen, Arun Nair, and Lizy K. John, Predictive Heterogeneity-Aware Application Scheduling for Chip Multiprocessors, **IEEE Transactions on Computers**, Vol. 63, No.2, pp. 435-447, February 2014.

20. Dimitris Kaseridis, Muhammad Faisal Iqbal, and Lizy K. John, Cache Friendliness Aware Management of Last-level Caches for High Performance Multi-Core Systems, **IEEE Transactions on Computers**, Vol. 63, No. 4, pp. 874-887, April 2014.

21. Lloyd Bircher and Lizy K. John, Complete System Power Estimation using Processor Performance Events, **IEEE Transactions on Computers**, Vol. 61, No. 4, pp. 563-577, April 2012

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E. ORAL PRESENTATIONS:

Keynote Speeches/Panels:

1. Panelist, "Reflecting on 50 Years of Computing Research, and Future Outlook", ACM FCRC, Plenary Panel, June 20, 2023, Orlando, Florida (ACM FCRC's First Ever Plenary Panel)
2. **Keynote Speech,** Predicting Performance of Data Centers at Scale, **Confluence 2022**
3. **Keynote Speech, The 17th International System-on-Chip (SoC) Conference, October 2019** Machine Learning for Power Modeling and Prediction
4. **Keynote Speech**, IEEE Women In Engineering International Leadership Summit (WIE ILS), Kochi, India, Sept 8, 2018
5. **Keynote Speech**, IEEE Min-Move Workshop held with IEEE Parallel Architectures and Compilation Conference (PACT), Computing In-Situ and In-Transit, Sept 2017
6. **Keynote Speech**, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) Conference, Machine Learning for Performance and Power Modeling/Prediction, April 2017, San Francisco, California
7. **Samsung** Technical Forum Plenary Speech, "Machine Learning for Power Modeling and Prediction", Austin, Texas, October 8, 2015
8. **Keynote Speech, Many Big, Many Little: Who will crunch all the Big Data?, Huawei Strategic Workshop, May 19, 2015, Shenzhen, China.**
9. **Keynote Speech**, Big Data and Cloud Workloads: An Architect's Perspective, BPOE Workshop in conjunction with ACM ASPLOS, Salt Lake City, Utah, 2014
10. **Invited Speech**, Performance Evaluation for Large Scale Systems: Closed Loop Control with Appropriate Metrics, ACM Supercomputing Conference (SC 2013), Nov 2013 (Host: Bill Kramer, UIUC)
11. **Keynote Speech**, ACM International Conference on Performance Engineering (ICPE), March 14, 2011, Karlsruhe, Germany
12. **Keynote Speech**, "Performance Evaluation and Benchmarking: The Return of Synthetic Benchmarks", IBM Center for Advanced Studies (CAS) Conference, Feb 22, 2008
13. **Keynote speech,** "Workload Characterization: Can it save Computer Architecture and Performance Evaluation", Workshop on Commercial Workload Characterization, Madrid, Spain, Feb 15, 2004.

Other Talks:

1. Invited talk, Hardware for ML and ML for Hardware Design, Ghent University, Belgium, June 2, 2023
2. Invited Talk, Energy-efficient Architectures for Machine Learning, University of Seville, Spain, May 30, 2023
3. Invited talk, Hardware for ML and ML for Hardware Design, University of Porto, Portugal, May 25, 2023

4. Invited talk, Hardware for ML and ML for Hardware Design, University of Coimbra, Portugal, May 24, 2023
5. Invited talk, Hardware for ML and ML for Hardware Design, ISCTE University Institute of Lisbon, Portugal, May 23, 2023
6. Invited talk, Hardware for ML and ML for Hardware Design, University of Lisbon, Portugal, May 23, 2023
7. Invited talk, Hardware for ML and ML for Hardware Design, ETH Zurich, May 12, 2023
8. Panelist, United States Patents and Trademarks Office, March 29, 2023
9. Panelist, IMAGINE Consortium, Enabling Intelligence in the Edge to Cloud Continuum: Challenges and Next Steps, March 2, 2023
10. Panelist, Rising Stars, UT Austin, October 28, 2022.
11. Tech Talk, AMD, Miniaturized Proxies of Industry Standard Benchmarks for Pre-silicon Evaluation, Sep 8, 2022.
12. OSFPGA Foundation Webinar, FPGAs for ML and ML for FPGAs, Aug 17, 2022
13. Basser Seminar, University of Sydney, July 28, 2022, "Systems for ML and ML for Systems"
14. IMAGINE kickoff, Cloud Thrust in IMAGINE, March 25, 2022
15. Machine Learning for Performance and Power Modeling/Prediction, MLSys at UT, 24 March 2022
16. Seminar, Machine Learning for Performance Evaluation and Prediction, Stanford Robust Group, October 25, 2021
17. Invited Talk, Predicting Performance of Data Centers at Scale, Cloud@MICRO Workshop, Oct 18, 2021
18. Invited Speaker, College of Engineering Trivandrum, "Machine Learning: The Hype and the Reality", Sep 5, 2021
19. **Panelist, Panel on Energy Efficiency at Cloud Scale AI**, Workshop on Energy Efficient Machine Learning and Cognitive Computing (EMC2), Aug 2, 2021
20. Panelist, MLSys Workshop: Benchmarking Machine Learning Workloads on Emerging Hardware, April 9, 2021
21. "Women in STEM: Challenges, Strategies, Role Models", Women in STEM Workshop, Cockrell School CARES Speaker, UT Austin, April 8, 2021
22. Invited Lecture, "When Caches Start Computing: How Should you Design your Algorithms?", SIAM Conference on Computational Science and Engineering, March 1, 2021
23. Data Center Benchmarking, Facebook, October 2020
24. Invited Speech, Google, Machine Learning for Performance and Power Modeling/Prediction, Sept 1, 2020

25. Invited Talk, Machine Learning for Performance and Power Modeling/Prediction", Saint Gits College of Engineering, India, Jan 10, 2020
26. Presentation, "How to enter and succeed in Graduate School", Saint Gits College of Engineering, India, January 10, 2020
27. Invited Talk, Demystifying Infrastructure Choices for Machine Learning", Providence College of Engineering, India, April 5, 2019
28. A Study of Core Utilization and Residency in Heterogeneous Smart Phone Architectures", P ACM/SPEC International Conference on Performance Engineering, April 2019, Mumbai, India.
29. Invited talk, Hot Regions in Hot Workloads, IEEE IISWC, Raleigh, North Carolina, Nov 1, 2018
30. Invited talk, Approximate Techniques for Performance and Power Modeling/Prediction MODSIM 2018, Washington, Seattle, Aug 16, 2018
31. Panelist, "Modeling and Simulation for Extreme Heterogeneity", MODSIM 2018, Seattle, Aug 17, 2018.
32. Seminar, Approximate Techniques for Performance and Power Modeling/Prediction, MIT, May 29, 2018
33. Computer Science Colloquium, Approximate Techniques for Performance and Power Modeling/Prediction, William and Mary University, Virginia, Apr 20, 2018
34. **Invited Speech, Industry-Academia Partnership**, UT Cloud Workshop, Computing In Situ and In Transit, Nov 10, 2017
35. Invited Speech, IEEE SPICES 2017, Machine Learning for Performance and Power Modeling/Prediction, Aug 10, 2017
36. Adaptive Energy-Efficient Designs for Next Generation Smart Phone CPUs, Samsung Austin Research Center, Feb 3, 2017
37. Computer Architecture, Memory Systems, Performance and Power Optimizations, Speech to USPTO Visitors, April 2017
38. Seminar, "Machine Learning for Power Modeling and Prediction", Polytecnico Milan, July 8, 2016
39. Colloquia, "Machine Learning for Performance and Power Modeling", Indian Institute of Science, January 9, 2016
40. Invited Talk, "Workload Characterization for Big Data Computing", Intel, Bangalore, January 9, 2016
41. Invited Talk, ARM, "Machine Learning for Performance and Power Modeling", Bangalore, January 7, 2016
42. Invited Talk, IBM Watson Research Center, Yorktown Heights, New York, "Big Data Workloads, An Architect's perspective ", Invited by: Michael Healy, Sep 14, 2015
43. Invited Talk, "Big Data Workloads, A Computer Architect's perspective", AMD, Austin, Texas, April 6, 2015

44. Invited Talk, Computer Science Department Colloquium, “Big Data Workloads, A Computer Architect’s perspective” Baylor University, May 1, 2015
45. Invited Speech, “Workload Characterization for Big Data Computing”, Shannon Lab, Huawei, May 21, 2015.
46. Huawei, China, Cloud and Big Data Workload Characterization: Challenges and Opportunities, June 23, 2014.
47. Shenzhen Institute of Advanced technology, Chinese Academy of Sciences, Shenzhen, Cloud and Big Data Workload Characterization: Challenges and Opportunities, June 24, 2014
48. Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, Shenzhen, Multicore System Design and Optimization, June 25, 2014.
49. Chinese Academy of Sciences, Beijing, June 27, 2014, Multicore System Design and Optimization
50. SRC India Design Review, Bangalore India, Jan 10, 2014
51. “Multicore System Design and Optimization”, Talk given to UT graduate Students, Sept 27, 2013
52. SRC Annual review Presentation, Portland Oregon, May 3, 2013
53. Georgia Tech, Performance Verification for Complex Chips: Role of Workload Proxies, April 2012
54. Presentation to Lockheed Martin, Hardware Software Co-design for Proprietary Systems, March 27, 2012
55. Texas A&M Seminar, Multicore System Design and Optimization: November 2011
56. Workload Synthesis for a Communications SoC, Invited talk at the Workshop on SoC Architectures, Accelerators and Workloads (SAW) organized by Ravi Iyer (Intel) in conjunction with HPCA, February 12, 2011, San Antonio
57. SRC Annual Review Presentation, March 2011
58. Lawrence Livermore National Lab, Jan 11, 2011
59. Talk at Freescale Meeting, December 2010
60. “Multicore System Design and Optimization”, UT Day at AMD, Aug 20, 2010
61. “Synthetic Benchmark Generation Framework for System Level Max Power Virus Generation and Performance Cloning”, SRC Annual Review Presentation, CMU, April 27, 2010 “
62. “Why consider graduate School”, Presentation to Honors Students and their parents, April 22, 2010
63. “LCA Research in Computer Architecture, Performance Evaluation and Workload Characterization”, April 7, 2010, Presented at AMD Day at UT,
64. “Automatic Benchmark Synthesis: The Return of Synthetic Benchmarks”, Colloquium, Computer Science Department, University of Pittsburg, April 26, 2010
65. Automatic Benchmark Synthesis for Validation of Performance and Power Modeling of High Performance Processors, Computer Science and Engineering Department Colloquium Penn State, March 2010.
66. SRC Annual Review, Stanford, CA, March 2009

67. “Effective Computer System Design using Workload Characterization”, Texas A & M University Computer Science Seminar, November 3, 2008
68. Tech Area Night Presentation, Embedded Systems Area, April 2008, ECE Department
69. “Chip Design”, Camp Texas, Incoming Student Camp, UT Austin, Aug 21, 2008
70. “Workload Characterization for Effective Computer System Design”, Computer Science Colloquium, The University of Texas at El Paso, Apr 18, 2008
71. “Graduate School: How to Enter and Succeed”, Talk given to IEEE Meeting, The University of Texas at El Paso, Apr 18, 2008.
72. LCA Research in Computer Architecture, Performance Evaluation and Workload Characterization, Talk given to Sun Microsystems Open Sparc Initiative, January 29, 2008
73. Performance Evaluation and Benchmarking, Talk given at UT@IBM: Building Collaboration, Creating Impact, Nov 5, 2007
74. LCA Research in Computer Architecture, Performance Evaluation and Workload Characterization, Aug 28, 2007, Computer Architecture Industry Affiliates
75. Computer System Design and Technology, Camp Texas, Aug 20, 2007
76. CRA-W/CDC Programming Languages Summer School, CS Department, UT Austin, “What Programming Language Researchers should know about Computer Architecture”, May 11, 2007
77. CRA-W/CDC Computer Architecture Summer Workshop, How to get started in Computer Architecture Research, Princeton, July 19 2006
78. SPEC Annual Meeting, “Use of Clustering in Benchmark Selection”, Sunnyvale, CA, Jan 2005.
79. Hewlett Packard, “Workload Characterization for Computer System Design and Evaluation”, June 15, 2004
80. University of Texas MITE Program “Electrical and Computer Engineering”, June 7 2004
81. Lizy John, “Panelist at ISPASS Panel”, Austin, TX, April 2004.
82. The University of Texas at Austin, ECE Department Graduate Student Orientation, “Life in Graduate School”, Aug 2003
83. The University of Texas at Austin, College of Engineering Honors Program, “Workload Characterization for Computer System Design”, Sept 14, 2002
84. The University of Texas at Austin, ECE Department Graduate Student Orientation, “Areas in Computer Engineering”, Aug 2001
85. The University of Texas at Austin, Women in Engineering Program, “Designing with Field Programmable Gate Arrays”, July 26, 2001
86. The University of Texas at Austin Honors Colloquium, “Design of Microprocessors”, July 27, 2001.
87. The International Conference on Supercomputing (ICS) 2001, “Improving Java Performance using Hardware Translation”, Italy, June 2001.
88. Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, “Evaluation of TPC-H benchmark on Athlon based systems”, Monterrey, Mexico, Jan 21st, 2001.

89. Fourth Workshop on Computer Architecture Evaluation using Commercial Workloads, “Performance Impact of Multithreaded Java Server Applications”, Monterrey, Mexico, Jan 21st, 2001.
90. The 5th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-5), “Is Compiling for Performance == Compiling for Power?” Monterrey, Mexico, Jan 20, 2001.
91. IEEE Workshop on Hardware Support for Objects and Microarchitectures for Java, Invited Talk, “Understanding, Exploiting and Improving Java Run Time Systems”, Sept 17, 2000.
92. Tivoli Corporation, Austin, “Characterizing, Understanding and Exploiting E-business workloads”, Aug 21, 2000.
93. The University of Texas at Austin Honors Colloquium, “Design of Microprocessors”, July 22, 2000.
94. IBM Center for Advanced Studies (CAS) Conference, IBM Austin, “Effectiveness of Out of Order Scheduling on Three Generations of IBM PowerPC Processors”, July 19, 2000.
95. Singapore National University, “Architectural Support for Java Run Time Systems”, Seminar in the Computer Science Department and Parallel Processing Laboratory, June 14, 2000
96. Nanyang Technological University, Singapore, “Architectural Support for Java Run Time Systems”, Seminar in the Electrical Engineering Department, June 13, 2000.
97. Intel, Austin, “Architectural Support for Java Run Time Systems”, Seminar at the Intel Texas Design Center, May 10, 2000.
98. University of Illinois, Urbana Champaign, “Understanding, Exploiting and Improving Java Run Time Systems”, Electrical and Computer Engineering Seminar, May 1, 2000.
99. The Pennsylvania State University, Computer Science and Engineering Department Colloquium, “Understanding, Exploiting and Improving Java Run Time Systems”, March 16, 2000.
100. Carnegie Mellon University, ECE Seminar, “Architectural Support for Java Run Time Systems”, March 15, 2000.
101. University of Paris Sud, France, Computer Science Seminar, “Architectural Support for Java Run Time Systems”, Jan 13, 2000.
102. High Performance Computer Architecture (HPCA) 2000, “Architectural Support for Java Run Time Systems”, Toulouse France, Jan 12, 2000.
103. Presentation before Technical Committee on Computer Architecture “HPCA 2002- Why Austin”, Toulouse, France, Jan 10, 2000.
104. The University of Texas Honors Colloquium, July 1999, “Design of Microprocessors”
105. IEEE International Conference on Computer Design, “Code Coalescing Unit: A Mechanism to facilitate Load Store Data Communication”, Oct 1998.
106. College of Engineering UT Austin, EFAC Council Spouse meeting, Presentation title “Research in High Performance Computer Architecture at the Laboratory for Computer Architecture”, Fall 1998 EFAC.
107. Workshop on Performance Analysis and its Impact on Design (held in conjunction with ISCA 98), “Characterization of MMX-Enhanced DSP and Multimedia Applications on a General Purpose Processor”, June 1998.

108. Workshop on Computer Architecture Education (held in conjunction with ISCA 98), “The Undergraduate Curriculum in the Electrical and Computer Engineering Department at the University of Texas at Austin”, June 1998.

109. Hawaii International Conference on System Sciences, “A Scalable Optoelectronic Interconnection Network for Parallel Computing”, Jan 1998.

110. IEEE International Conference on Computer Design, “Design and Performance Evaluation of a Cache Assist to implement Selective Caching”, Oct 1997.

111. IBM Austin Innovation Series presentation, Half-day seminar “Improving Memory Access Performance of Programs”, Aug 1997.

112. Presentation at the Workshop on Integrating Design and Design Automation into the Undergraduate Computer Science Curriculum, Tampa, FL, Aug 1997.

113. Half-day Tutorial on Rapid Prototyping using FPGAs, presented at Microelectronics Systems Education (MSE) 1997, Crystal City, VA, July 1997.

114. Research in Computer Architecture in the ECE Department, Presentation before the ECE Visiting Committee, May 1997.

115. 1996 IEEE VLSI Workshop, “A Decoupled Architecture with a CISC-style Access Processor and a RISC-style Execute Processor”, Clearwater, FL, Nov 1996.

116. IEEE Symposium on Parallel and Distributed Processing, “Improving the Parallelism and Concurrency in Decoupled Access/Execute Architectures”, New Orleans, LA, Oct 1996.

117. Presentation at the Workshop on Integrating Design and Design Automation into the Undergraduate Computer Science Curriculum, Tampa, FL, Aug 1996.

118. North Carolina State University, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, June 1996.

119. University of Texas at Austin, Electrical and Computer Engineering Department, “Improving Memory Access Performance of Programs”, May 1996.

120. Ohio State University, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, May 1996.

121. Characterization of Media Workloads: The University of Texas at Austin Digital Signal Processing Seminar, April 12, 1998.

122. University of Maryland, College Park, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, April 1996.

123. University of North Carolina Chapel Hill, Computer Science Department, “Improving Memory Access Performance of Programs”, Apr 1996.

124. The Pennsylvania State University, Computer Science and Engineering Department Colloquium, “Improving Memory Access Performance of Programs”, March 1996.

125. University of Connecticut, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, March 1996.

126. Tufts University, Electrical Engineering Department, “Improving Memory Access Performance of Programs”, March 1996.

127. Ohio University, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1996.

128. Catholic University, Washington D. C., Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1996.

129. University of North Texas, June 1996, “Improving Memory Access Performance of Programs”

130. Johns Hopkins University, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1996.

131. Arizona State University, Electrical Engineering and Technology, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, 1995.

132. Kansas State University, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, 1995.

133. University of Delaware, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1995.

134. International Conference on VLSI Design (IEEE) “Design of a Highly Reconfigurable Interconnect for Array Processors”, Jan 1995.

135. The International Symposium on High Performance Computer Architecture (HPCA-1), “Program Balance and its Impact on High Performance Architectures”, Jan 1995.

136. IEEE International Conference on Parallel Processing, “Module Partitioning and Interlaced Data Placement Schemes to Reduce Conflicts in Interleaved Memories", Aug 1994.

137. University of Kentucky, Electrical Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Summer 1994.

138. IEEE Tampa Chapter, “Rapid Prototyping Using Field Programmable Gate Arrays”, Jan 1994.

139. University of South Florida, ACM Chapter, December 1993, “Research in Computer Architecture”

140. University of South Florida, Computer Science and Engineering Department, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Jan 1993.

141. IBM Vermont, “Issues in the Design of a Decoupled Architecture for the RISC Environment”, Dec 1992.

142. ACM/IEEE International Symposium on Computer Architecture (ISCA 92), “Memory Latency Effects in Decoupled Architectures”, Goldcoast Australia, May 1992.

F. PATENTS: 16 US patents granted;

1. US patent 11,531,617 Allocating and accessing memory pages with near and far memory blocks from heterogeneous memories, L John, JH Ryoo, HM Hsu, K Ganesan, Dec 20, 2022
2. US Patent 10,949,741, Generating sets of training programs for machine learning models, LK John, R Panda, X Zheng, A Gerstlauer, 2020
3. US Patent 10,901,894, Allocating and accessing memory pages with near and far memory blocks from heterogeneous memories, L John, JH Ryoo, HM Hsu, K Ganesan, 2020
4. U.S. Patent # 10,437,648, Guided Load Balancing of Graph Processing Workloads on Heterogeneous Clusters, October 8, 2019

5. U.S. Patent 10,296,465, Processor Using a Level 3 Translation Lookaside Buffer Implemented in Off Chip or Die Stacked Dynamic Random Access memory", May 21, 2019
6. U. S. Patent 10,261,915, Intelligently Partitioning Data Cache to allocate space for Translation Entries, April 16, 2019
7. U. S. Patent 9,235,397, Method and Apparatus for increasing task execution speed, January 12, 2016
8. U. S. Patent 9,038,039, Apparatus and Method for Accelerating Java Translation, May 19, 2015
9. U. S. Patent 8,359,597, "Workload-guided application scheduling in multi-core system based atleast on application branch transition rates, Jan 22, 2013
10. US Patent 8,250,350, "Computer System with non-volatile write-protected memory based operating system and secure system architecture, Aug 21, 2012
11. US Patent 8,230,407, "Apparatus and method for accelerating Java translation", July 24, 2012
12. US Patent 8,214,629, Computer system with secure instantly available applications using non-volatile write-protected memory", July 3, 2012
13. US patent 8,041,931, "Branch prediction apparatus, systems, and methods", Granted Oct 18, 2011 (Patent has been licensed by UT)
14. U S Patent 7,370,183,"Branch Predictor comprising a split branch history shift register". Patent has been licensed by UT, May 6, 2008
15. U S Patent 7,107, 434, " System, Method and Apparatus for Allocating Hardware Resources using Pseudo Random Sequences". Patent has been licensed by UT, Sept 12, 2006
16. U S Patent 5,867,422 " Computer Memory Chip with field Programmable Memory Cell Arrays", Granted Feb 1999.

Other Applications:

1. Korean Patent 10-2008-0106796 - Method and Apparatus to save Java bytecode translations as blocks rather than per bytecode in an external (off processor) Java accelerator hardware
2. Patent Application filed in Japan and China - FE-200703-016-1-US0 - Method and Apparatus to save Java bytecode translations as blocks rather than per bytecode in an external (off processor) Java accelerator hardware
3. Patent Application filed in Korea and being filed in US, Japan and China - FE-200703-017-1-US0 - Method and Apparatus to Perform Embedding of Constants into Native Instructions
4. Provisional U. S Patent Application, Automatically Generating Microprocessor Benchmarks to Generate Maximum Power Consumption and Operating Temperature, August 2008, Application No. 61088252
5. Provisional filed on one. Field Programmable Gate Arrays for Machine Learning, September 2019, UT Austin

G. RESEARCH FUNDING:

(sponsoring agency, title of grant, total dollar value, beginning and ending dates and role)

1. SHF: Small: Quasi Weightless Neural Networks for Energy-Efficient Machine Learning on the Edge, $450K, 09/2023-08/2026 ($450K, my share)

2. Hierarchical, AI-Enabled Modeling and Optimization of Superconductor Enhanced Supercomputers, DOE, $400K, 09/2023-08/2025 (with Dr. Andreas Gerstlauer)

3. Ultra Low-Energy Ultra Low-Latency Machine Learning using Weightless Neural Networks, Semiconduction Research Consortium, $255K, Jan 1 2023-Dec 31, 2025

4. Machine Learning Workload Analysis and Characterization, Semiconduction Research Consortium, $145,500, Jan 1 2022-Dec 31, 2024

5. Hierarchical, AI-Enabled Modeling and Optimization of Superconductor Enhanced Supercomputers, DOE, $400K, 09/2023-08/2025

6. Collaborative Research: SHF: Small: Quasi Weightless Neural Networks for Energy-Efficient Machine Learning on the Edge, $600K, 09/2023-08/2026

7. Novel Computing Paradigms for Partial Differential Equations, $717,763, Exxon Mobil, July 2019 – May 2023 (co-PI)

8. Meta (Facebook), “Creating a dataset for ML-guided chip design”, $50K, Oct 2022-Oct 2023

9. ARM Corporation, “Virtual Link Architecture for Cross-Core Communication”, $50K, Sept 2021-Aug 2022. (Sole PI)

10. Facebook, “Predict the Performance of Data Center at Scale”, $60K, Jan 2021-Dec 2021 (Sole PI)

11. Machine Learning Workload Characterization, $255K, Semiconductor Research Consortium, Sept 2020 AI Hardware Program ($145.5 K my share)

12. ARM Corporation, “Virtual Link Architecture for Cross-Core Communication”, $100K, Sept 2019-Aug 2021. (Sole PI)

13. ARM Corporation, “Characterization of Video Workloads”, $25K, March 2020 (Sole PI)

14. Facebook, “Predict the Performance of Data Center at Scale”, $50K, Jan 2020-Dec 2020 (Sole PI)

15. Intel Corporation, “Miniaturized Proxies of Industry Standard Benchmarks for Pre-silicon Evaluation”, $80K, June 2019-May 2020

16. **National Science Foundation (NSF),** “Predictive Modeling for Next Generation Heterogeneous System Design”, $1 Million, Oct 2018-Sept 2023 (Co-PI)

17. Intel Corporation, “Miniaturized Proxies of Industry Standard Benchmarks for Pre-silicon Evaluation”, $80K, June 2018-May 2019

18. Samsung GRO Grant, “Learning Based Thermal Modeling”, $99K, Oct 2018-Sept 2019. (Co-PI)

19. **NSF,** "Improving Research Reproducibility using Proxy benchmarks", $214K, Oct 2017-Sept 2019 (Sole PI)

20. **NSF,** SPX: "Computing in Situ and In Transit for Hierarchical Numerical Algorithms", $800K, Sept 2017-Aug 2020 (Co-PI)

21. Intel Corporation, "Miniaturized Proxies of Industry Standard Benchmarks for Pre-silicon Evaluation", $80K, Jan 2017-May 2018. (Co-PI)

22. Samsung Austin Research Center, "Trace Snippets for RTL Power Modeling", $99,990, Dec 2016-June 2018 (Sole-PI)

23. Intel Corporation, "Power-Aware System Compilation", $300K, Oct 2013-Sep 2016, (Co-PI)

24. Oracle Corporation, "A Methodology to Identify Application Memory Access Patterns for Efficient Hierarchical Memory Subsystem", $97,283, June 2015-May 2016 (Sole PI)

25. Samsung GRO Grant, "Adaptive Energy-Efficient Designs for Next Generation Smart Phone CPUs", $99,985, Sep 2015-Aug 2016 (Co-PI)

26. Samsung GRO Grant, "Scalable Network/System Co-Simulation For Power and Performance Aware Network of Systems Design", $99,985, Sep 2015-Aug 2016 (Co-PI)

27. Huawei Corporation, "Big Data Workload Energy Characterization", $110,000, June 2014-May 2015 (Sole PI)

28. Oracle Corporation, "A Methodology to Generate Miniature Proxies for Database workloads", $60,000, Jan 2014-Dec 2016

29. Semiconductor Research Consortium (SRC), "Workload characterization for Big Data", $240,000, Sep 2013-Aug 2016 (Sole PI)

30. **NSF,** XPS: "Algorithms and Architectures for Multiresolution Applications", $749,801, Sep 2013-Aug 2015

31. AMD Corporation, "Decomposition of Large Data Analytics into Hierarchical Models", $50,000, June 2013-May 2015

32. Oracle Corporation, "A Methodology to Identify Application Memory Access Patterns for Efficient Hierarchical Caching", $60,000, June 2013-May 2014.

33. **NSF,** SHF: "Sustainable and Reliable Multicore and Many-Core Computing via Cross-Layer Solutions", $300,000, Sep 2012-Aug 2015 (Co-PI)

34. Semiconductor Research Consortium (SRC), "Multi-dimensional Modeling, Design and Exploration of Multi-core SoCs", $345K, May 2012-April 2015 (Co-PI)

35. AMD Corporation, "Automatic Generation of Multicore Proxy Workloads and Stressmarks", $50K, April 2012-March 2013 (Sole-PI)

36. AMD Corporation, “Multicore Stressmarks”, $50K, April 2011-March 2012 (Sole-PI)

37. **NSF**, SHF: Small: “Workload Characterization and Benchmark Synthesis for Emerging Computing Systems”, $425,000, Sept 2011-Aug 2015.

38. AMD Corporation, “Stress-testing Multicore Processors for Worst-Case Power Consumption and Voltage Emergencies”, $50,000, April 2010-March 2011 (Sole-PI)

39. Semiconductor Research Consortium (SRC), “Power Consumption Based Multicore Task Scheduling and Load Balancing”, $360,000, April 2011-March 2014 (Co-PI)

40. Lockheed Martin, “Performance Cloning for Dissemination of Proprietary Applications to Hardware Vendors”, $100,000, 2008-2009 (Sole PI)

41. Sun Microsystems, “Benchmark Synthesis for Performance and Power Modeling”, $45,000, 2008-2009 (Sole PI)

42. IBM Faculty Award, Workload Characterization, $15,000, 2008-2009 (Sole PI)

43. **NSF**, Collaborative Research Archer: “Seeding a Community Based computing Infrastructure for Computer Architecture Research and Education”, $67,631, 2008-2010 (Co-PI)

44. AMD Corporation, “Computer Architecture Research”, $8,000, Dec 2007-Dec 2008 (Sole PI)

45. Semiconductor Research Consortium (SRC), “Automatic Benchmark Synthesis for Validation of Performance and Power Models of High-Performance Processors”, $330,000, April 2008-March 2011 (Co-PI)

46. NSF, “Simplifying Performance Evaluation using Workload Characterization”, $300,000, Sep 2007-Aug 2011 (Sole PI)

47. AMD Corporation, “Computer Architecture Research”, $5000, Nov 2006-Nov 2007 (Sole PI)

48. IBM Faculty Partnership Award, $25,000, June 2007 (Sole PI)

49. IBM Center for Advanced Studies (CAS) Faculty Partnership Award, $7500, June 2006 (Sole PI)

50. AMD Corporation, “Computer Architecture Research”, $5,000, Nov 2005 (Sole PI)

51. Samsung Corporation, “Java Accelerators”, $128,000, Feb 2005-Aug 2006 (Sole PI)

52. IBM Center for Advanced Studies (CAS) Faculty Partnership Award, $25,000, June 2005(Sole PI)

53. **NSF,** “Statistical Techniques for Computer Performance Evaluation”, $200,000, 2004-2008 (Sole PI)

54. AMD Corporation, “Computer Architecture Research”, $5,000, Jan 2005 (Sole PI)

55. IBM Performance Evaluation Research, $500, Dec 2004 (Sole PI)

56. IBM Center for Advanced Studies (CAS) Faculty Partnership Award, “Statistical Techniques in Performance Evaluation and Benchmarking”, $25,000, July 2004 (Sole PI)

57. Hewlett Packard, “Computer Architecture Research”, $800, June 2004 (Sole PI)

58. Intel Corporation, “Performance Impact of Emerging Workloads on Intel Processors”, $35,000, March 2004 (Sole PI)

59. AMD Corporation, “Research in Computer Architecture and Workload Characterization”, $3000, Dec 2003 (Sole PI)

60. IBM Faculty Partnership Award Project: “Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads”, $25,000, June 2003 (Sole PI)

61. Intel Corporation, “Performance Impact of Emerging Workloads on Intel Processors”, $35,000, May 2003 (Sole PI)

62. IBM Shared University Research (SUR) grant, $60,000, 2002

63. IBM Faculty Partnership Award- “Developing a Methodology for Predicting Characteristics of Future/Emerging Workloads”, $25,000, June 2002 (Sole PI)

64. AMD Corporation, “Research in Computer Architecture and Workload Characterization”, $5,000, May 2002 (Sole PI)

65. Intel Corporation, “Performance Impact of Emerging Workloads on Intel Processors”, $35,000, March 2002 (Sole PI)

66. Motorola Corporation, “Development and Characterization of Control-Plane Network Workloads”, $50,000, Jan 2002

67. AMD Corporation, “Computer Architecture Research”, $5000, Dec 2001 (Sole PI)

68. IBM Shared University Research (SUR) Grant, $100,000, 2001

69. **NSF,** “Designing Microprocessors and Computer Systems for Emerging Workloads”, $265,000, 2001-2004 (Sole PI)

70. IBM Faculty Partnership Award- “Effectiveness of Out of Order Microarchitectural techniques for web server workloads”, $30,000, May 2001 (Sole PI)

71. Tivoli Corporation, “Understanding and Optimizing e-Business workloads and the underlying infrastructure”, Aug 2000 (Sole PI)

72. IBM Center for Advanced Studies Partnership Award- “Effectiveness of Out of Order Microarchitectural Techniques for web server workloads”, $25,000, March 2000 (Sole PI)

73. **NSF CAREER Award-** “Improving the Access-Execute Balance and Concurrency in High Performance Processor”s, $315,000, 1996-2000 (Sole-PI)

74. UT Co-op Book Subvention Grant, $2500, Aug 1999 (Sole-PI)

75. DELL-LARIAT grant- “Characterization of Multimedia Application and Analysis of their Performance Impact”, $32,127, July 1999 (Sole-PI)

76. Intel Corporation, Workshop on Workload Characterization, $4000, July 1999 (Sole-PI)

77. Intel Corporation, Computer hardware grant- “Characterization of Multimedia Workloads and Analysis of their Performance Impact”, $4,181, July 1999(Sole-PI)

78. Intel Corporation, “Web Server Characterization Studies on the Pentium Platforms”, $15,320, Dec 1998

79. DARPA, TRIPS: “The Tera-op Reliable Intelligently adaptive Processing System Implementation for Polymorphous Computing Architectures (PCA)”, $7,617,912, 2003-2005 (Co-PI)

80. DARPA, TRIPS: “The Tera-op Reliable Intelligently adaptive Processing System”, $3,027,480, June 2001-May 2003 (Co-PI)

81. State of Texas Advanced Technology Program (ATP) Grant, “High Performance MultiMedia Processors”, $157,800, Jan 2000 - Dec2001 (PI)

82. **NSF,** “Impact of Contemporary Programming Paradigms and Workloads”, $356,314, 1998-2001

83. State of Texas Advanced Technology Program (ATP) Grant, “High Performance Digital Signal Processors”, $134,640, Jan 1998-Dec 1999 (Co-PI)

84. IBM- SUR Grant- “End-to-End Measurement, Modeling and Simulation of Parallel/Distributed Computer Systems”, $100K, Oct 1997

85. **NSF** CISE Infrastructure Grant, Developing a Design Automation Infrastructure, $373,524, 1995-19 (Co-PI)

Ph.D. SUPERVISIONS COMPLETED:

Shuang Song	May 2020	Distributed Graph Processing (Facebook)
Jiajun Wang	May 2019	Data Reuse Optimization (Google)
Michael LeBeane	Aug 2018	Optimizing Communication for Clusters of GPUs (AMD)
Reena Panda	Dec 2017	Proxy Benchmarks for Emerging Workloads (Apple)
Wooseok Lee (0.5)	May 2018	Power-Aware Mobile Systems (Samsung)
Xinnian Zheng (0.5)	May 2017	Learning Based Performance Modeling (NVIDIA)
Jee Ho Ryoo	May 2017	Heterogeneous Memory Systems (Oracle)
M. Faisal Iqbal	Aug 2013	Multicore Communication Processors
Youngtaek Kim	May 2013	Stressmarks for Voltage Emergencies (Intel)
M. Umar Farooq	Dec 2013	Value Based Branch Prediction (ARM)
Arun Arvind Nair	May 2012	Modeling of Soft Errors (AMD)
Karthik Ganesan	Dec 2011	Automatic Generation of Synthetic Workloads for Multicore Systems (Oracle)
Jian Chen	May 2011	Resource Management for Efficient Single-ISA Heterogeneous Computing (Intel)
Ciji Isen	May 2011	The Use of Memory State Knowledge to Improve Computer Memory System Organization (AMD)
Jeff Stuecheli	May 2011	Ccordinated Memory Scheduling (IBM)
Dimitris Kaseridis	May 2011	Memory-subsystem Resource Management for the Many-core Era (ARM Corporation)
Lloyd Bircher	Dec 2010	Predictive Power Management for Multi-Core Processors (AMD)
Ajay Joshi	Dec 2007	Constructing Adaptable and Scalable Synthetic Benchmarks for Microprocessor Performance Evaluation (ARM)
Aashish Phansalkar	May 2006	Similarity Analysis and Benchmark Subsetting (Employed at Intel)
Rob Bell Jr.	Dec 2005	Automatic Workload Synthesis for Early Design Studies and Performance Model Validation (IBM, Samsung)
Byeong Kil Lee	Aug 2005	Network Processor Design: Benchmarks and Architectural Alternatives (Employed at Texas Instruments)
Shiwen Hu	Dec 2005	Effective Adaptive Computing Environment Management via Dynamic Optimization, (Freescale)
Yue Luo	Aug 2005	Improving Sampled Microprocessor Simulation (Microsoft)
Madhavi Valluri	May 2005	A Hybrid-Scheduling Approach for Energy-Efficient Superscalar Processors (Employed at IBM)
Juan Rubio	Aug 2004	Exploring the Potential of a Hierarchical Computing Model for a Commercial Server (IBM Austin Research Lab)
Tao Li	Aug 2004	OS-aware Architecture for Improving Microprocessor Performance and Energy Efficiency, (Professor University of Florida)
Ravi Bhargava	Aug 2003	Instruction History Management for High-Performance Microprocessors (Employed at AMD)
Deepu Talla	Aug 2001	Architectural Techniques to Accelerate Multimedia Applications on General-Purpose Processors, August 2001 (Vice President at NVIDIA)
Ramesh Radhakrishnan	Aug 2000	Microarchitectural Techniques to Enable Efficient Java Execution (Strategic Technology Office, Dell)

M.S. SUPERVISIONS COMPLETED:

Zachary Susskind	Dec 2022	Electrical and Computer Engineering
Steven Flolid	Dec 2021	Electrical and Computer Engineering
Qinzhe Wu	Dec 2022	Electrical and Computer Engineering
Sangram Kate	May 2021	Electrical and Computer Engineering
Daniel Rauch	May 2021	Electrical and Computer Engineering
Abigail Dowd	May 2020	Electrical and Computer Engineering
Snehil Verma	May 2020	Electrical and Computer Engineering
Harsh Gugale	May 2020	Electrical and Computer Engineering
Jim Xavier	May 2020	Electrical and Computer Engineering
Bagus Hanindhito	May 2020	Electrical and Computer Engineering
Shuang Song	Dec 2019	Electrical and Computer Engineering
Jiajun Wang	Dec 2018	Electrical and Computer Engineering
Sarbartha Banerjee	May 2018	Electrical and Computer Engineering
Yashwant Marathe	May 2018	Electrical and Computer Engineering
Alex Schulyak	Dec 2016	Electrical and Computer Engineering
Joseph Whitehouse	May 2016	Electrical and Computer Engineering
Jee Ho Ryoo	May 2014	Electrical and Computer Engineering
Darshan Gandhi	May 2014	Electrical and Computer Engineering
Abhishek Tondon	Dec 2013	Electrical and Computer Engineering
Don Owen	May 2013	Electrical and Computer Engineering
Ankita Garg	May 2013	Computer Sciences
Bhargavi Narayanasetty	May 2011	Electrical and Computer Engineering
Chaitanya Nayak	May 2011	Electrical and Computer Engineering
Rengarajan	2010	Electrical and Computer Engineering
Karthik Ganesan	Dec 2008	Electrical and Computer Engineering
Rajiv Bhatia	Aug 2008	Electrical and Computer Engineering
Justin Friesenhahn	Dec 2007	Electrical and Computer Engineering
Jason Matalka	Aug 2006	Electrical and Computer Engineering
Kathryn Stacer	May 2006	Electrical and Computer Engineering
Lloyd Bircher	May 2006	Electrical and Computer Engineering
Diego Vila	May 2006	Electrical and Computer Engineering
Brijesh Patel	2005	Electrical and Computer Engineering
Jenson Lam	2005	Electrical and Computer Engineering
Brian Gaide	2005	Electrical and Computer Engineering
Jignesh Gondalia	2005	Electrical and Computer Engineering
Saket Kumar	May 2004	Electrical and Computer Engineering
Michael Arunkumar	Dec 2003	Electrical and Computer Engineering
Michael Lance Karm	Dec 2003	Electrical and Computer Engineering
Patrick James Peters	Dec 2003	Electrical and Computer Engineering
Mike Clark	May 2003	Electrical and Computer Engineering
Anand Sunder Rajan	2003	Electrical and Computer Engineering
James Yang	2002	Electrical and Computer Engineering
Ravi Bhargava	Aug 2000	Electrical and Computer Engineering
Vikram Godbole	May 2000	Electrical and Computer Engineering

Sanjeev Ghai	May 2000	Electrical and Computer Engineering
Srikanth Kannan	May 2000	Electrical and Computer Engineering
Jyotsna Sabarinathan	Dec 1999	Electrical and Computer Engineering
Jody Joyner	Dec 1999	Electrical and Computer Engineering
Juan Rubio	May 1999	Electrical and Computer Engineering
Poorva Murarka	May 1999	Electrical and Computer Engineering
Purnima Vasudevan	May 1999	Electrical and Computer Engineering
Roy Shalem	Aug 1998	Electrical and Computer Engineering
Dachih-Tang	Aug 1998	Electrical and Computer Engineering
Yin Teh	Dec 1997	Electrical and Computer Engineering
Ramesh Radhakrishnan	Aug 1997	Computer Science and Engineering
Vijay Kammila	Dec 1996	Computer Science and Engineering
Vinod Reddy	Dec 1996	Computer Science and Engineering
Amudha Muthiah	Dec 1996	Computer Science and Engineering
Raghuveer Reddy	May 1995	Computer Science and Engineering

Ph.D. IN PROGRESS:

1. Aman Arora
2. Qinzhe Wu
3. Zhigang Wei
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5. Zachary Susskind
6. Li Ruihao
7. Ashen Ekanayake
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1. Anthony Do (2021)
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5. Tanmay Anand
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16. Xiayong Wu

VITA: *(One-half page paragraph that can be used for general purposes)*

Dr. Lizy Kurian John holds the Truchard Foundation Chair in Engineering in the Department of Electrical & Computer Engineering at The University of Texas at Austin. She received her Ph.D. in computer engineering from The Pennsylvania State University in 1993. She joined The University of Texas Austin faculty in 1996. Her research is in the areas of computer architecture, multicore processors, memory systems, performance evaluation and benchmarking, workload characterization, and reconfigurable computing.

Prof. John's research has been supported by the National Science Foundation, Semiconductor Research Consortium (SRC), DARPA, Lockheed Martin, AMD, Oracle, Huawei, IBM, Intel, Motorola, Freescale, Dell, Samsung, Texas Instruments, etc. She is recipient of NSF CAREER award (1996), UT Austin Engineering Foundation Faculty Award (2001), Halliburton, Brown and Root Engineering Foundation Young Faculty Award (1999), University of Texas Alumni Association Teaching Award (2004), The Pennsylvania State University Outstanding Engineering Alumnus (2011) etc. She is in the ISCA (International Symposium on Computer Architecture) Hall of Fame and the HPCA (High Performance Computer Architecture) Hall of Fame.

Lizy John holds 15 U. S. patents and has published 16 book chapters, 300+ refereed journal and conference publications, and more than 50 workshop papers. She has coauthored books on Digital Systems Design using VHDL (Cengage Publishers 2017, 2007), Digital Systems Design using Verilog (Cengage Publishers 2014) and has edited a book on Computer Performance Evaluation and Benchmarking (CRC Press 2005). She has also edited three books on workload characterization.

Prof. John is the Editor-in-Chief of IEEE Micro, and has served in the editorial boards of IEEE Transactions on Computers, IEEE Transactions on VLSI, IEEE Transactions on Sustainable Computing, IEEE Computer Architecture Letters, ACM Transactions on Architectures and Code Optimization. She is a member of IEEE, IEEE Computer Society, ACM, and ACM SIGARCH. She is an IEEE Fellow (Class of 2009), ACM Fellow (2020), and Fellow of the National Academy of Inventors (2020).