The University of Texas at Austin
Department of Electrical and Computer Engineering

EE 460M: DIGITAL SYSTEM DESIGN USING HDL

Spring 2014 | ENS 115 | T-Th 11:00am-12:30pm | Unique Number: 16970/16975/16980

Instructor

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Teaching Assistants

Daniel Arulraj, email on Canvas
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TA hours: On Canvas (courses.utexas.edu)
Lab and TA Office hours location: ENS 302

Course Overview

In this course, the principles of advanced digital design will be taught. This course builds on logic design principles learned in EE316: Digital Logic Design and demonstrates how digital design and rapid prototyping have been facilitated by HDLs (Hardware Description Languages) and FPGAs (Field Programmable Gate Arrays). Digital design is taught at a higher level of abstraction than EE316. This course has a significant lab component involving Verilog HDL and FPGAs. Students will learn principles of making complex digital systems work correctly and will practice prototyping such systems using state of the art tools.

Prerequisites

EE 316 and EE319K with a grade of at least C in each.

TextBook

No required text book. Course notes packet will be provided to students via HKN.

Grading Policy

Lab assignments	30%
Midterm Exams	30%
Final Exam	25%
Homeworks/Optional Labs	10%
Class Participation, Pop quizzes, Surveys	5%

Canvas

The primary mode of communication for the course will be Canvas. All lecture slides, lab documents, homeworks, TA hours, etc will be posted on Canvas. Please check the course web page periodically for any last minute announcements. Many updates may only appear on Canvas. This document and the schedule handout will also be posted on Canvas. It is the first semester we are using Canvas. So please

be patient with the TAs and me as we get more used to Canvas. Report issues to us so that we may correct the problems.

Lectures

The following topics will be covered in the lectures:

- Review of basic logic design techniques
- Design Flow, High level design
- Verilog description of digital systems, simulation and synthesis
- Design using programmable logic devices
- SM Charts and Microprogramming
- Field Programmable Gate Arrays (FPGAs)
- Advanced Topics in Verilog
- Microprocessor Design
- Test generation and design for testability
- Rapid Prototyping using FPGAs

Labs

The course has a significant lab component. Lab assignments involve modeling digital circuits in Verilog, simulation, synthesis and implementation on FPGAs. The primary lab is ENS 302. In addition to ENS 302, computers in other LRC labs can also be used. Software packages for logic design, digital system simulation, implementation on FPGAs, etc will be available in all labs. However, hardware FPGA boards are available only in ENS 302. In order to access the lab, you need your ID card/badge with the proximity chip. If you have access problems, resolve it during first week by talking to TAs and the professor.

The lab manual will be posted on Canvas. So you can start working on labs early at your convenience. The due dates for the labs are available in the schedule handout. Any updates to the lab manual and to the schedule will be notified either through announcements on Canvas or via email.

The lab submission procedure involves submitting the assignment electronically on Canvas and doing a demo to the TAs during assigned slots. The demo/checkout will be during your designated lab session after the lab due date. Labs will be accepted late with 10% credit loss per day for 5 more working days after the due date. No credit for lab assignments turned in after that except for very special situations when prior permission is obtained from the professor. The lab tends to be crowded near the due date. So, try to do your labs early.

The first 3 lab assignments (Lab 0, 1 and 2) are individual. For subsequent lab assignments, you can work with a partner. Working in teams is an important part of being an engineer and is therefore encouraged. Please form teams of 2. Lab partners have to contribute equally to the assignment. Team members can be from different lab sessions, hence each team member demos the lab separately to the TA. One submission on Canvas but separate individual demos. You can change lab partners whenever you want. If a team member does not contribute to an assignment, the TAs and I need to be informed at the demo/checkout of that lab. Questions will be asked during demo and depending on answers, different grades can be assigned to the team members. No credit will be given to non-participating team members. Do not come at the end of the semester saying your team partner did not help. If there is an issue, inform TAs and me as and when the issue is happening.

Lab 0 is a tutorial lab where you will learn the tools to be used during the entire semester in the labs. Labs 1, 2 and 3 lay the ground work. Labs 4 through 8 will give you more exposure to digital design and

interfacing. By the end, you will have designed simple digital circuits (like adders and counters) to advanced digital circuits (like a microprocessor).

Tests
There will be 2 tests during the semester and a comprehensive final. Tests are a substantial part of the overall grade and the tests will essentially evaluate you on what you learn in the lectures.

Pop quizzes and Surveys
There will be several pop-quizzes (at least 5) and attendance worksheets during the semester. No makeups will be allowed on pop quizzes. Surveys will be circulated occasionally during the lectures or via Canvas. They will be anonymous and your honest opinion is solicited. Those participating in surveys get class participation credit.

Homeworks
There will be approximately 6 paper and pencil homework assignments. You will submit your answers in the class to the TAs on the due dates. One day late submission with 10% penalty will be accepted. Further late submissions cannot be accepted because solutions might already be posted (under special circumstances you can always talk to me). You can work in groups of two on the homework assignments. Over the years, I have noticed that the homework assignments help students prepare for the tests. Please refer to the schedule handout for homework details and due dates.

Alternate for Homeworks: The homeworks typically prepare students better for tests, however some students who are well-versed with the material may like the challenge of additional labs. If you belong to that category, there are 2 additional optional labs. You can do those 2 labs instead of the paper-and-pencil HW assignments. You have to choose whether you are doing HW assignments or Alternate labs before Feb 15th. You cannot do both.

Expectations
Dishonesty in any work related to the course will be treated very seriously. No proxies allowed for pop quizzes or any other graded work. For homework and lab assignments, while discussing with other students is allowed, do not look at other students' written solutions or Verilog code. Do not leave your directories/disks accessible to others. Group partners are supposed to equally contribute to the assignment and to all the parts of the assignment.

Cell phones should be turned off before the class starts. If your cell phone rings in class, you will lose credit equivalent to one pop quiz. If my phone rings in class, those in class will get free credit equivalent to 1 quiz.

No disruptive activity/talking amongst students is allowed in class during lectures. If you have a question on the material, ask the instructor. Be professional in your behavior in class. Disruptive activity can lead to grade penalties.

Academic Dishonesty
Faculty in the ECE Department are committed to detecting and responding to all instances of scholastic dishonesty and will pursue cases of scholastic dishonesty in accordance with university policy. All parties in our community -- faculty, staff, and students -- are responsible for creating an environment that educates outstanding engineers, and this goal entails excellence in technical skills, self-giving citizenry,

and ethical integrity. Industry wants engineers who are competent and fully trustworthy, and both qualities must be developed day by day throughout an entire lifetime. Scholastic dishonesty includes, but is not limited to, cheating, plagiarism, collusion, falsifying academic records, or any act designed to give an unfair academic advantage to the student. The fact that you are in this class as an engineering student is testament to your abilities. Penalties for scholastic dishonesty are severe and can include, but are not limited to a record in your academic folder, a zero on the assignment/exam, re-taking the exam in question, an F in the course, or expulsion from the University. Don't jeopardize your career by an act of scholastic dishonesty.

Details about academic integrity and what constitutes scholastic dishonesty can be found at the website for the UT Dean of Students Office and the General Information Catalog, Section 11-802.

Course Evaluation

This course will be evaluated using the standard UT course/instructor evaluation forms during the last week of class. In addition, the instructor may use a few other in-class evaluations.

Drop Policy

The fourth day of University classes is the last day of the office add/drop period. After this official period, all course changes must be initiated with the student's academic dean and must have the approval of a departmental advisor and the dean's representative. Typically drops are not approved unless students can demonstrate "good cause", i.e. health or personal problems that did not exist at the end of the official add and drop period.

The University of Texas at Austin provides, upon request, appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD or the College of Engineering Director of Students with Disabilities at 471-4321.

Engineering Professionalism

Imagine working as an engineer in one year. Whether in academia or industry, your success will be partly determined by how others perceive you. Much of your recognition will come from your creativity, design abilities and your problem-solving skills. However, a large part of your success will be determined by your superior's or colleagues' perception of your professionalism as a part of your engineering capabilities. In fact, you might possess some of the best technical skills in the world, and still be a failure as an engineer if you do not conduct yourself in a professional manner. Here are a few of the attributes of professional behavior related to this class:

On-time arrival to class and for group meetings: Repeatedly showing up late to work could indicate that you do not care. Showing up late to a meeting suggests that you are disorganized and have no respect for the others in attendance. Showing up late to class can disrupt the class. At times, I have pop quizzes at the beginning of the class. If you have a legitimate reason like a job interview, please inform the instructor early that you will be arriving late or leaving early.

Proper conduct in group settings: Being courteous to a speaker, giving others time to speak, listening, and avoiding disruptive behavior are all expected in any professional environment. No disruptive activity/talking amongst students in class during lectures. During lecture, if you have questions or clarifications, ask the instructor. Cell phones should be off during lectures.

Being prepared: Imagine the negative consequences of showing up to an important meeting with your boss and not knowing the subject under discussion. Being prepared for a meeting, presentation, or discussion is fundamental to engineering professionalism.

Clear communications: Whether oral or written, the ability to communicate with others in a clear way is fundamental. If you have special problems, feel free to communicate to the professor.

Complete and thorough documentation: Your work must be accurate, complete, thorough and above all neat. Others must be able to understand what you have done. The professionalism of the documentation you produce will reflect on how good an engineer you are.

Honesty: Do your share. Never take credit for the work of others. Contribute fairly to your group. Do not expect your team-mate to do the hard work.

Dedication: No team would want a player that does not care about achieving the team goals. Being dedicated to the goals of the team and doing what it takes to achieve the goals separates the winners from the losers.

A major part of our responsibility here at the University of Texas is to prepare you for your future roles. Just as described above, the professionalism you demonstrate on a daily basis will have an impact on your success here and in life.

Finally, **your time here is a fantastic opportunity to learn and grow. Digital Design using HDLs and FPGAs is one of the most interesting things in the world to learn. It is a lot of fun and joy. Dedicate yourself to your studies and to preparing yourself for the wonderful opportunities that come from being a digital systems designer and an engineer.**