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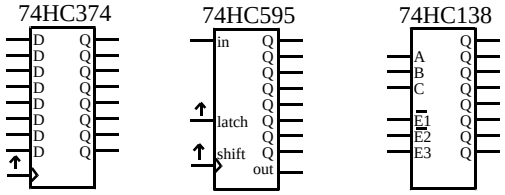
October 4, 2006, 1 to 1:50pm

This is an open book, open notes exam. You may put answers on the backs of the pages, but please don't turn in any extra sheets.

(25) Question 1. The objective of this question is to design a 24-bit parallel output interface to your 9S12C32, which only has an 8-bit PAD, 6-bit PTM, and 8-bit PTT. Your interface should be able to set and clear each of the 24 bits independently. You are free to build the interface using as many of the following building blocks as you need. The 74HC374 is an 8-bit D flip flop, the **D** inputs are copied to the **Q** outputs on the rising edge of the clock. The 74HC595 has an 8-bit internal shift register and an 8-bit latch, the **in** signal is shifted in and the **out** signal is shifted out on the rising edge of the shift signal. On the rising edge of the latch signal, the values of the 8 bit shift register are latched so the 8 signals are available on the **Q** outputs. The 74HC138 is a decoder. The decoder is active if **E1**=0, **E2**=0 and **E3**=1. If active there is exactly one **Q** output which is low depending on the ABC input address. The other seven **Q** outputs will be high. If the decoder is inactive, all **Q** outputs are high.

74HC32 74HC08 74HC04



Part a) Show a basic block diagram for the hardware interface. External logic will be required.

Part b) Show the software device driver. The function names and parameters are given.

```
// initialize 24-bit interface
void Dig24_Init(void){
```

```
// output 24 bits
void Dig24_Out(char data[3]){
```

(25) Question 2. One way to manage free-space on a disk is to implement a **bit vector**. For each of the 256 blocks on our disk, there will be a single bit, specifying whether the block is free (1) or allocated. In C, we can define 256 bits as a word-array with 16 entries.

```
unsigned short BitVector[16];
```

Similar to the directory, the BitVector will exist both in RAM, as the above C definition, and on the disk as block 1. The format operation will initialize 254 of these bits to 1, performing:

```
BitVector[0] = 0x3FFF; // blocks 0,1 used (directory, BitVector)
for(i=1;i<16;i++) BitVector[i]=0xFFFF; // blocks 8-255 are free
eDisk_WriteBlock(BitVector,1);         // update disk copy
```

Part a) Write a helper function that allocates a free block updating the disk copy of BitVector.

```
// allocate a free block, returns a block number of a free block
// Output: block number 2 to 255 if successful and 0 if full
unsigned char AllocateBlock(void){
  eDisk_ReadBlock(BitVector,1);        // fresh RAM copy
```

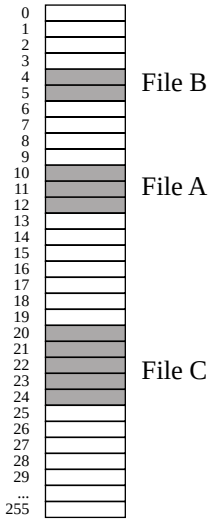
Part b) Write a helper function that deallocates a block updating the disk copy of BitVector.

```
// deallocate a free block
// Input: block number 2 to 255
void DeallocateBlock(unsigned char blockNum){
  eDisk_ReadBlock(BitVector,1);        // fresh RAM copy
```

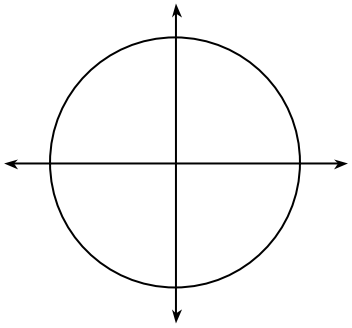
(10) Question 3. Consider a file system that uses contiguous allocation as illustrated by the figure on the right. The block size is 32 bytes and all 256 blocks can be used to store data. The directory is not stored on the disk. Each directory entry contains the file name (e.g., A, B, C), the start block (e.g., File B starts at block 4) and the number of blocks used in the file (e.g., File C has 5 blocks). The file sizes are always a multiple of 32 bytes. I.e., a file can contain only 32, 64, 96, … 8192 bytes. For example, File A is 3*32=96 bytes, File B is 2*32=62 bytes and File C is 5*32=160 bytes. Does this system have external fragmentation? Explain your answer.

Directory

`A,10,3`
`B,4,2`
`C,20,5`



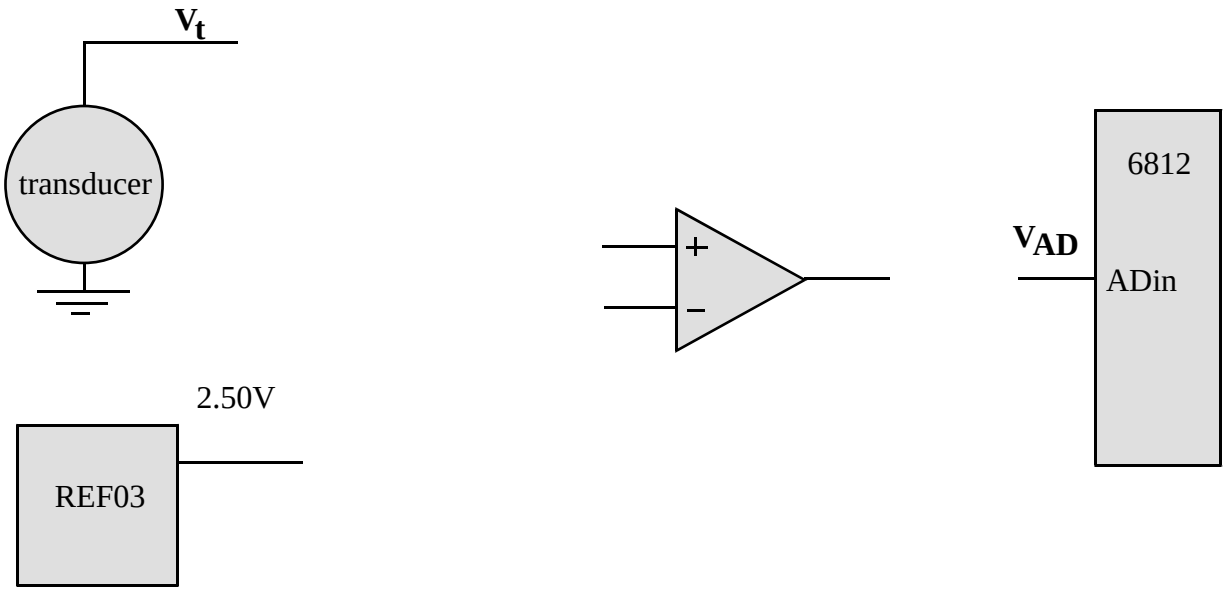
(20) Question 4. The sampling rate of a real-time data acquisition system is 4000 Hz. There is a large amplitude noise component at 250 Hz. Show pole-zero plot for the design of a high-Q 250-Hz digital reject filter. Just draw the positions of the poles and zeros. You do not have to calculate the H(z) or show the filter equation.



(20) Question 5. The objective of this question is to design the analog electronics to interface a transducer to the 0 to +5V built-in ADC of the 6812. The transducer output, $\mathbf{V_t}$, is a single voltage (relative to ground, not differential), with a range of 0.3125 to 0.9375 volts.

$$\mathbf{V_{AD} = 7.5 - 8V_t}$$

Part a) Build this interface with one op amp and a REF03 2.50V analog reference. You do not need to show the power connections. You do not need to include an analog low pass filter.



Part b) What is the voltage resolution, referred to input $\mathbf{V_t}$, of the system if the ADC has 10 bits?