Jonathan W. Valvano November 20, 2000, 11:00am-11:50am

(40) Question 1. Implement the following IIR digital filter at 250 Hz.

Part a) Show the private global variables required to implement this system.

```
unsigned char x[3],y[3]; // raw and filtered data
```

Part b) Show the ritual that initializes the system.

```
#define Rate 8000
#define OC0  0x01
void ritual(void) {
asm(" sei");     // make atomic
  DDRH=0xFF;     // Port H is outputs
  TIOS|=OC0;     // enable OC0
  TSCR|=0x80;    // enable
  TMSK2=0x32;    // 500 ns clock
  TMSK1|=OC0;    // Arm output compare 0
  y[1]=y[0]=x[0]=x[1]=0;
  TFLG1=OC0;     // Initially clear C0F
  TC0=TCNT+Rate; // First one in 4 ms
asm(" cli"); }
```

Part c) Show the output compare channel 0 interrupt service routine. Show the code for all functions that you call.

```
unsigned char A2D(unsigned char chan){
  ATDCTL5=chan;    // Start A/D
  while ((ATDSTAT & 0x8000) == 0){};
  return(ADR0H); }
#pragma interrupt_handler TOC0handler()
void TOC0handler(void){
  TFLG1=OC0;       // ack OC0F
  TC0=TC0+Rate;    // Executed every 4 ms, is 250 Hz
  y[2]=y[1];       // shift Y MACQ data
  y[1]=y[0];
  x[2]=x[1];       // shift X MACQ data
  x[1]=x[0];
  x[0] = A2D(2);   // new data
  y[0]=(12*x[0]-10*x[2]+25*y[2]+16)/32;}
```

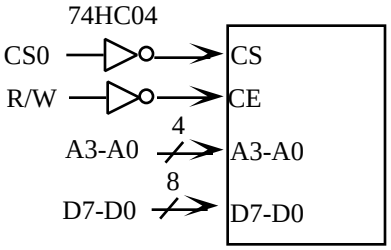
Part d) Show the code that specifies the output compare interrupt vector, i.e., set the 16-bit value at 0xFFEE.

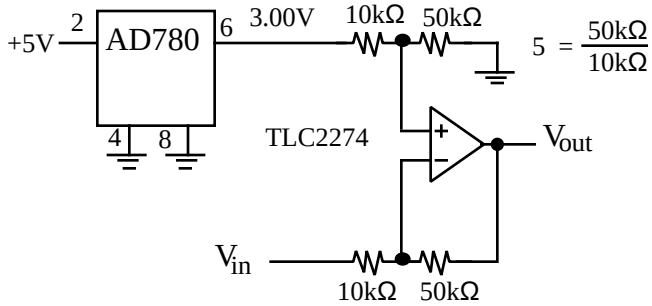
```
#pragma abs_address:0xffee
void (*TC0_vector[])() = { TOC0handler};
#pragma end_abs_address
```

(20) Question 2. Design an analog circuit that runs on a single +5V supply.

Part a) V_{out} =5•(V_{in}-2) or V_{out} =5•(3 - V_{in}) I built this second one

Part b) Show the circuit. Label all chip numbers, resistors and capacitors but not pin numbers.





(40) Question 3. Interface an Output chip

Part a) WDA=(106,t_{cyc}+20)

Part b) WDR = (earlier(↓CS-150, ↓CE-150),earlier(↓CS, ↓CE))

Part c) Show digital circuit for the interface between the expanded narrow mode 6812 and the output port.

Part d) This interface is trigger on ↓CS. The ↑CS0 is t_{cyc}+10, so ↓CS is t_{cyc}+20, assuming a 10ns gate delay. 106<↓CS-150 or 106< t_{cyc}+20-150 or 236< t_{cyc} So 1 stretch is needed to make t_{cyc}= 250ns.