

Aashish Phansalkar
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Objective: To seek an internship position related to my research interests.

Research Interests: Computer Architecture, Performance Evaluation, Statistical techniques for workload characterization, Benchmark subsetting to reduce simulation time for benchmark suites.

Education: **Ph. D, Electrical and Computer Engineering, (currently pursuing)**
University of Texas at Austin (Advisor: Dr Lizy K John)
Current GPA: 3.81/4.0
M.S., Electrical and Computer Engineering, August 2002.
University of Texas at Austin.
Bachelor of Engineering, Electrical Engineering, June 2000.
Government College of Engineering, Pune.
University of Pune, India.

Publications:

Measuring Program Similarity: Experiments with SPEC CPU Benchmark Suites

Aashish Phansalkar, Ajay Joshi, Lieven Eeckhout, and Lizy K. John.

IEEE International Symposium on Performance Analysis of Systems and Software. March 2005.

Analyzing and Improving Clustering Based Sampling for Microprocessor Simulation

Yue Luo, Ajay Joshi, Aashish Phansalkar, Lizy John, and Joydeep Ghosh.

17th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD).
October 2005.

Measuring Benchmark Similarity using Inherent Program Characteristics

Ajay Johi, Aashish Phansalkar, Lieven Eeckhout, Lizy John

To appear in IEEE Transactions on Computers

Performance Prediction using Program Similarity

Aashish Phansalkar and Lizy John

To appear in SPEC workshop

Related Courses:

Advanced Computer Architecture, Superscalar Computer Architecture, Computer Performance Evaluation and Benchmarking, Data Mining, Engineering Programming Languages, Computer Architecture, Operating Systems, Compilers, High Speed Computer Arithmetic, Statistical Methods in Engineering, VLSI-I, Digital integrated circuits, Data Structures in C++, Digital Electronics, Microprocessor fundamentals and applications, Advanced microprocessor techniques, Power Electronics, Digital Computational Techniques, System Design Metrics.

Experience: **Graduate Research Assistant at Laboratory for Computer Architecture**
August 2004-till date.

24th May 2004 – 24th August 2004

Summer Intern at Intel Corporation

Worked as a summer intern at Intel Corp. (LTDN Design group). Worked as a member of circuit design group and owned functional block to complete circuit design goals on domino and register file elements. I was always wanted to get some idea about circuit design on a bigger scale.

21st May 2001 – 28th August 2001

Summer Intern at Oasis Design Inc, Austin TX.

Oasis Design Inc is dedicated to develop hardware that supports multimedia-networking solutions for automotive, industrial, PC and home market. Media Oriented Systems Transport (MOST) fiber optic network is the backbone for these solutions. I was working on a design project for the network interface chip.

1) Design and verification of routing bus interface for the micro controller on the MOST2 (Network interface IC).

2) Verification of Source data engine and routing bus interface for the same.

Tools used: VHDL, Design Analyzer (Synopsys).

Teaching experience

September 2000- May 2002

Teaching Assistant for Electrical and Computer Engineering laboratory at UT Austin.

August 2002-May2004

Teaching Assistant for Digital Systems Design lab at UT Austin.

**Projects done
at school:**

Computer Architecture

1) Designed a very simple tool to implement event counting on Pentium 4 machine. The tool consists of a device driver program on Linux platform and user interface program written in C to setup the event counting. Analysis on how to further modify the tool to implement Precise Event Based sampling (PEBS) and micro-op tagging was also made. Verification of the simple event counting was done using a small test program written in C with level 0 optimization using gcc compiler.

2) Modification of SimpleScalar simulator code to add victim cache and pre-fetch buffer and verify results stated by Jouppi about the gain in performance.

3) Design of a trace driven cache simulator and analysis of instruction mix of the simulator itself using Sun's Spix tools.

4) Optimization of matrix multiplication program for speed using software techniques like loop unrolling, cache blocking to increase instruction level parallelism.

5) Simulator for LC-2 (university little computer) which includes assembler and micro-architecture simulator. Programming was done using C.

Logic / Circuit Design

1) Design of a transistor level sequential circuit of minimizing power delay product with fixed area budget.

2) Gate level schematic design and simulation of an 8-bit ALU that executes the arithmetic, logical, shift and compare instructions, using a CAD tool from Micromagic Inc.

3) Modification of Verilog code of university design of ARM-2 microprocessor to include saturated arithmetic instructions to its instruction set.

Programming :

1) Study of importance of templates in C++ and developed a class of valarray for lazy evaluation over a wide range of variables (scalars, complex numbers and valarrays).

2) Implementation of similar valarray class in Java, but using object oriented approach and compare the performance of both.

3) Implementation of network controller in C++ to control bandwidth and a scheduling algorithm.

Skills: Programming Languages: C, C++, Java, Python, Familiarity with Perl.

Familiarity with tools: SimpleScalar Toolset, Cacti cache model simulator to calculate cache access latency and power, Shade Analyzers from Sun Microsystems