Digital System Design

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Reference:

- Digital Systems Engineering. W.J. Dally and J.W. Poulton. Cambridge University Press, 1998.

Background

So far we have looked at “Boxes” and “Chips,” which are abstractions.

And, in the past, designers have ignored electrical issues in digital system design.

Instead they’ve designed in terms of discrete logic.

Due to technology trends, this is no longer possible.

A Digital System

A **Digital System** represents information with discrete symbols (usually 0 and 1).

In a Digital System, noise below a given threshold is completely thrown out and can be corrected.

Digital Systems are constructed from 3 basic components:

- Logic - operates on symbols (eg, add two numbers)
- Memory - stores symbols or moves information in time
- Communication Channels - moves information in space (eg, wires)

Systems-Level Engineering Issues

- Power Distribution
- Noise Management
- Signaling
- Timing
- Synchronization

System-Level Design is More Challenging

- Wires
  - Off-Chip: Transmission lines at high frequency.
  - On-Chip: More resistive.
- Number and speed of gates increasing faster than number and speed of pins.
  - Interchip communication a system bottleneck.
  - Overcome by signaling and timing conventions.
- Power Distribution
  - Lower supply voltages, higher current, thinner metal layers, make power distribution a challenge.
- Clock skew/jitter at high frequencies.

Importance of System-Level Issues

- Digital Systems engineering issues affect:
  - Performance
  - Reliability
  - Power dissipation
- Many examples of chips and systems not working due to system-level issues not adequately addressed.

Treatment

- System-level design largely ignored in academia
  - Courses on circuits/logic, RTL/arch are common.
  - Courses on circuits to design systems are less common.
- Misconception: must abstract electrical properties to discrete symbols.
- Meaningful architecture design requires knowledge of:
  - System organization.
  - Interfaces (channel protocols).
- System-level engineering is important because it constrains architecture and defines cost.

Ad Hoc Solutions

The following are suboptimal solutions but still show up:

- Tune open-loop clock tree.
- Wide metal lines for power.
- Full swing signaling.
- Corner pins for power and ground.

Companies often address system level problems using the same solution they used last time. This leads to problems as technology advances.

Standards

Standards are a major influence, even if solution is suboptimal. For example:

- Edge triggered synchronous timing.
- Full swing underterminated voltage mode signaling.
- Many catalog parts use these.

Trend toward ASICs implies catalog parts less essential and better solutions are used.

Systems Analysis of a Multicomputer Node

See Figure 1-1 in Daley and presented in lecture.

Architect presents system designer with block diagram

- Information flow (B/W required).
- Power flow.
- Timing Information.
- Architectural simulations.

Choose signaling conventions and see if you can meet pin counts

Feeds and Speeds

Efficient use of available B/W very important for overall system performance.

A good design balances demands for B/W against the number of chips and pins and wiring area.

Controlled by the partitioning and topology of the system

Problem: Not Enough Pins for the Router

Potential solutions:

- Reduce router B/W - performance hit.
- Pay more money - faster signaling convention or larger pin count.
- Repartition Router - 2 router chips, may have to communicate with each other.

Signaling Conventions

A signaling convention is a method used to encode symbols into physical representations.

Criteria for a good signaling convention:

- maximize B/W per pin
- minimize power dissipation
- noise immunity

Current Mode vs. Full-Swing Signaling

Current mode signaling (eg, SECM) encodes signals as positive or negative currents (± 2.5mA). The receiving end uses an amplifier to measure the change in voltage over a terminating resistor.

Full-swing (eg, CMOS) encodes signals as 3.3V or 0V. The transmission lines are unterminated and the receiver uses a CMOS inverter to read signals. It takes multiple steps just to drive the wire with the signal.

Current mode signaling:

- Is faster - uses incident wave signaling, terminated transmission lines.
- Uses less power - small signal swing.
- Offers better noise immunity - better signal isolation.

See Chapter 3 and 7 of Dally for more on these conventions.

Timing and Synchronization

A timing convention governs when signals can change and when they are sampled.

Examples of synchronous timing conventions:

- Edge triggered flip-flops.
- Level sensitive latches.

Clock distribution:

- Off-chip - clock trees with matched transmission lines and buffers.
- On-chip - lossy wires and power supply variations pose difficulties.

Trends

Not just feature size, $0.25 \rightarrow 0.18$.

But also:

- Chip size
- Voltages
- Grids/Tracks
- Gate Delay
- Pins
- RC

Power Distribution

The challenge: supply a stable DC voltage under large AC current demands.

The resistance (on-chip) and inductance of wires (pins, board) present difficulties.

Current demand can range from 0 to it's maximum value in half a clock cycle. The current transient induces high voltage transient across the parasitic inductance of the package. Use on-chip bypass capacitors and regulator to alleviate this problem.

Noise

Corrupts signals on channels between modules, disturbs the state of logic networks and memory cells adds jitter to timing.

Digital implies we can recover signal within the noise margin, a fixed threshold.

Interference is noise created by the system. Generated by power supply (modulates the delay of timing elements), cross talk (one line coupled to another), intersymbol interference (same line, different symbols, slow circuits or bad terminations).

Manage noise with a gross noise margin.

Cancel noise whenever possible (differential amplification).