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Office Hours: MW 1:00-2:00pm, ACE 6.120

EE 382M – Verification of Digital Systems
Spring 2004
Lecture: MW 3:30-5:00pm

Description:

This course aims to study the use of computers to automate digital design—specifically, we address the problem of checking the correctness of digital hardware.

We will begin by defining analytical models for hardware and the problem of formally verifying the equivalence of combinational logic designs.

Model checking is a popular paradigm for the formal verification of digital designs. In this approach properties are specified as formulas which are interpreted over designs. We will motivate model checking, and describe associated verification algorithms. This will be followed by a survey level treatment of some topics related to formal verification—compositional methods, theorem proving, mathematical logic and automata theory.

Real-world verification engineers use "testing"—they write assertions about the design, and then run test cases over a simulation model of the design. We will study techniques that assist designers in specifying these test cases.

Regular lectures will be interspersed with seminars by industrial practitioners of FV, who will share their real-life verification experiences.

Prerequisites:

This course is intended for graduate students with an interest in system-level VLSI design, hardware/software systems, communication protocols, and discrete-event systems. A knowledge of digital design and C programming, and a reasonable degree of mathematical sophistication will be expected. Everyone is welcome to attend; visitors from industry are especially encouraged.

Recommended reading:

1. Kenneth L. McMillan, "Symbolic Model Checking", KAP, 1993.
2. H. Enderton, "A Mathematical Introduction to Logic", Academic Press, 1972.
3. VIS Group, "VIS: Verification Interacting with Synthesis" `www.cad.eecs.berkeley.edu/~vis`.

Format/Evaluation:

Approximately 6 homeworks will be assigned. These will range from devising algorithms to verifying designs, and will be worth 35% of your grade. There will be one midterm on Wednesday March 24, 2004 worth 30% of your grade; a final project will constitute the remainder of the grade. The project will entail designing a verification algorithm or experimenting with verification in the context of a design.

Tentative Outline

Warming up

1. Introduction to formal verification
2. Modeling hardware
3. Combinational equivalence checking
4. BDDs
5. Sequential equivalence checking

Model checking

1. Temporal logic—syntax and semantics
2. Explicit approaches to model checking
3. Symbolic model checking
4. Compositional verification
5. Regular languages and automata
6. Mathematical logic

Testing

1. High-performance simulation
2. Coverage metrics
3. Input generation under biases and constraints
4. Enhancing simulation with ATPG and BDDs
5. Commercial offerings: Verisity

Guest lectures

1. Guest lecture—simulation
2. Guest lecture—testing
3. Guest lecture—practise

Projects

1. Project Presentations—1
2. Project Presentations—2

Note: All departmental, college and university regulations concerning drops will be followed. The University of Texas at Austin provides upon request appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD.