

EE382m: Homework 1

Modeling Hardware

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Due 2.9.04

1. Construct a circuit which has as primary inputs the vector \vec{x} and c (a single control bit) and produces $F(G(\vec{x}))$ when $c = 1$ and $G(F(\vec{x}))$ when $c = 0$.

Assume that F and G are to be implemented by given fixed combinational logic blocks. Your implementation is to be efficient in the sense that it should use as few of the F and G blocks as possible. You are free to use all the glue logic you want (i.e., MUXes, AND gates, INVertors, etc.).

Hint—the best implementation is not a netlist.

10 marks

2. Given a netlist η with initial state s_0 , the output language $\Theta_{s_0}^\eta$ is defined to be the set of all output sequences that η can produce for the initial state s_0 . (Note that the output language is simply the projection of $L_{s_0}^\eta$ with respect to the outputs.)

Let η_1 and η_2 be netlists, with initial states s_0 and t_0 respectively; show there is a netlist μ with initial state m_0 so that

$$\Theta_{m_0}^\mu = \Theta_{s_0}^{\eta_1} \cup \Theta_{t_0}^{\eta_2}$$

10 marks

3. Recall that a language over a set A is a set of sequences over A . In the sequel assume $A = X \times Y$, where X and Y are specified sets.

A language \mathcal{L} over A will be called a *Moore language* if the following holds:

- For every sequence $f = \langle (x_0, y_0), (x_1, y_1), \dots, (x_{n-1}, y_{n-1}) \rangle$ if $f \in \mathcal{L}$, then for every $c \in X$ the sequence $\langle (x_0, y_0), (x_1, y_1), \dots, (c, y_{n-1}) \rangle$ is in \mathcal{L} .

Suppose Γ is an arbitrary language over A . Show that there exists a unique maximal Moore language Γ^* contained in Γ . (By this I mean that there is exactly one language Γ^* such that (1.) Γ^* is Moore, and (2.) is contained in Γ , and (3.) there is no other Moore language containing Γ^* which is also contained in Γ .)

10 marks

4. Design D_1 is defined to be a **safe replacement** for design D_0 (denoted by $D_1 \preceq D_0$) if given any state $s_1 \in S_{D_1}$ and any finite input sequence $\pi \in I^*$, there exists some state $s_0 \in S_{D_0}$ such that the output behavior of D_1 at s_1 on applying input π coincides with that of D_0 at s_0 under π (i.e., in the terminology of FSM's, $\lambda_{D_1}(s_1, \pi) = \lambda_{D_0}(s_0, \pi)$).

- (a) Is state 111 in D_0 is equivalent to any state in D_1 ?
- (b) Is state 10 in D_1 is equivalent to any state in D_0 ?
- (c) Is the design $D1$ in Figure 1 a safe replacement for design $D0$?

15 marks

5. Extra credit

First we review a couple of definitions:

Definition 1 Given states $s_0 \in S_{D_0}$ and $s_1 \in S_{D_0}$, we say state s_0 is **equivalent** to state s_1 (denoted by $s_0 \sim s_1$) if for any sequence of inputs $\pi \in I^*$, it is the case that $\lambda_{D_0}(s_0, \pi) = \lambda_{D_0}(s_1, \pi)$.

Definition 2 Given a design D_0 , a sequence of inputs $\pi \in I^*$ is called an **initializing sequence** for the design if for any pair of states s_0, s_1 in the design, we have $\delta_{D_0}(s_0, \pi) \sim \delta_{D_0}(s_1, \pi)$.

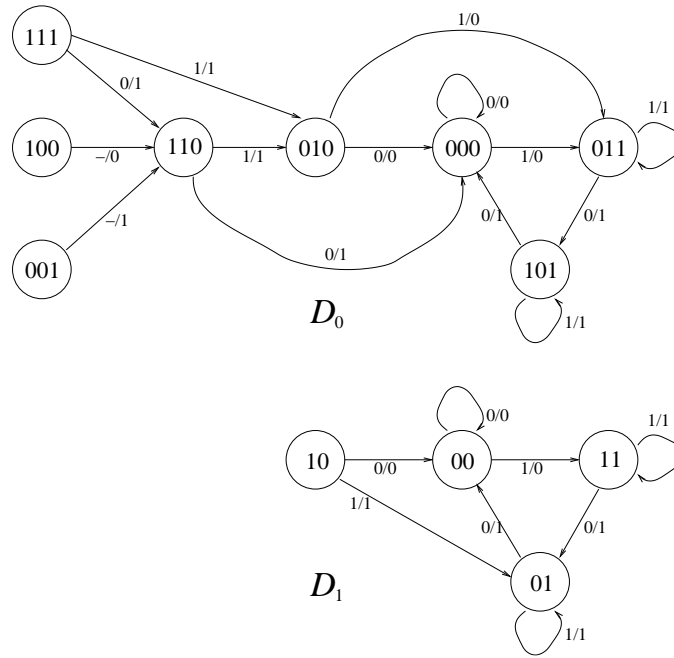


Figure 1: Example of a safe replacement ($D_1 \preceq D_0$)?

Prove the following:

If $D_1 \preceq D_0$ and ρ is an initializing sequence for D_0 then ρ is also an initializing sequence for D_1 and for any states $s_0 \in S_{D_0}$ and $s_1 \in S_{D_1}$, we have $\delta_{D_0}(s_0, \rho) \sim \delta_{D_1}(s_1, \rho)$.

25 marks