EE 382M.7 — VLSI-1 (17235) Fall 2007
Adnan Aziz ACE 6.120
Office Hours: TuTh 11:00-12:00 Lecture: TuTh 12:30-20-0, ENS 126

Description:

We aim to study the process of implementing a digital system as a CMOS integrated circuit.

The course will begin with a review of the basics of CMOS transistor operation and the manufacturing process for CMOS VLSI chips.

We will then study in detail the problem of implementing logic gates in CMOS. Specifically, we will cover layout, design rules, and circuit families.

Afterwards, we will examine techniques for analysing and optimizing timing and power at the circuit level. We will study sequential elements—latches and flops—and clocking. This will be followed by an overview of datapath design: detection logic, shifters, comparators, adders, and multipliers. We will also study memories, specifically the workhorse 6-T SRAM cell as well as peripheral decode logic.

The course will conclude with a survey level treatment of various topics, including advanced circuit design techniques, clock tree design, functional verification, test, design-for-test, electrical effects, packaging, and future trends.

Prerequisites:

This course is intended for ECE graduate students. A knowledge of Electical Circuits (EE411 or equivalent), and Digital Logic Design (EE316 or its equivalent) is required.

Recommended text:

- CMOS VLSI Design: A Circuits and Systems Perspective. N. Weste and D. Harris. *3rd Edition*, 2005. Addison-Wesley.

Web site: All material related to the course is available at `www.ece.utexas.edu/~adnan`

Format/Evaluation:

I will assign approximately 6 written homeworks, which will consist of questions from the book, and will be worth 5% of your grade. There will be two in-class midterms worth 35%, and a final project, worth 25% of your grade. Three major design projects will make up the remaining 35% of your grade.

Outline

Week	Material
	Preliminaries
Aug 30	Introduction, history
Sep 4	MOS transistors, Lab 1 presentation
Sep 6	MOS transistors
Sep 11	CMOS processing
	CMOS circuit and logic design
Sep 13	Basic logic gate design
Sep 18	Basic physical design
Sep 20	Logical effort
Sep 25	Interconnect, Lab 2 presentation
Sep 27	Circuit families
Oct 2	Adders
Oct 4	Sequential elements
Oct 9	Clocking
Oct 11	SRAMS
	Datapath and memories
Oct 16	ROMs, CAMs, PLAs
Oct 18	Datapath-1, Lab 3 presentation
Oct 23	Midterm 1
Oct 25	Datapath-2
	Topics
Oct 30	Test-1
Nov 1	Test-2
Nov 6	DSM effects
Nov 8	Verification
Nov 13	Verification Circuit pitfalls
Nov 15	Low power
Nov 20	Midterm 2
Nov 22	THANKSGIVIING
Nov 27	Clock trees, PLLs
Nov 29	I/O
Dec 4	Scaling-1
Dec 6	Scaling-2

NOTE: All departmental, college and university regulations concerning drops will be followed. The University of Texas at Austin provides upon request appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD.