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EE 306
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Solutions to Problem Set 4
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1 (4.8)
  a) 8 bits
  b) 7 bits
  c) 3 bits

2 (5.2)
We cannot tell anything about the size of MAR from the given information.
Size of MDR is 64 bits.

3 (5.4)
  a) 8 bits are required for the address
  b) 6 bits are required for the PC offset
  c) PC offset for address 10 would be +6 (addresses in decimal) or +C
     (addresses in hex)

4 (5.10)
A: BRnzp x155
B: JSR xF55

A is a conditional branch instruction (that is, it checks the condition codes),
whereas B is an unconditional jump.
B stores return address automatically in R7, whereas A does not.

5 (5.16)
  a) LD is the best to use for loading a single value from an address within
     +256 or -255 locations of the LD instruction.
b) To load from an address which is further away than is allowed by the PC offset, LDI can be used. LDR can also be used if the address you want to load from is in the base register.

c) To load from an array of sequential addresses, LDR is the best to use. The base register can be easily incremented to load each successive value into a register before using it.

6 (5.22)

The instructions are:
LEA R3, x3F ; R3 ← x3050 (x3010 + x1 + x3F)
LDR R4, R3, x0 ; R4 ← x70A4
LDR R6, R4, x0 ; R6 ← x123B

Therefore, x123B is loaded into R6. The 3-instruction sequence can be replaced by a LDI R6, x3F

7 (5.24)

The largest address the instruction can load from is x4030 (x4011 + x1F). With a zero-extended LDR, the largest address the instruction can load from is x4050 (x4011 + x3F).
The smallest address that the zero-extended LDR could load from is x4011 (x4011 + x0).

8 (5.26)

a) To address 64KB we would need 16 bits since 64K = 2^6*2^{10} = 2^{16}
b) Largest immediate value that can be represented is +1. (Opcode + DR + SR + Steering Bit = 14 bits, which means 2 bits are left to represent immediate value. The largest 2’s complement number that can be represented in 2 bits is +1). However, since the opcode, DR, and SR take up 13 bits, we cannot use the register add mode anyways. So there is no need for the steering bit, in which case the largest immediate value is +3. Either answer is acceptable.
c) Each operating system routine takes 32 memory locations. There are 128 routines, so totally 4KB or 4096 bytes will be required.
d) +63 is the largest immediate value. Logic is the same as part b.

9 (5.32)

Since we don’t know the initial value in R0, we cannot say what the condition codes would be at the end of execution of the given segment of code.

10 (5.40)

A is the signal which tells the computer whether or not to branch.
MUL Ri, Rj, Rk is the most useful instruction.

MOVE and NAND require 1 instruction and 2 instructions respectively in the LC3.
SHFL can be implemented with 1 MUL instruction. MUL cannot always be implemented with SHFL, though. So, MUL is the most useful.