CMOS Analog Integrated Circuit Design

Lab 1 Introduction to Cadence

Department of Electrical and Computer Engineering

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In this lab, the students are introduced to Cadence integrated circuit design environment, the tool set that will be extensively used in the labs of *CMOS Analog Integrated Circuit Design*. Main contents of this lab include,

- 1. How to log in and log out SUN workstations and some basic UNIX commands.
- 2. Introduction to Cadence Design System for analog integrated circuit design, including, Cadence environment set up, schematic capture, creating symbols, starting analog environment, and circuit simulation with spectreS.

The TA will verify and evaluate your schematic and simulation results. Evaluation sign-up sheets will be available 3-4 days before the due date.

1. Objectives:

- 1. To learn how to use Cadence program.
- 2. To draw a simple inverter schematic with Virtuoso Schematic Composer.
- 3. To simulate the inverter schematic in Analog Environment.
- 4. Plot and view simulation waveforms in Waveform window.

2. Using UNIX Sun Workstations:

1. Log in: The Unix terminals in the Learning Resources Center, ENS 507, are used for the labs. You should have a login account to the system if you are a registered student. Check with the proctors in ENS 507 if you have any problems to log in.

Please choose "Common Desktop Environment (CDE)" when you log in Sun machine. Otherwise, the figures shown in this lab manual may look different. Click "Options" on the login window and go to "Sessions" and choose "Common Desktop Environment (CDE)".

2. Basic UNIX commands: If you need to learn basic UNIX commands, tutorial in the following URL will be more than enough -- http://www.unixtools.com/unixprimer.html. Some basic commands are summarized in the table below.

Commands	Explanation
man command_name	print manual for <i>command_name</i> on screen. Type space to see the
	following pages if one screen can not hold all the information.
	Type 'b' to go back to the previous screen. Type 'q' to quit
	viewing the manual if there are more than one screens. For
	example, you can try "man pwd" for information of command
	"pwd".
pwd	print working directory, print current working directory that you
	are in.

Basic UNIX Commands

cd directory_name	change directory to <i>directory_name</i> . If only "cd" is typed without			
	directory_name, change to your home directory.			
mkdir directory_name	make a new directory named <i>directory_name</i>			
rmdir directory_name	remove directory named <i>directory_name</i>			
1s	list files in one directory. "Is -l" list file information in a long			
	format.			
mv file_name new_file_name	move <i>file_name</i> to <i>new_file_name</i> . It can also be used to move a			
	file to a different directory using "mv <i>file_name directory_name</i> ".			
cp file_name new_file_name	copy file_name to new_file_name. It can also be used to copy a			
	file to a different directory using "cp file_name directory_name".			
rm file_name	remove <i>file_name</i> . Unlike windows, you can NOT recover a			
	removed file. Be cautious when you remove a file. You can add			
	one line (between " and "), "alias rm 'rm -i'", into			
	the .cshrc file in your home directory.			
textedit <i>file_name</i>	start text editor program to edit <i>file_name</i> .			
quota -v	check disk quota.			
command &	Run <i>command</i> in the background.			

3. Log out: If you are using "Common Desktop Environment (CDE)" desktop, click "EXIT" button on the tool bar at the bottom of the desktop.



3. Using the Cadence Tool for IC Design

The Cadence Design System includes several software packages for integrated circuit design, such as, schematic composer, circuit simulators, layout editor, and layout extraction and verification tools. Cadence design framework manages the process for development of analog, digital, and mixed-signal (with both analog and digital) integrated circuits. In this course, we will only use the tools that are involved in analog integrated circuit design. This section has the following contents:

- 1. Introduction to Cadence
- 2. Setting up the Environment
- 3. Starting Cadence
- 4. Library Manager
- 5. Schematic Composer
- 6. Creating symbols

- 7. Starting the Analog Environment
- 8. Simulation in the Analog Environment (DC and transient analyses)
- 9. Plot and view waveforms in waveform window

3. 1. Introduction to Cadence

The Cadence program that we are using is IC 5.0.33 with NCSU_CDK 1.2. Menus are generally customized. We can use CMOS processes available through MOSIS (http://www.mosis.org/) for schematic and layout design. The tools we are going to use in our labs include: 1. Virtuoso schematic composer, 2. Analog environment with SpectreS circuit simulator, 3. Virtuoso layout editor, 4. DIVA - DRC, Extraction and LVS verification tools.

In this lab, we will learn Virtuoso Schematic Composer and Analog Environment with SpectreS circuit simulator. Virtuoso layout editor, DRC, Extraction, LVS verification, and post layout simulation will be introduced in Lab 2.

3.2. Setting up the Cadence Environment

First of all, open the console on the sunfire machine (i.e. sunfire1 or sunfire2)[†].



Then a console window pops up as shown below.

[†] sunfire machines are sunfire1 and sunfire2. sunapp machines are sunapp1, sunapp2, and sunapp3. These are the UNIX application servers at ECE LRC. Different applications, such as web browser netscape and PDF viewer acroread, are available on sunfire servers. You can not start Cadence on sunfire machines. Instead, Cadence should run on sunapp machines. Web browser netscape and PDF viewer acroread are not available on sunapp machines.

-	Console	• •
<u>W</u> indow <u>E</u> dit Options		<u>H</u> elp
Sun Microsystews Inc. SunOS	have been moved to II r sunapp3,	October 2001

As you see on the screen, "all CAD/EDA applications have been moved to the SunApp machines", you have to connect to sunapp1, sunapp2, or sunapp3 machine to start Cadence. Type "ssh sunapp2" in the console command and press <ENTER> to connect to sunapp2 as shown in the following screen snapshot. Please make sure that there is a space between "ssh" and "sunapp2".

If it is the first time you login to sunapp2, you will be asked, "Are you sure you want to continue connecting (yes/no)?" Type "yes" and press <**ENTER**>. Then, you are prompted for your password to access sunapp machine. Type your password and press <**ENTER**>. (Note: Once you answered "yes" from the machine that you are using now, it won't ask you the same question again if you connect to the same machine next time. Instead, you will be directly asked to enter your password.)



Now, you see the console command line prompt changed to "sunapp2%:" showing that you have connected to sunapp2. If you connect to sunapp1 or sunapp3, then the console will display "sunapp1%" or "sunapp3%" instead. Please understand that all of the following commands related to Cadence have to run on sunapp machines. Cadence is not accessible on sunfire machines. Other applications may or may not run on sunapp, but are available on sunfire.

You should create a directory under your home directory called "Analog". Type "mkdir Analog" ("mkdir" is the UNIX command to make a directory) and press <<u>ENTER</u>>. Don't forget the space between "mkdir" and "Analog". Note that an <<u>ENTER</u>> key stroke following the command text is

always needed to execute a command. For simplicity, we will not repeat saying the $\langle \text{ENTER} \rangle$ key stroke after the command line in the following sections. Please add an $\langle \text{ENTER} \rangle$ key stroke at the end of any command line by yourself to execute that command.

Type "chmod 700 Analog" to change the permission of "Analog" directory, thus other students can not see your design files. If you leave your directory open and some one else copied your work, you will have equal responsibility for copying of lab work.

The user settings should be copied from /usr/local/packages/cadence/local/cdssetup directory. There are three files you should copy from that directory, cdsinit, cdsenv, and simrc.

1. The first file is .cdsinit . Type the following command.

```
cp /usr/local/packages/cadence/local/cdssetup/cdsinit ~/Analog/.cdsinit
```

Note: The source file is cdsinit while the destination is .cdsinit (with a leading dot). You can also copy-and-paste the above command line into the console.

<u>Mindow Edit Options</u> Individuals using this computer system without authority, or in excess of their authority, are subject to having all of their	Help
activities on this system monitored and recorded by system personnel. 	
In the course of monitoring individuals improperly using this I system, or in the course of system maintenance, the activities I of authorized users may also be monitored.	
Anyone using this system expressly consents to such monitoring l and is advised that if such monitoring reveals possible l evidence of criminal activity, system personnel may provide the l evidence of such monitoring to law enforcement officials.	
' 	
sunapp2% sunapp2% tosh sunapp2?/home/ecelrc/faculty/slyan>mkdir Analog sunapp2?/home/ecelrc/faculty/slyan>chmod 700 Analog	
sunapp2;/home/ceclrc/faculty/slyan>cp /usr/local/packages/cadence/local/cdss /cdsinit "/Analog/.cdsinit sunapp2;/home/ceclrc/faculty/slyan>	etup

2. The second file is .cdsenv . Type the following command.

cp /usr/local/packages/cadence/local/cdssetup/cdsenv ~/Analog/.cdsenv

3. The last file is .simrc . Copy the file by typing

cp /usr/local/packages/cadence/local/cdssetup/simrc ~/Analog/.simrc

4. Then, revise .cshrc file in your home directory (not "Analog" directory). Add the lines inside the frame on next page into the .cshrc file at your home directory, ~/.cshrc ("~/" is your home directory).

To avoid confusion, you are required to use tcsh shell which probably is not your login shell. To invoke the tcsh shell, type the following command.

tcsh

A sample .cshrc file can be found at (don't forget the leading dit in the file name)

http://www.ece.utexas.edu/~slyan/labs/setup/.cshrc

which is also shown below.

Sample .cshrc file for students in Analog Integrated Circuit Design

```
alias setprompt 'set prompt = "%B%m%b:`pwd`>"'
if ($?prompt) then
    setprompt
    set history = 40
    alias h history
endif
set path = (/bin /usr/local/bin /usr/local/gnu/bin /usr/bin /usr/sbin /usr/bin/X
11 /usr/X/bin .)
```

settings for cadence

```
setenv CDS_LIC_FILE /usr/local/packages/cadence/license.dat
setenv INSTALL_DIR /usr/local/packages/cadence
setenv LM_LICENSE_FILE /usr/local/packages/cadence/license.dat
setenv PATH ${PATH}:/usr/local/packages/cadence/ic/tools/bin:/usr/local/packages/cadence/ldv/tools/simvisdai/bin:/usr/
local/packages/cadence/ldv/tools/verilog/bin:/usr/local/packages/hspice/current/bin
setenv CLS_CDSD_COMPATIBILITY_LOCKING NO
```

settings for NCSU CDK

```
setenv IC $INSTALL_DIR/ic
setenv CDS_SITE /usr/local/packages/cadence/local
setenv USE_NCSU_CDK 1
setenv CDS_Netlisting_Mode Analog
setenv SIMRC /usr/local/packages/cadence/local/skill
```

set prompt = "%B%m%b:`pwd`>"

```
alias ls 'ls -F'
alias ll 'ls -l'
alias rm 'rm -i'
alias cp 'cp -i'
alias cd 'cd \!* ; set prompt = "%B%m%b:`pwd`>"'
```

Your .cshrc file may look very similar to the above example .cshrc file. Just add the framed lines to your original .cshrc file by typing or copy-and-paste. Please be careful that copy-and-paste may cause line misalignment problem. For example, the command started with "setenv PATH \${PATH} ..." appears to have several lines, but they all are in the same long physical line in the file, and are not separated with "RETURN" characters. When you copy-and-paste that command, several "RETURN" characters might be inserted. Correct that problem if it happens.

The following lines are recommended for your .cshrc file.

```
alias rm 'rm -i'
alias cp 'cp -i'
```

If you have the following command aliases, when you delete a file or multiple files using 'rm', you will be prompted "rm: remove file_name (yes/no)?" If you type 'y' or 'yes', the file will be deleted. Otherwise, it will not. Thus you are given the last chance to make a decision whether the file should be kept or deleted . 'cp -i' has the same effect that, you are prompted to decide whether to overwrite a file if you copy a file to an existing file.

Or, if your original .cshrc file is the same as the one given above except the lines for the cadence setup, directly saving the .cshrc file to overwrite the original one could be a better option to avoid copy-and-paste problems. To do this, follow the steps below.

Rename the original .cshrc file to a different file name, such as .cshrc_old, by typing

```
mv .cshrc .cshrc_old
```

In case that you need the original .cshrc file later on, it is still available as .cshrc_old.

You can download .cshrc file from the above link. Before download the new .cshrc that may overwrite the original .cshrc file, please rename your original .cshrc to .cshrc_old.

Start the web browser as shown below from CDE.



Type or copy the link http://www.ece.utexas.edu/~slyan/labs/setup/.cshrc to web browser "Location" field, and press <<u>ENTER></u>.

Save the file by choosing "File \rightarrow Save As", as shown below. A new "Save As..." window appears. You may need to change the location. Confirm the file location and click OK.

			Save As
			Filter
			/home/ecelrc/faculty/slyan/*.cshrd
14		1	
Ċ.	-		Netscape: Directories Files
9	File Edit View	Go	Communicator
d i	New	⊳	🐴 🔥 💉 🖻 🚳 👔 . cdsdoc
V	Open Page	Alt+O	load Home Search Netscape Print Security Shop .dt .gimp-1.2
<	Save As	Alt+S	dion: http://www.ece.utexas.edu/~slyan/labs/setup/.cshrc .java
	Save Frank As		. Mathematica
Æ	Sen <u>d</u> Page		.2 01/16/96(ece.utexas.edu) /usr/share/src/ecelrc/share/usr/local/lib/1
Δ.	Send Lin <u>k</u>		Sh users.
	Edit Page		pt = "%B%m%b: 'pwd'>"/
	Edit Erana		Selection
d.	Upload Flix .		al/bin /usr/local/gnu/bin /usr/bin /usr/sbin /usr/bin/x11 /usr/x/bin .) /home/ecelrc/faculty/slyan/.cshrc
-	Print	Alt+P	
П	<u>C</u> lose	Alt+W	
s	Exit	Alt+Q	OK Filter Cancel
	setenv CDS_LIC_FIL setenv INSTALL_DIP	E /usr/	local/packages/cadence/license.dat ocal/packages/cadence

Now, you have a new .cshrc file in you home directory. If necessary, you can copy some of the command lines from you old .cshrc file .cshrc_old to your new .cshrc file.

Type the following command to load the new .cshrc file to the command shell.

source .cshrc



5. Use any text editor to create ~/Analog/cds.lib. Include the following lines in the cds.lib file.

-- cds.lib example file for Analog Integrated Circuit Design INCLUDE /usr/local/packages/cadence/local/cdssetup/ncsu.lib

Or you can download cds.lib file from http://www.ece.utexas.edu/~slyan/labs/setup/cds.lib,

following the similar steps as above. Save the cds.lib file in your "Analog" directory instead of your HOME directory! Make sure that the path is similar to the one in the screen snapshot below.

F	Filter						
	me/ecelrc/faculty/slyan/Analog/*.lib						
[Directories Files						
	Format for Saved Document: Source						
ę	Selection						
	<pre>>/ecelrc/faculty/slyan/Analog/cds.lib</pre>						
	OK Filter Cancel						

6. Change current directory to "Analog" directory by typing the following command,

cd Analog

Console		1
<u>W</u> indow <u>E</u> dit <u>O</u> ptions	Help	
sunapp22 sunapp22 sunapp22 sunapp22 /nome/ecelrc/faculty/slyan>cp /usr/local/packages/cadence/local/cdss /dsint "/Analog/.dsint sunapp2?/nome/ecelrc/faculty/slyan>cp /usr/local/packages/cadence/local/cdss /dsenv "/Analog/.dsint sunapp2?/nome/ecelrc/faculty/slyan>cp /usr/local/packages/cadence/local/cdss /since "/Analog/.sinc sunapp2?/nome/ecelrc/faculty/slyan>cp /usr/local/packages/cadence/local/cdss sunapp2?/nome/ecelrc/faculty/slyan>cp /usr/local/packages/cadence/local/cdss sunapp2?/nome/ecelrc/faculty/slyan>curce "/.cshrc sunapp2?/nome/ecelrc/faculty/slyan/Analog sunapp2?/nome/ecelrc/faculty/slyan/Analog>	etup	

Type "1s -la" to check if you have these 4 files: .cdsinit , .cdsenv , .simrc , cds.lib .

```
sunfire2:/home/ecelrc/faculty/slyan/Analog>ls -al
total 152
drwx--l--- 2 slyan students 4096 Sep 10 17:23 ./
drwx--s--x 23 slyan students 28672 Sep 10 17:17 ../
-rw------ 1 slyan students 6848 Sep 10 17:23 .cdsenv
-rw------ 1 slyan students 29418 Sep 10 17:20 .cdsinit
-rw----- 1 slyan students 2475 Sep 10 17:23 .simrc
```

Now we are ready to use Cadence tools. Type "icfb &" command. The '&' at the end means we run icfb

at the background.

icfb &

Next time when you run Cadence, type the following commands.

tcsh cd Analog icfb &

3.3. Starting Cadence

You should always start Cadence from the directory that contains the Cadence user setup information. In our case it is your "~/Analog" directory. You can start Cadence by typing the following command (assuming you start from your HOME directory).

tcsh cd Analog icfb&

🔀 icfb - Log: /home/ecelrc/faculty/slyan/CDS.log					
File Tools Options			Help 1		
loading vars from /usr/loc loading vars from /usr/loc loading vars from /usr/loc loading vars from ~/.cdsen Loading avv.cxt	s/cadence/ic5033/tools/plot/.cd	tup/cdsenv for tool sche tup/cdsenv for tool spec tup/cdsenv for tool ui	ematic		
<u> </u>					
mouse L:	М:	R:			

After a short while, a window called "CIW" (Command Interpreter Window) appears as shown above. CIW displays Cadence log file "CDS.log" at your home directory. When you use a specific Cadence tool (e.g. Virtuoso) and run a task (e.g. DRC), most of the times the results will be displayed in CIW. Thus you should check back on this CIW window very often to know what is happening for the tasks that you have initiated.

Your Cadence designs (schematic, layout, ...) are organized in libraries. You can go to menu "Tools \rightarrow library manager" to start the library manager, which usually automatically starts after CIW appears, thus you may not always need to click menu "Tools \rightarrow library manager". How to use library manager will be explained in Section 3.4.

You can read Cadence documents through the Help menu of CIW as shown below. Or, your can type "cdsdoc" (for IC 5.0.33 package) on the command Console of UNIX (not in CIW) to read the documents for all Cadence tools.

😠 icfb - Log: /home/ecelrc/faculty/slyan/CDS.log		
File Tools Options		Help 1
loading wars from /usr/local/packages/cadence/local/cdssetup/cdsenv for	tool	Using the CIW
loading vars from /usr/local/packages/cadence/local/cdssetup/cdsenv for loading vars from /usr/local/packages/cadence/local/cdssetup/cdsenv for	tool	Cadence Documentation
Loading vars from /usr/local/packages/cadence/local/cdssecup/cdserv for Loading vars from /usr/local/packages/cadence/local/cdssecup/cdserv for Loading vars from ~/.cdserv for tool asimenv	tool	Known Problems and Solutions
Loading awv.cxt		Product Notes
Loading /usr/local/packages/cadence/ic5033/tools/plot/.cdsplotinit Loading layers.cxt		What's New
Loading NCSU SKILL routines		DFII Infrastructure
T		Compatibility
mouse L: M: R		About icfb
×		



The above cdsdoc window will appear. Double click the item that you would like to open, or highlight the item, and click "Open" button, you may expand or collapse the document tree, or open the document html webpage in the web browser, such as netscape. You may need to start web browser on sunfire machine before starting 'cdsdoc' command on sunapp machine.

You can open or save PDF version of the documentation by click "View/Print PDF" button in the web browser. You may also find the PDF files in the sub-directories under /usr/local/packages/cadence/ic/doc on sunapp machines. Note that /usr/local/packages/cadence directory is not accessible on sunfire machines. Netscape and acroread (PDF file viewer) are only available on sunfire machines. Thus if you want to read the PDF documentation directly in acroread or other PDF viewer/editor applications, you may have to copy the PDF files from sunapp to sunfire or other computers, and view the files on sunfire or other computers.



3.4. The Library Manager

CIW and Library Manager are probably the two most important and most frequently used windows in Cadence tools. CIW shows the log information; Library Manager helps you to manage your designs which are generally organized in a hierarchy of libraries/cells/cell_views. When you start a design in Cadence for the first time, you have to create a library where you can store your designs (cells/cell_views). Every library is associated with a technology file that supplies all the color maps, layer maps, design rules, extraction parameters required to view, design, simulate and fabricate your design.

1. Starting Library Manager

The Library Manager usually automatically starts after CIW window appears. In case that the library manager has not started, or accidentally was closed, go to CIW window, click on "Tools \rightarrow Library Manager". Library Manager looks like the window at the left (see next page).

- 2. Create a new library
- In Library Manager window, click on "File→New→Library..."

A dialog window pop up, as shown in the right. At the "Name" field, enter the name of the library that you want to create, in our case "Lab1", to store your design cells.

🔀 Library Manager: Directoryects/	slyan/shouli/teach/Analog			
<u>File Edit View D</u> esign Manag	ler		<u>H</u> elp	
Show Categories Show I	Files			
Library	Cell	View		
L	Ĭ	L		
NCSU_Analog_Parts NCSU_Digital_Parts				X Library Manager: Directoryects/slyan/shouli/teach/Analog
NCSU_Sheets_8ths basic				File Edit View Design Manager
cdsDefTechLib				New Library
				Open (Read-Only) ^r Category
J				Save Defaults
- Messages				Open Shell Window ^p
Loading NCSU Library Manager Log file is "/home/projects/s	customizationsdone. lyan/shouli/teach/Analog/libMana	ıger.log".		CdsDefTechLib

Attach this library to an existing technology (example shown: AMI 0.6 µm technology) by clicking the radio button "Attach to existing tech library -->" and choosing "AMI 0.60u C5N (3M, 2P, high-res)", thus the Cadence tools would know the technology information of your design (like SPICE models, DRC rules, ERC rules, etc.). Please do not enter or change any other fields or options.

🔀 Crea	te Library	/				x
ок	Cancel	Apply				Help
Library						
Name	: Labl	4				
Path:	Ĩ					
Techno	logy Libi	ary				
Other		ou must		n (i.e., layout) data you do not nee sting tech library or compile one.	d a tech library.	
	⇔No te	ch libra	y needed			
			sting tech library	AMI 0.60u C5N (3M, 2	2P, high-res) =	
	🔷 Comp	ile tech	library			
Misc.						
	I/O Pa	d Type:	🔶 Perimeter 🔷	rea array		

<***For information only***> You can also use "compile tech library". This creates a local copy of the technology library in your run directory, thus it is not very efficient in the sense that, every user has a copy of an identical tech library, and if there is any change made to the main technology library, each user has to update his copy of the compiled tech library. Because of these two reasons, we prefer "attach to existing tech library" to "compile tech library".

Now your library manager window should look like,

🔀 Library Manager: Directoryec	ts/slyan/shouli/teach/Ar	nalog	_ 🗆 ×			
<u>File</u> Edit <u>View</u> Design Ma	nager		<u>H</u> elp			
🔲 Show Categories 🛛 🔲 Sho	w Files					
Library	Cell	View				
Lab1	I	Ĩ				
Lab1 NCSU_Analog_Parts NCSU_Digital_Parts NCSU_Sheets_8ths NCSU_TechLib_ami06 basic cdsDefTechLib						
Messages						
Loading NCSU Library Manager customizationsdone. Log file is "/home/projects/slyan/shouli/teach/Analog/libManager.log".						

You have not only created a library "Lab1" of your own, but also included its associated technology library "NCSU_TechLib_ami06" in your library path.

3.5. Editing Schematics Using Virtuoso Schematic Composer

At this point, you have created a library (in the example "Lab1") to store your design and can start the design process. For a full custom design, we start from creating a schematic. Then we simulate this design to verify its functionality and analyze its behavior to optimize the performance. After that we will do layout of the design. Layout will be introduced in Lab 2.

You can usually initiate a command in Cadence Schematic Composer and Layout Editor in three ways, (1) choosing a menu from the top menu bar; (2) clicking a button on the left toolbar of the window, or (3) pressing a *hot key*. All of three will give the same results. You can choose what you feel most convenient. For example, to add an instance, you can choose "Add \rightarrow Instance ..." from the menu bar,

or you can click the button if from tool bar at the left side of the window, or you can simply press the hot key "i" from the keyboard.

Function	Hot key	Menu	Tool button
Check and save	F8	Design \rightarrow Check and Save	
Save	F2	Design \rightarrow Save	
Add instances	i	Add \rightarrow Instance	Q
Edit properties	q	Edit \rightarrow Properties	

1 .Hot keys, menus, and tool buttons

Add wires	W	Add \rightarrow wire (narrow)	
Label a wire	1	Add \rightarrow Wire Name	abc
Delete (a pin, label, wire, instance)	DEL	Edit → Delete	34
Add a pin	р	Add → Pin	•
Undo	u	Edit → Undo	
Zoom in	Z	Window \rightarrow Zoom \rightarrow Zoom In	
Zoom in by 2X	^ _Z	Window \rightarrow Zoom \rightarrow Zoom In By 2	€ ²
Zoom out by 2X	Z	Window \rightarrow Zoom \rightarrow Zoom Out By 2	୍ଦ୍
Fit the schematic	f	Window \rightarrow Fit	

2. Creating a new schematic

In your Library Manager window, click on the "File \rightarrow New \rightarrow Cellview". A pop-up dialogue window appears. Click on the library name button and select "Lab1". Click on the "Tool" button to select "Composer-Schematic". The "View Name" will automatically change to "schematic". Enter the name of the cell you wish to design in "Cell Name". For this lab, we will design a CMOS inverter, with the cell name of "Inverter". Click "OK" after you type in the cell name.

🔀 Library Manager: Di	ectoryects/s
<u>File E</u> dit <u>V</u> iew	<u>D</u> esign Manage
New	🕑 Library
juen Juen (Read-Only)	Cell View.
ve Defaults	
en Shell Window	^p
t Tomashták szálo	^ <u>x</u>
SU_TechLib_amiO6 sic)
lsDefTechLib	

An empty schematic edit window will appear as shown below.



In the following steps, we will learn how to create an inverter schematic.

3. Adding an instance

To place an instance, e.g. an NMOS device, in your schematic, activate the schematic window, then click on menu "Add→Instance" (or type "i" hot key, or click on the left side tool bar). The "Add Instance" dialogue box appears together with the "Component Browser" dialogue window. In case the "Component Browser" window does not appear, click on the "Browse" button in the "Add Instance" window to start it.

🔀 Virtu	😿 Virtuoso® Schematic Editing: Lab1 Inverter schematic									
Cmd	l:		Se	el: O						
Tools	Desigr	n V	Vindow	Edit	Add Check Sheet	Optio	ns	NC	SU	
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Component Browser Commands Librar NCSU_Analog_Parts Flatten Filter Uncategorized	4 Commands Help	Image: State
CONTENTS Current_Sources Diodes H_Spice_Only Microwave_Parts Misc_Parts	nbsim nbsim nbsim4 njfet nmes4 nmos	Rotate Sideways Upside Down Model name ami06N
N Transistors P_Transistors Parasitic_Devices R_L_C Spectre_Only	Innos4 nunos4 nv nunos hv npn usernpn N_Transistors	Model Type ♦ system ◇ user Multiplier 1. Fingers 1. Width (grid units) 10.

In "Component Browser" window, click on "Library" multi-selection button and choose "NCSU_Analog_Parts". Click on "N_Transistors" and choose "nmos4" as your NMOS device (Note

that "nmos4" has 4 terminals. While "nmos" only shows 3 terminals, drain, gate, and source. The bulk terminal is hidden, and is specified in the properties window to a certain wire name through the wire label /name. Use of "nmos4" is encouraged to avoid some hidden mistakes. To place the instance, activate the schematic window and click the left mouse button to put the instance at the place desired.

Note in Cadence schematic composers and layout editors, a command will not terminate unless the user cancels or starts a new command. In this case, you can see another instance is ready to be placed right after you placed the first instance. To terminate the current operation (which is "Add Instance" in this

case), press $\langle ESC \rangle$ key on the keyboard. In fact, you can always cancel the current operation in schematic or layout editors by pressing $\langle ESC \rangle$ key.

4. Setting the properties

To set the properties of the instance that you just placed, or any object in your schematic or layout design, select the object by clicking on it and then go to "Edit→properties→Object..." (or by typing "q" hot key). An object properties editing form will pop up. The following is the properties window of an NMOS Transistor. Change the "Width", "Length", and "Multiplier" properties to "Width"=6u, "Length"=0.6u, and "Multiplier"=2, as shown in the right side window snapshot. Keep other parameters unchanged.

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synnn								

In a similar manner, we can add an instance of PMOS

transistor. Set the properties of the PMOS transistor as, "Width"=6u, "Length"=0.6u, and "Multiplier"=4.

Note that in the "Edit Object Properties" window, "Apply to" multi-selection button shows "only current". If you want to change the properties of multiple instances at the same time, you may highlight multiple instances first, and change "Apply to" multi-selection button to "all selected", change the properties in the properties list, and confirm the change by click "Apply" or "OK" button at the top of the "Edit Object Properties" window. The properties of all highlighted instances are changed to the same set of values. The difference between "Apply" or "OK" is that, if you click "Apply" button, the properties in the list will be applied, but the "Edit Object Properties" window remains open for further action; if you click "OK" button, the properties will be applied, and the "Edit Object Properties" window closes. You can always cancel current change and close the window by clicking "Cancel" button. You can clear the entire properties and set to default values (usually bank or empty fields) by clicking "Default" button.

<***For information only***> You may find "Apply", "Previous" and "Next" function buttons useful when you highlight multiple objects and change the properties of the instances one after another.

Note that you can also change of the properties of the device in the "Add Instance" window as show previously while you place the instance.

5. Wiring the instances

To connect the PMOS and NMOS devices or any other devices, click on "Add \rightarrow Wire (narrow)" in the schematic window (or type "w" hot key). Click on the terminal where the wire starts, and then click at

the terminal where the wire ends, a wire will be automatically added. If you are not satisfied with the automatic wiring, you can remove the wire by selecting the wire and press <<u>DEL</u>> key. The reroute it manually. This time, instead of directly clicking on the terminals where the wire starts/ends, you can click the left mouse button wherever you want to confirm the suggested wiring shown in yellow color.



If you want to stop the wire somewhere empty instead of connecting it to a terminal, double click your left mouse button and a dangling wire is created. In general dangling wire should be avoided. However, in some cases, for example, if you want to label this wire or add a pin to this wire, a dangling wire makes sense.

<***For information only***> Click on "Add→Wire Name..." (or type hot key "l" – the lower case of "L" not a number "1") in the schematic window, the following dialogue box would appear. You can specify a name for each wire, but we generally only add labels for those wires that you may have interest to see signal voltages in simulation, or the wires that you may want to connect with the same wire label, or the global wires like VDD or VSS. An "!" denotes a global wire name, such as "VDD!" and "gnd!". Global wires are not encouraged in most cases, like global variables are not often used in software programming practice. If you specify the positive and negative power supplies of a cell (such as an inverter or an amplifier) to "VDD!" and "VSS!", it is not flexible if you want to connect the cell to different power supplies other than "VDD!" and "VSS!".

6. Creating pins

Click on "Add \rightarrow Pin..." (or type hot key "p") in the schematic window, "Add Pin" window would appear.

We have to specify its input/output behavior for each pin.

For an input pin, choose the "Direction" to be "input". Specify the "Pin Names" ("Vin" in the example). Activate the schematic window and click the left mouse button to place the pin in the schematic.

🔀 Add Pin	1				×
Hide	Cancel	Defaults			Help
Pin Name	s	VirĮ			
Direction		input	- Bus Expa	nsion 🔶 off <	on
Usage	5	schematic	Placemer	it 🔷 🔶 single	🔷 multiple
Rotati	e		Sideways		Upside Down

Similarly we can add an output pin ("Vout" in the example) to the output of the cell. The "Direction" of "vdd" and "vss" pins are specified as "InputOutput".

Please note that Cadence automatically labels internal nodes, usually you don't have to explicitly label them.

7. Check and save the design

After the design has been completed, click menu "Design→Check and Save" to check and save your design. Go to the CIW window to see if there is any error in your design. The following schematic shows the completed design of the inverter. Use the widths, lengths, and multipliers of the transistors given in the following screen shot.

You can save the design (without checking) by

```
clicking "Design→Save", or clicking
```

button, or pressing hot key <F2>. Saving the design frequently is encouraged to avoid loss of work due to unexpected reasons, such as loss of power, network failure, and etc.

3.6. Creating Inverter Symbol

Symbols are useful when the schematic design is done hierarchically. At a higher level of abstraction, we would like to use a symbol to replace the schematic details of a cell. The symbol of a schematic cell should define all the inputs and outputs of that cell.

There are two ways to create a symbol. If you already have a schematic design, you can create its symbol right from the cell. If you don't have a schematic design yet or you want to manually create a symbol for the cell, you can start from scratch manually.

In this section, we introduce how to create a symbol from schematic cell view.

Click on "Design \rightarrow Create Cellview \rightarrow From Cellview" menu in the schematic edit window, a pop up dialogue box will appear.



🕻 Virtu	ioso® Schematic Editing:	Lab1 Inverter schematic
Cmd	l: Sel: O	
Tools	Design Window Edit	Add Check Sheet Options
	Check and Save	- f8
Y	Save (not needed)	f ² vdd 🔶 -
۲	Save As	f3
	Hierarchy	
€ ²	Create Cellview	From Cellview
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We can use the default setup in this window, thus click "OK". The symbol edit window will appear that contains a default symbol created automatically by Cadence. It has a red box that encloses the green colored inverter symbol. This red box defines the actual size that a symbol will occupy in a parent schematic. Even though you can change the size of this red box to an arbitrary size, it is preferred to exactly fit the symbol within the red box. The small red squares indicate the pins. [@InstanceName] and [@PartName] are display variable holders for instance name (such as "I0") and part name (such as "Inverter") when the inverter symbol is placed in a parent schematic. The following figure shows the symbol.

🔀 Virtu Cmd		mbol Editi Sel	_	b1 In	verter sy	ymbol					_	
Tools	Design	Window	Edit	Add	Check	Option	ıs					Help
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<i>3</i>	Mouse L	:			M :			R:				

If you don't like this rectangular symbol that is automatically created by the tool, you can edit it or create a symbol of your own. In the following paragraph, we will explain how to edit a symbol.

When the pointer is moved to above the rectangle, a yellow dashed rectangle appears along with the green rectangle as shown in the following figure. The yellow dashed rectangle indicates the object under the focus of the pointer. If you click the left mouse button, the object under focus will be selected and highlighted. Highlight and select the green rectangle by clicking the left button. Press key to delete it.

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If you press and hold the left mouse button and move the pointer, a yellow rectangle will appear. Any objects inside of the yellow rectangle will be selected (highlighted) when you release the left mouse button. Select (and highlight) the Vss pin.

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				tance	
		(@partName)	· ·		
	<u> </u>				

Select "Edit \rightarrow Move" or press the hot key "m", the following window will appear. Click "Rotate" button twice. Note that you may not see the button is pressed if you click too fast. Move the pointer the symbol edit window and click the "vss" pin, you may see as the following figure.

	Move	×
[@instanceName] · · · · · · · · · · · · · · · · · · ·	Hide Cancel	Help
Vin v 🖗 partName] Vout ——• · · · ·	Snap Mode anyAngle =	
	Rotate Sideways	Upside Down

Move the vss pin to wherever you like, and click the left mouse button, the vss pin is dropped to the new location.

Choose menu "Add \rightarrow Shape \rightarrow Line" or click the tool bar icon \square , and draw a triangle. Choose menu "Add \rightarrow Shape \rightarrow Circle" to add the small circle of the inverter. Move the pins, triangle, and the small circle, if necessary, by selecting and moving them one by one. Resize the red rectangle if necessary by

choosing menu "Edit \rightarrow Stretch" or by clicking the tool bar icon \square , and stretch one side of the red rectangle. You finally have a symbol as shown below.

Vin (@partName]

3.7. Create Inveter_tst Schematic Cell

Create another schematic cell, "Inveter_tst", to test the inverter that we just created.

Following the procedures to create "Inverter" schematic, create a new schematic "Inveter_tst". In the new "Inveter_tst" schematic editing window, create an instance of the inverter by choosing menu

"Add \rightarrow Instance". Component Browser window appears, and choose "Lab1" library and "Inverter" cell, as shown in the right figure. Place the inverter symbol in "Inveter_tst" schematic.

Similarly, place positive power supply source Vdd, negative power supply source Vss, and input voltage

source of the inverter, Vin. Vdd and Vss are "vdc" cell from NCSU_Analog_Parts library. Both Vdd and Vss have a DC voltage of 2.5V. Please pay attention to the polarities of the supply voltages. Vin is "vpulse" cell from NCSU_Analog_Parts library. Specify parameters of Vin as shown in the properties window in the right.

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			Ad	d	Delete	Modify	
	User F	roperty	Mas	ster Value		Local Value	Display
	lvsign	ore	TRUE		Ĭ.		off =
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AC ma	gnitude		I				off =
AC ph	ase		Ĭ.				off 😑
Voltag	je 1		-2	.5 V			off =
Voltag	e 2		2.	5 V <u>í</u>			off 😑
Delay	time		1r	i sį			off =
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Fall tir	ne			0.0p 🧃			off 😑
Pulse	width			5n s			off =
Period				n đ			off =
DC vo	Itage		0	¥.			off 😑
	file name				_		off =

Add R0 and C0 as the load resistor and capacitor of the inverter.

We choose $R0 = 100 \text{ k}\Omega$, and C0 = 1 pF. Both of them are from NCSU_Analog_Parts library.

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Commands

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Help 12

Lab1

All components are summarized in the table below.

Instance Name	Library	Category	Cell	Comments
IO	Lab1		Inverter	
X 7:	NCCLI Analas Danta	Maltara Campaga	Varia	Properties in the above
Vin	NCSU_Analog_Parts	Voltage_Sources	Vpulse	figure.
Vdd	NCSU_Analog_Parts	Voltage_Sources	vdc	DC voltage = $2.5V$
Vss	NCSU_Analog_Parts	Voltage_Sources	vdc	DC voltage = $2.5V$
R0	NCSU_Analog_Parts	R_L_C	res	Resistance = $100 \text{ k}\Omega$
C0	NCSU_Analog_Parts	R_L_C	cap	Capacitance = 1 pF

Wire the components together. The Inveter_tst final schematic looks like below.

<***For information only***> You may find the Composer Tutorial from Cadence useful at /usr/local/packages/cadence/ic/doc/comptut/comptut.pdf on sunapp machines.



3.8. The Analog Environment

1. Preparing the model files for simulation

The simulator we will use will be specterS. Before proceeding further, we need to copy the model files for the NMOS and the PMOS transistors to ~/cadence/models/spectre directory. By default the spectreS simulator searches device models in that directory.

Create ~/cadence/models/spectre if the directory does not exit. Note that "~" is your HOME directory. If you are not sure how to create ~/cadence/models/spectre directory, follow the following procedures. (1). Type "cd" in your UNIX shell command line to change current directory to your home directory. (2). Create ~/cadence directory by typing "mkdir cadence" if you do not have ~/cadence. (3). Type "mkdir cadence/models" to create ~/cadence/models directory. (4). Type "mkdir cadence/models/spectre" to create ~/cadence/models/spectre directory.

The CMOS technology that we use is AMI 0.6u. The NMOS and the PMOS model files are named as ami06N.m and ami06P.m respectively. You can view the properties of NMOS and PMOS transistors in schematic Inverter (cell Lab1/Inverter). Note that the "model" properties of NMOS and PMOS are ami06N and ami06P respectively.

Download the ami06N.m and ami06P.m files from the following http links.

Ami06N.m at http://www.ece.utexas.edu/~slyan/labs/setup/ami06N.m

ami06P.m at http://www.ece.utexas.edu/~slyan/labs/setup/ami06P.m

You can download the model files using *netscape* web browser on sunfire machines, as shown below.

Save the ami06N.m file as ~/cadence/models/spectre/ami06N.m by choose "File \rightarrow Save As ...", choose the ~/cadence/models/spectre directory in the "Save As ..." window as shown below.

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	Filter	_
× Netscape:	<pre>ne/ecelrc/faculty/slyan/cadence/models/spectre/*.</pre>	тį
File Edit View Go Communicator	Directories Files	
Image: Second		
Back Forward Reload Home Search Netscape Print Security Shop		
👔 🏹 Bookmarks 🧔 Location: [http://www.ece.utexas.edu/~slyan/labs/setup/ami06N.m		
* Run: t3af TT * Vendo:: AWI 0.5 * Date: 12 / 03 / 2003 .00027. sal06N MNOS (LEVEL=11 & TOOT: 27 & TOOT: 1.4IE-8 & XJ=1.5E-7 &	Format for Saved Document: Source Selection slrc/faculty/slyan/cadence/models/spectre/ami06N.	
NOTE:1.7217 & VITH0=0.8374355 & X1=0.03935503 & X2=-0.1024413 & X2=-0.1024413 & X3=-8.3345333 & VI=12=6 & \\ VI=12=6 & \\ VI=12=	OK Filter Cance	

Repeat the above procedures to save the ami06P.m file as ~/cadence/models/spectre/ami06P.m .

We will open Analog Environment to simulate Inveter_tst schematic. We will specify the outputs to be saved, and you will also specify analysis types, do simulations, and plot the simulation results in the waveform window.

2. Starting the Analog Environment from schematic window

In the Inveter_tst schematic editing window, choose menu "Tools \rightarrow Analog Environment".

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Analog Design Environment window will appear.

	nvironment (1)	
Status: Ready T=25 C Simulator: hspiceS Session Setup Analyses Variables Outputs Simulation Results Tools Help Design Analyses Library Lab1 # Type Arguments	S 4	
Session Setup Analyses	Variables Outputs Simulation Results Tools	Help
Design	Analyses	÷Ę
	# Type Arguments Enable	TRAN
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Design Variables	Outputs	[]‡√
# Name Value	# Name/Signal/Expr Value Plot Save March	se la compañía de la
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3. Selecting the simulator

In the Analog Design Environment window, choose menu "Setup \rightarrow Simulator/Directory/Host ...". Simulator/Directory/Host setup window appears and set "Simulator" as "specterS" as shown in the following window screen snapshot.

🔀 Cadence® Analog Desig	n Environment (1)			_ 🗆 ×
Status: Ready			T=25 C Simulator:	
Session Setup Analyse	s Variables Ou	tputs Simulation	Results Tools	Help
Design		Analy	292	-7
Simulator/Pirec				ž
Library L Temperature		Arguments	Er	hable JAC
Cell I Model Path Model Corner				- DC
View s Environment				T T Z
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Des Simulation Files		Outp		Ē
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OK Cancel	hspiceS spectre			Help
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Project Directory	hspice SVerilog	ulation		
Host Mode	spectre SVerilog spectre Verilog	ote 🔷 distributed	I	
Host				
Remote Directory				

4. Setting the model search paths

Now we will set the model directory, thus the Analog Design Environment can find the model files for simulation. In the Analog Design Environment window, choose menu "Setup \rightarrow Model Path". The following window appears. Note that ~/cadence/models/spectre, the directory we used to store the model files, is the first item in the "Directories". Note that in the Inverter schematic, the "Model name"

in the Properties Window of the NMOS and PMOS transistors is "ami06N" and "ami06P". When simulating the schematic, the Analog Design Environment will search "ami06N.m" and "ami06P.m" starting from the first directory listed in the "Directories" in the "Setting Model Path" window, until the right model files are found or the last directory in the "Directories" list has been searched.

🔀 Setting Model F				nt (1)
OK Cancel I	Defaults App	ly Apply & Ru	n Simulation	He
Directories				nce/models/spectre al/models/spectre/public
New Directory	I	e Add Below	Change Dele	

5. Choose analysis (simulation) types

DC Analysis

In the Analog Design Environment window, click menu "Analyses→Choose…", the Choosing Analysis window will appear. Following the following steps:

- (1) Click "dc" radio button in the "Analysis" section.
- (2) In the "DC Analysis" section, select "Save DC Operating Point" button.
- (3) Click "Component Parameter" button in the "Sweep Variable" section.
- (4) Click "Select Component" button.
- (5) The schematic window rise up, click the input voltage source Vin.
- (6) A new window, Select Component Parameter window, appears as shown below in the right. Click "dc – vdc – DC voltage" line.
- (7) Click OK of the Select Component Parameter window. In the Choosing Analysis window, "Component Name" text field will be filled as "/Vin" and "Parameter Name" text field shows as "dc". You can also save steps (4) to (6) and type directly "/Vin" in the "Component Name" text, and "dc" in the "Parameter Name" text field.
- (8) In the "Sweep Range" section, click "Start-Stop" button. Specify -2.5 as "Start" and 2.5 as "Stop".
- (9) In the "Sweep Type" section, "Automatic" is selected by default. You can change to "Linear", and specify the "Step Size" as 10m (V).

😿 Choosing Analyses Affirma Analog Circuit Design Environment 🔀			
OK Cancel Defaults Apply Help	🔀 Virtuoso® Schematic Editing: Lab1 Inverter_tst schematic Cadence® An		
Analysis 🔷 tran 🔷 ac 🔷 sp 🔷 pdisto 🔷 spss	Cmd: Sel: 0 Status: Ready		
🔶 🔶 🕹 xf 🕹 pss 🕹 noise	Tools Design Window Edit Add Check Sheet Options NCSU		
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Sweep Variable Temperature Component Parameter Model Parameter	€ ² C ² Vin Vin Vin Vout tot		
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	🖋 1 1 1 1 2 1 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	dc vdc	"DC voltage"
Sweep Type	\frown	mag acm phase acp	"AC magnitude" "AC phase"
Automatic 🖃	N VSS	phase acp tc1 tc1	"Temperature coefficien
		tc2 tc2	"Temperature coefficien
Add Specific Points 🔲		tnom tnom	"Nominal temperature"
Enabled Detions			
chanta – Opuona	> Select component		

After the above steps, the Choosing Analysis window will look like,

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OK Cancel Defaults App	ily I	Help
Analysis ↓ tran ↓ ac ♦ dc ↓ xf	· · · · ·	
DC	Analysis	
Save DC Operating Point		
Sweep Variable Temperature Component Parameter Model Parameter	Component Name //Virď Select Component Parameter Name dď	
Sweep Range	Parameter Name dd	
◆ Start-Stop ◇ Center-Span Start	-2.5j Stop 2.5j	
Sweep Type	 ♦ Step Size ↓ Total Points 	
Add Specific Points 🗌		
Enabled	Options	

Click "Apply" button to apply (save) the change.

Transient Analysis

Following the following steps to specify transient analysis options in Choosing Analysis window.

- (1) Click "tran" radio button in the "Analysis" section.
- (2) In the "Transient Analysis" section, type "100n" as the "Stop Time".
- (3) Click "conservative" button as the "Accuracy Defaults (errpreset)".

Choosing A	nalyses	Cadence) Analog De	esign Environment (1) 🗴
OK Can	el Defau	ts Apply			Help
Analysis	♦ tran ◇ dc	⇔ac ⇔xf	⇔sp ⇔pss	◇pdisto ◇sps ◇noise	S
		Transient	Analysis		
Stop Time	100n				
Accuracy I) te 🔄 libera	શ	
Enabled 📕				Options	

Click "OK" button to apply (save) the change and close the Choosing Analysis window.

6. Specify the outputs to be saved

In the Analog Design Environment window, choose menu "Outputs \rightarrow Save All ...". The Save All window pops up as shown below. The option button of "Select all node voltages" is on by default. Click "Select all DC/Transient terminal currents" option button to select it. Click OK button to save the change and close the window.

🔀 Cadence® Analog Design E	wironment (1)		
Status: Ready	T=27 C Simulato	Keep Options	
Session Setup Analyses		OK Cancel Defaults Apply	
Design Library Lab1 Cell Inverter_tst View schematic	Setup Nyses Delete 3 1 dc To Be Marched 5.5 2.5 2.5 Save All	Select all node voltages Select all DC/Transient terminal currents Select all AC terminal currents (useprobes)	
Design Variables	Outputs	Save All AHDL Module Variables	

<u><***For information only***></u> Or you can choose "Outputs \rightarrow To Be Plotted \rightarrow Select from Schematic" and then the schematic window will rise up and becomes active. Click a wire to select a voltage ouput and a device pin to select a current output, when finished hit <ESC>.

7. Run simulations

The Analog Design Environment window should look like the following snapshot. You can start simulation by selecting menu "Simulation \rightarrow Run" or simply clicking the button if at the right side of the Analog Design Environment window.

Status: Ready	T=27 C Simulator: spectre	s 7
Session Setup Analyses	Variables Outputs Simulation Results Tools	Help
Design	Analyses	۲Ļ
Library Lab1	# Type Arguments Enable	J AC
Cell Inverter tst	1 tran 0 100n cons yes	⇒ DC
view schematic	2 dc t -2.5 2.5 10myes	T T Z
Design Variables	Outputs	
# Name Value	# Name/Signal/Expr Value Plot Save March	3
		8
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Check the CIW window for the simulation log information.

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File Tools Options		Help
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8. Waveform window

View/plot simulation results

You can plot the simulation results in Waveform window through the following steps.

- (1) Choose "Results → Direct Plot → DC" or "Results → Direct Plot → Transient Signal".
- (2) The schematic window rise up. You can plot a voltage waveform by clicking a net and/or a current waveform by clicking the pin of a component. After you have selected all the voltages/currents, press <ESC> key.

If you use "Outputs \rightarrow To Be Plotted \rightarrow Select from Schematic", after successful simulation, the required signals are automatically plotted.

The following figure show inverter supply current and output voltage, with input voltage swept from -

2.5V to 2.5V. The waveform can be obtained by choosing "Results \rightarrow Direct Plot \rightarrow DC" and selecting the output voltage of the inverter and the current through "vdd" pin (the small red square) of the inverter.



The input/output voltages of the inverter in the transient simulation are shown below. The waveform can be obtained by choosing "Results \rightarrow Direct Plot \rightarrow Transient Signal" and ...



Some useful commands of the waveform window	/
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Function	Hot key	Menu	Tool button	
Fit all	f	Zoom → Fit		
Zoom in	Z	Zoom → Zoom In		
Zoom out	Z	Zoom → Zoom Out		
Marker A	а	Markers $ ightarrow$ Crosshair	* *7	
		Marker A		
Marker B	b	Markers $ ightarrow$ Crosshair	air 🗸	
		Marker A		
Switch axis mode				
Open calculator		Tools →		
window		Calculator…		
Print hard copy		Window → Hard		
		Сору		
Update/redraw the	Window → Update			
waveform(s) from	Result			
the simulation				
output data *				

* Waveform window will not automatically update the waveform if you have re-run the simulation (with possibly changed schematic parameters).

Last updated on Feb. 11, 2006

References:

[1] ELEN474 Analog Integrated Circuit Design Lab Manual, Texas A&M University, 1998

[2] Cadence on-line documentation, command "cdsdoc" in UNIX shell.