CycleSim: A Phase-Locked Loop Simulator

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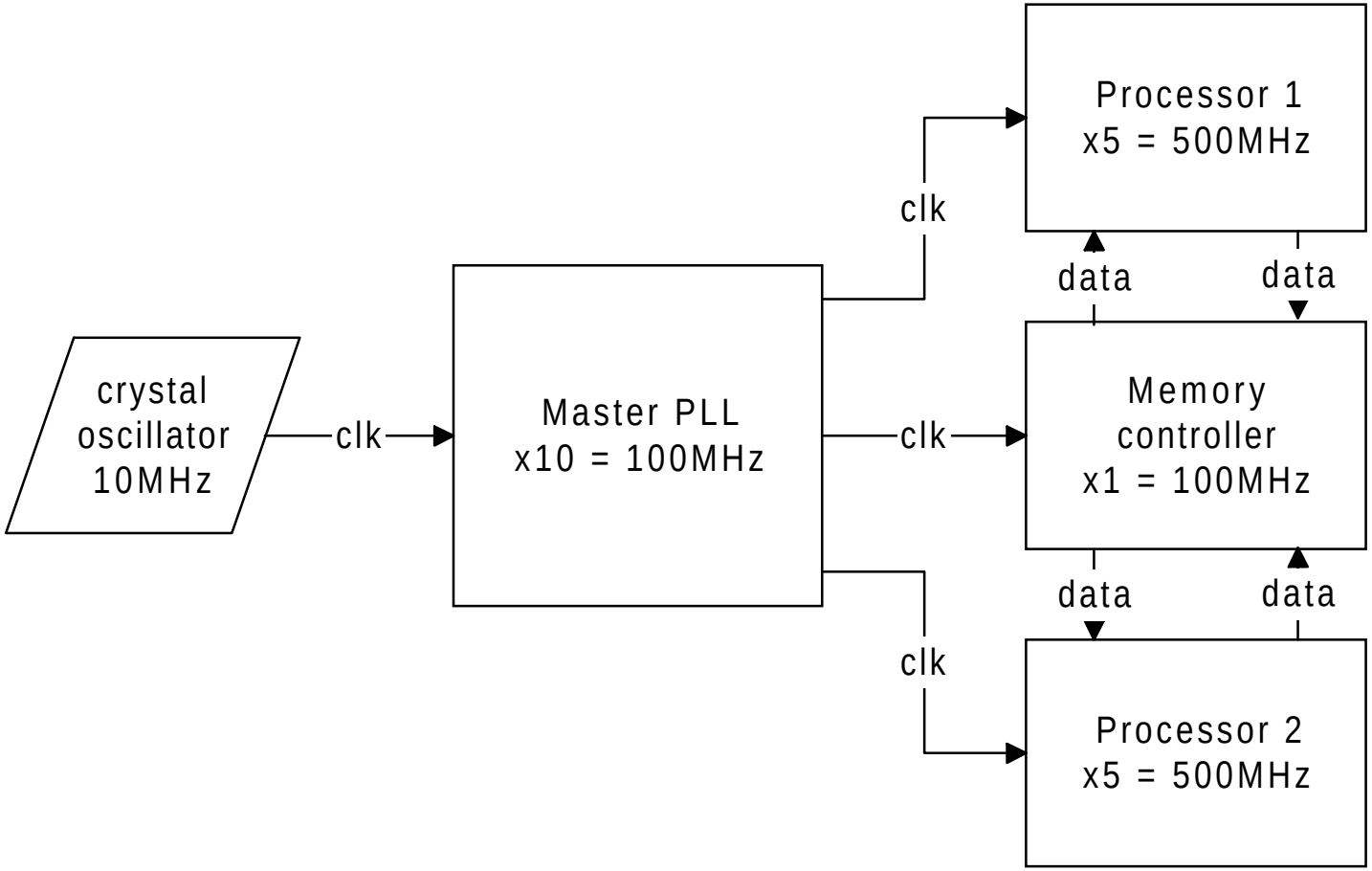
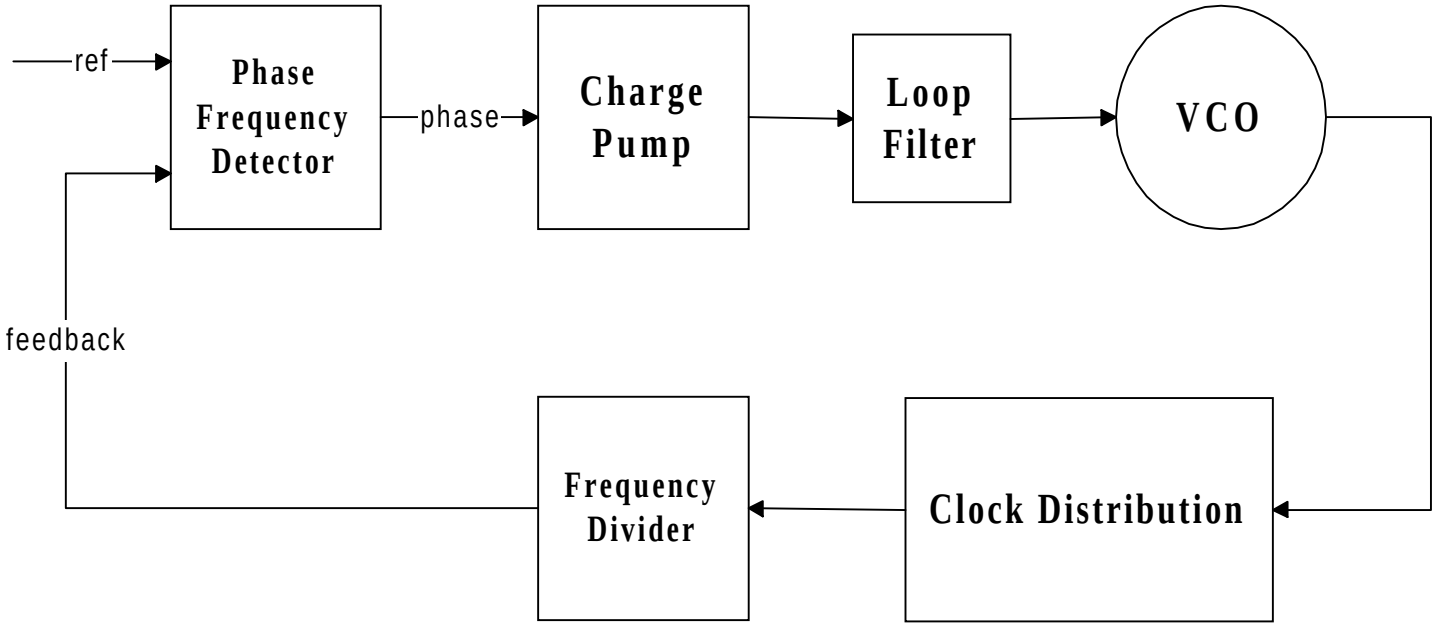
Phase-Locked Loop (PLL) Primer

- Used for clock generation/distribution in computers
- Capable of frequency multiplication and phase alignment of clocks
- Can be implemented as a separate clock chip or internal to a microprocessor, ASIC, etc.

Clock Distribution Example



- PFD (phase-frequency detector) generates up or down pulses depending on whether the feedback is leading or lagging the reference. The pulse is proportional to the phase difference
- Charge pump converts the pulses to current and pumps the filter up or down.
- The VCO (voltage-controlled oscillator) uses the voltage on the filter to control its frequency
- The divider frequency divides the clock



PLL Performance

- Cycle-to-cycle and period jitter (clock accuracy)
- Long-term jitter
- Loop bandwidth
- Must be independent of multiplier

Current methods of PLL simulation

Tool	Domain	Pros	Cons
SPICE	time	accurate	slow for PLL sims; too much data
EESof	frequency	fast	accuracy; difficult to model
Analytical	s-domain z-domain time	fast	not accurate

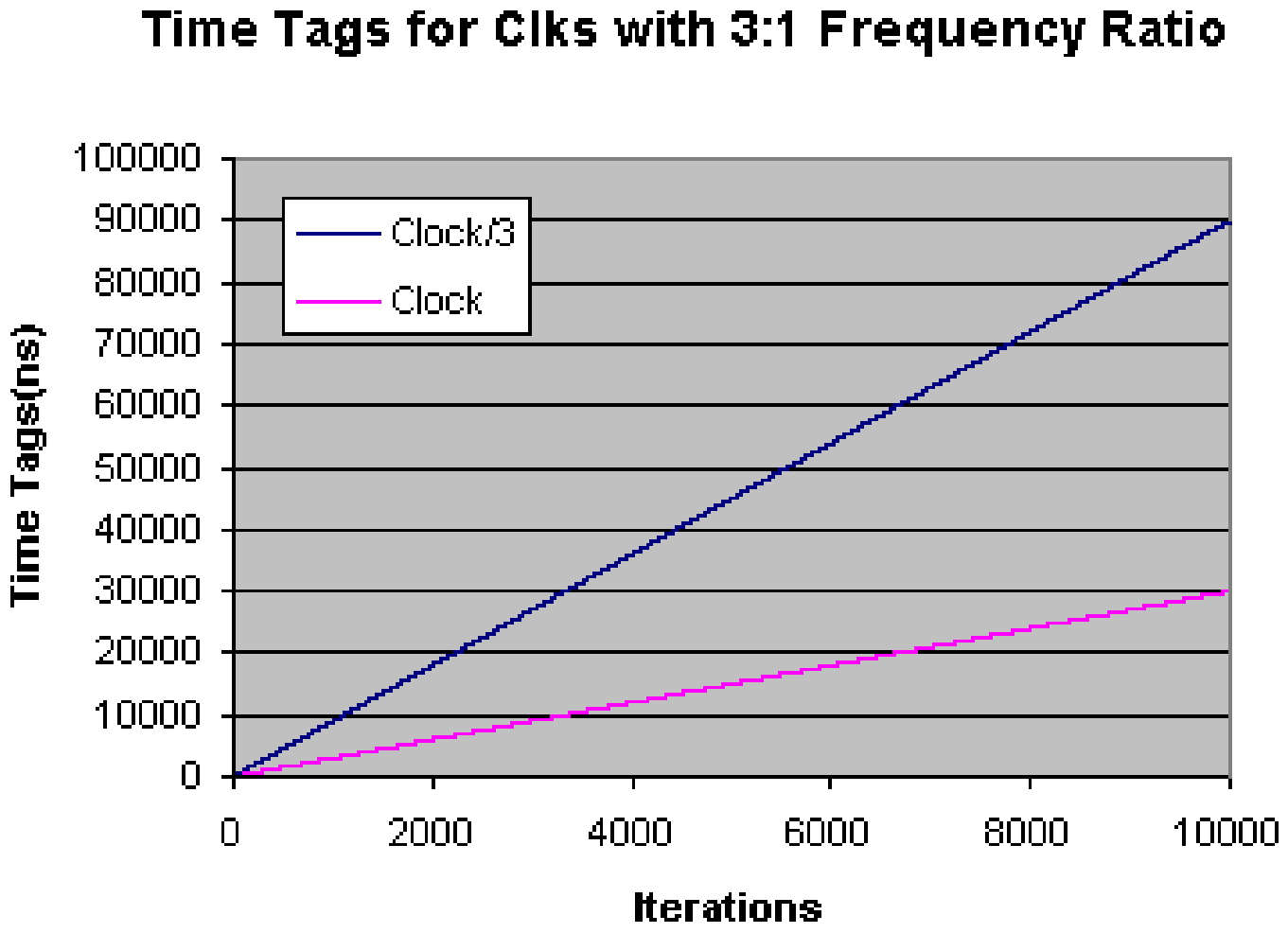
More on SPICE:

•PLL's have clock frequencies of > 1GHz and loop bandwidths of < 5 MHz

•Full loop simulation can take a week and generates files > 100 MB

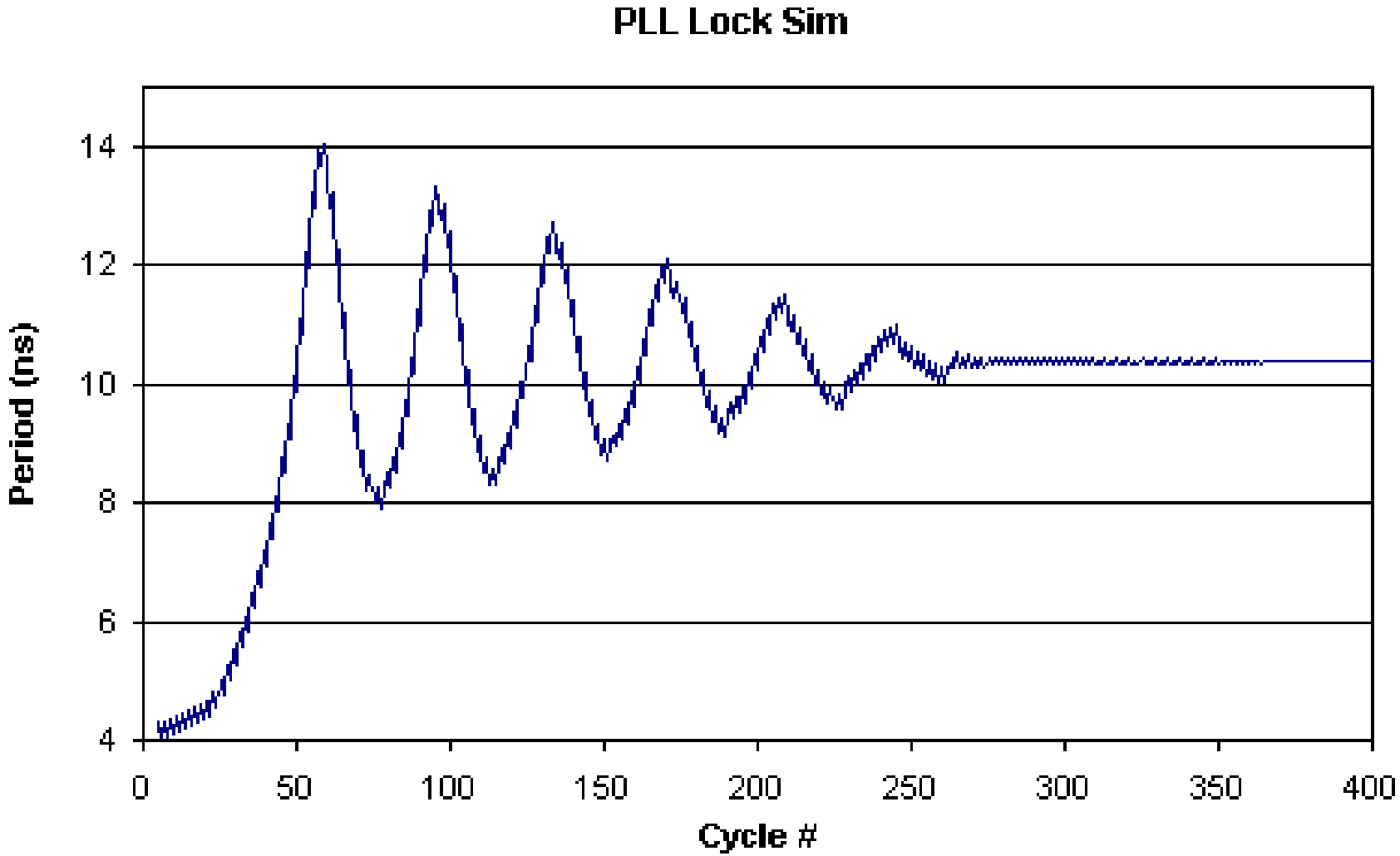
CycleSim

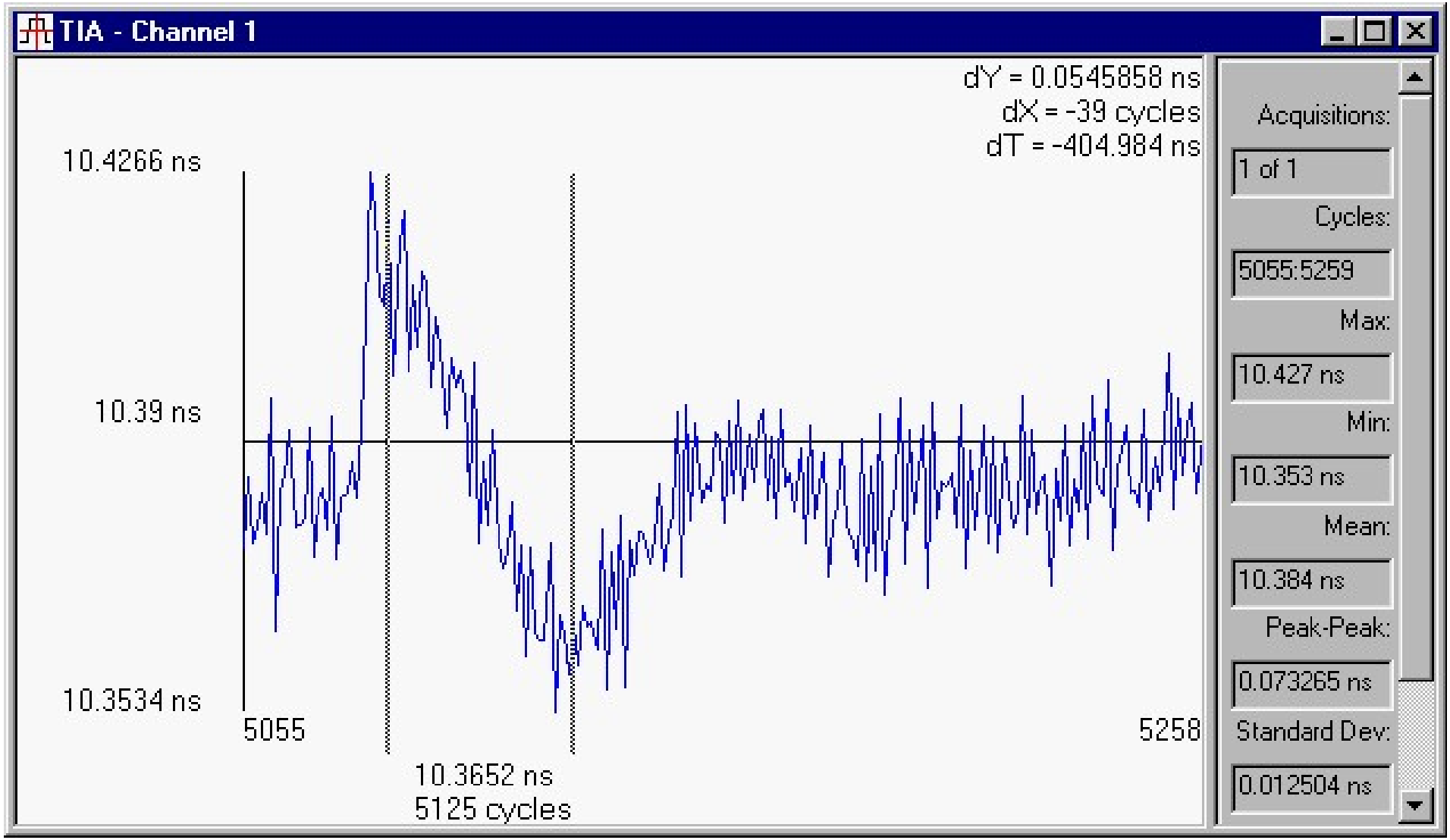
- **The PLL is modeled as DDF (not statically schedulable)**
- **Implemented in C++; each object is a node**
- **Clock sources such as VCO and reference have tokens that represent time tags**
  - **Time tags represent the point in time at which a clock waveform crosses a threshold on a rising edge**
- **Each iteration of the simulation is one cycle of the clock sources**
- **During each iteration the time tags are adjusted accordingly**

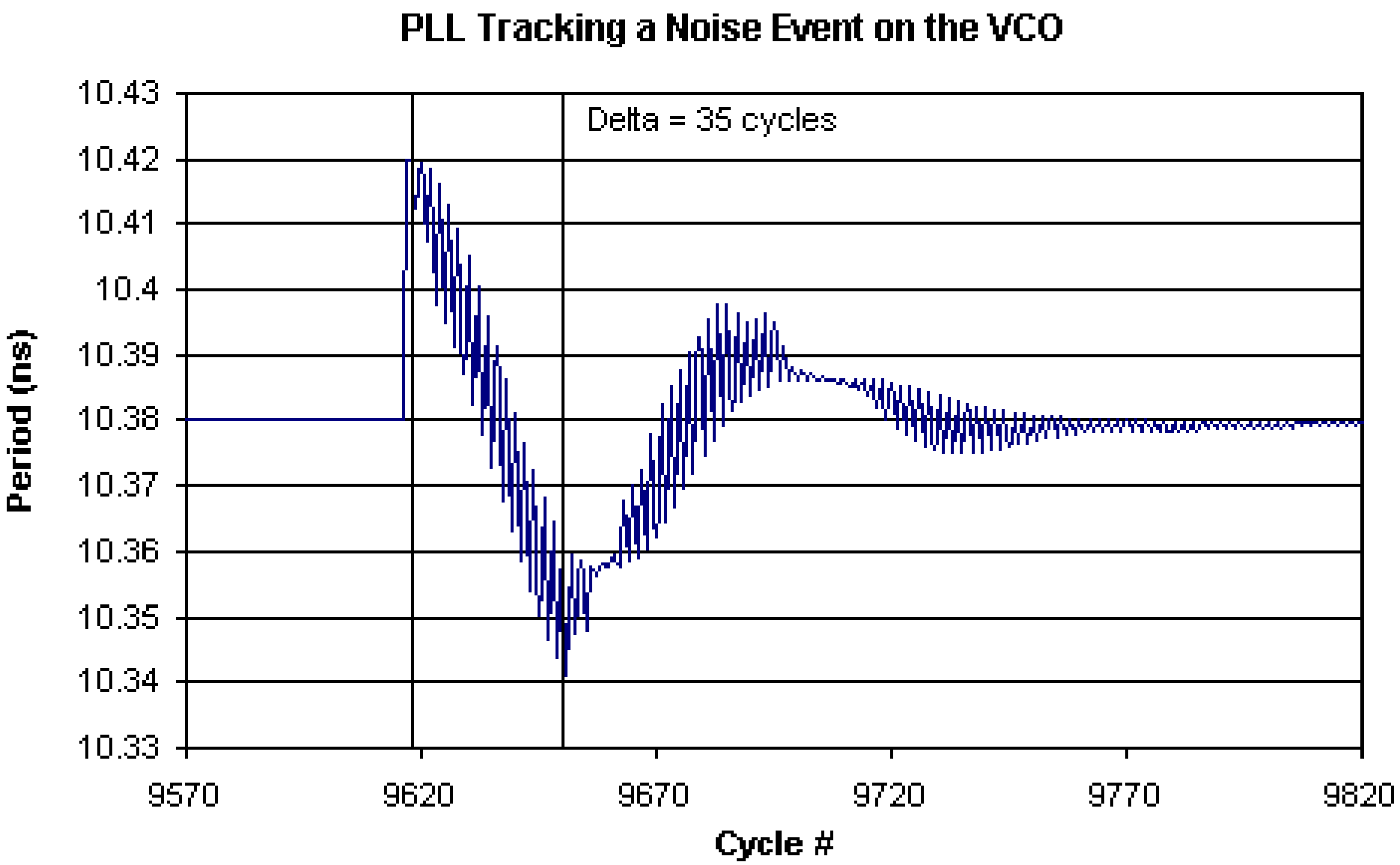

Time Tags for Clks with 3:1 Frequency Ratio
Time Tags(ns)
100000
90000
80000
70000
60000
50000
40000
30000
20000
10000
0
Clock/3
Clock
0
2000
4000
6000
8000
10000
Iterations

CycleSim (part 2)

- Reference clock - produces periodic time tags
- Phase-frequency detector - outputs phase difference between the reference clock and the divider
- Charge pump - integrates current over the phase difference and produces a change in voltage
- Loop filter - accumulates changes in voltage off charge pump
- VCO - uses voltage from loop filter to produce an output time tag


PLL Lock Sim
Period (ns)
14
12
10
8
6
4
0
50
100
150
200
250
300
350
400
Cycle #


TIA - Channel 1
dY = 0.0545858 ns
dX = -39 cycles
dT = -404.984 ns
10.4266 ns
10.39 ns
10.3534 ns
5055
5258
10.3652 ns
5125 cycles
Acquisitions:
1 of 1
Cycles:
5055:5259
Max:
10.427 ns
Min:
10.353 ns
Mean:
10.384 ns
Peak-Peak:
0.073265 ns
Standard Dev:
0.012504 ns


PLL Tracking a Noise Event on the VCO
Delta = 35 cycles
Period (ns)
10.43
10.42
10.41
10.4
10.39
10.38
10.37
10.36
10.35
10.34
10.33
9570
9620
9670
9720
9770
9820
Cycle #

Conclusions

- PLL's are mixed signal circuits which makes them difficult to simulate, especially in the time domain
- The cycle domain is more "natural" for describing PLL's as clock sources
- CycleSim is several orders of magnitudes faster than SPICE making it easy to fine tune current designs and explore new ones