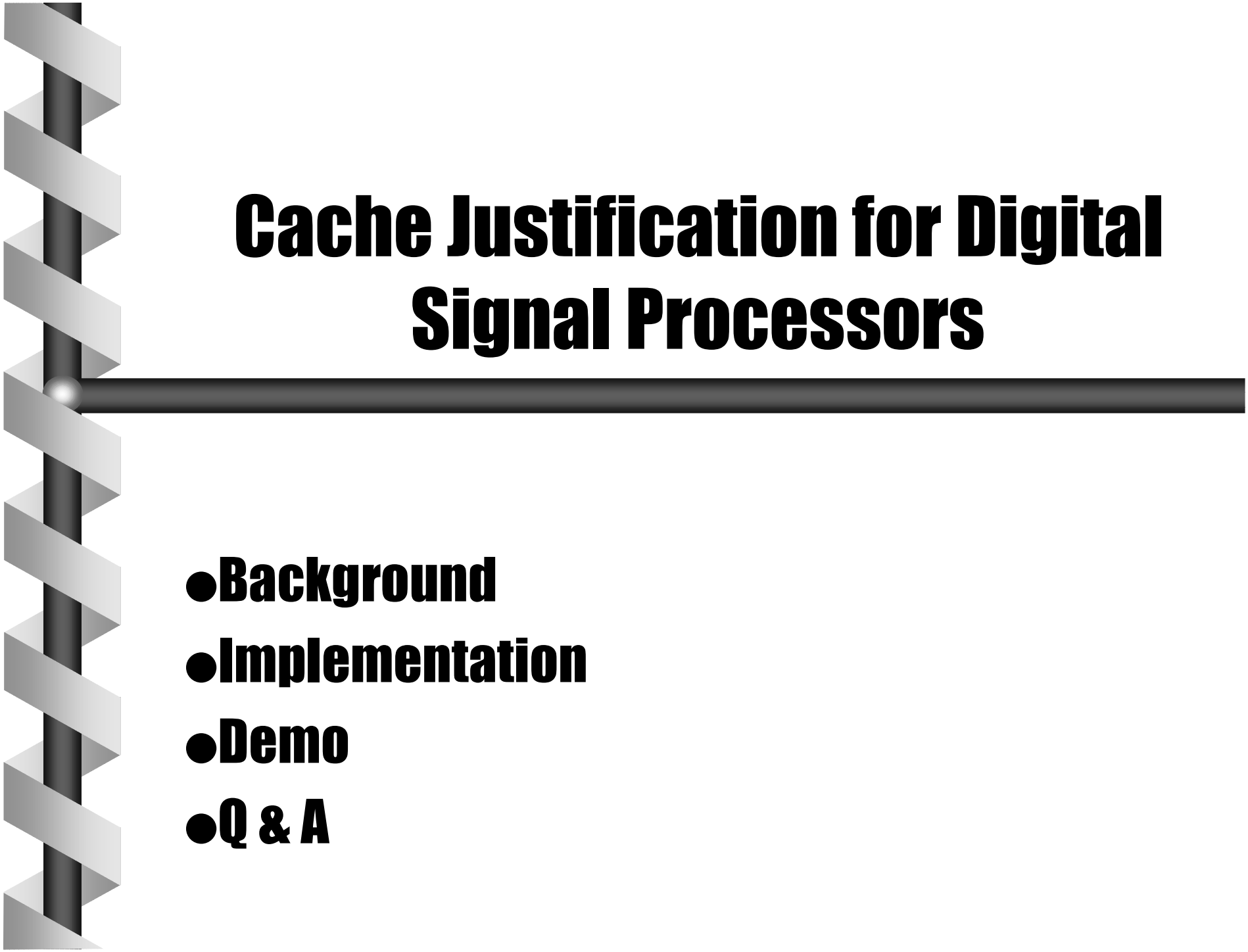
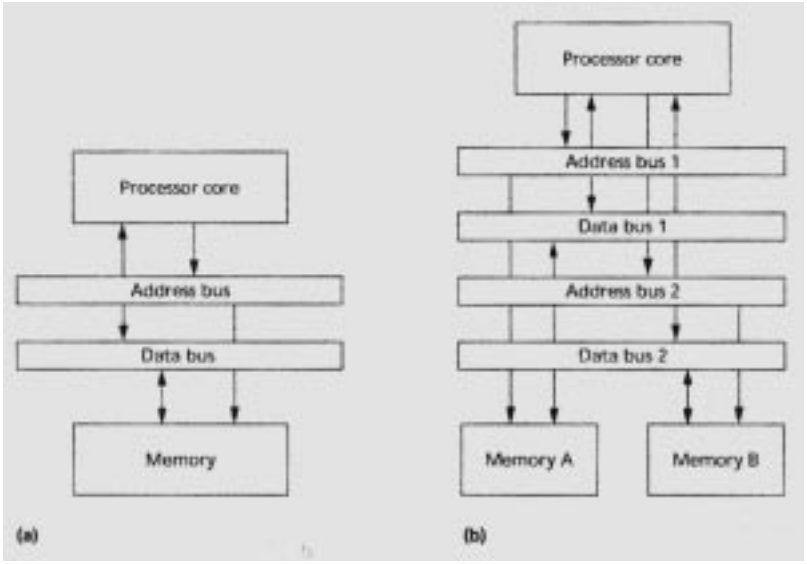


Cache Justification for Digital Signal Processors

- Background
- Implementation
- Demo
- Q & A

GPPs vs. DSPs

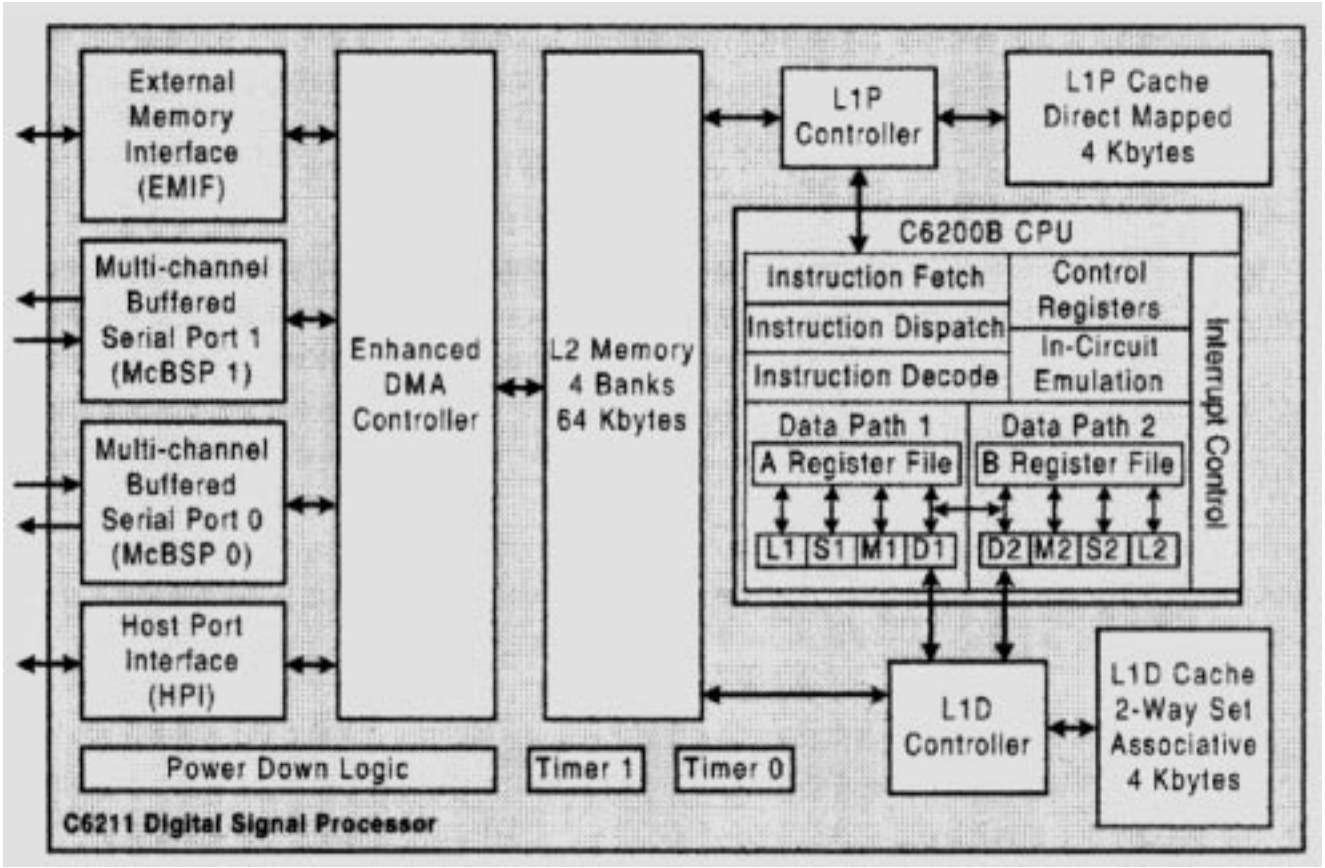
- Von Neumann
  - one memory space
  - one bus set
- Harvard
  - two memory spaces
  - two bus sets



Need for Cache

- GPPs
  - typically have data and instruction caches
  - multiple levels
- DSPs
  - typically no caches (some use program cache)
  - on-chip memory banks

TMS320C6211



Project Objective

- Substantiate performance gain
  - cache justification
  - cache utilization
- Hardware and software
  - TI's Code Composer Studio
  - common DSP kernels

Texas Instruments' Findings

- 80% of optimal cycle performance
- 98% hit in L1P
- 91% hit in L1D
- 96% hit in L2 (in 4-way set-associative mode)
- 99.5% of all CPU cycles without going to external memory

Application	Efficiency
v.34	89%
AC-3 Decoder	90%
Zlib File Compression	96%
Line Echo Cancellation	99%
GSM Frame Encoder	92%
GSM Frame Decoder	88%
ADSL	85%

My Findings

DSP Kernels	L1P Hit Ratio	L1D Read Hit Ratio	L1D Write Hit Ratio
IIR filter	92493/92517 (99.97%)	891/918 (97.06%)	356/371 (95.96%)
Vector Multiply	225696/225717 (99.99%)	1042/1066 (97.75%)	304/318 (95.60%)
MAC	171735/171158 (99.99%)	1350/1374 (98.25%)	460/475 (96.84%)
FFT	52366/52402 (99.93%)	118408/118805 (99.67%)	69894/69923 (99.96%)
Telecom	240145/240171 (99.99%)	328/338 (97.04%)	153/176 (86.93%)

Conclusion

- My findings ≈ TI's findings
- Caches do enhance performance
- Allows for faster development time
- Meets growing application needs