Cache Justification for Digital Signal Processors

- Background
- Implementation
- Demo
- Q & A
GPPs vs. DSPs

- **Von Neumann**
  - one memory space
  - one bus set

- **Harvard**
  - two memory spaces
  - two bus sets
Need for Cache

- **GPPs**
  - typically have data and instruction caches
  - multiple levels

- **DSPs**
  - typically no caches (some use program cache)
  - on-chip memory banks
TMS320C6211
Project Objective

- Substantiate performance gain
  - cache justification
  - cache utilization
- Hardware and software
  - TI’s Code Composer Studio
  - common DSP kernels
Texas Instruments’ Findings

- 80% of optimal cycle performance
- 98% hit in L1P
- 91% hit in L1D
- 96% hit in L2 (in 4-way set-associative mode)
- 99.5% of all CPU cycles without going to external memory

<table>
<thead>
<tr>
<th>Application</th>
<th>Efficiency</th>
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<tbody>
<tr>
<td>v.34</td>
<td>89%</td>
</tr>
<tr>
<td>AC-3 Decoder</td>
<td>90%</td>
</tr>
<tr>
<td>Zlib File Compression</td>
<td>96%</td>
</tr>
<tr>
<td>Line Echo Cancellation</td>
<td>99%</td>
</tr>
<tr>
<td>GSM Frame Encoder</td>
<td>92%</td>
</tr>
<tr>
<td>GSM Frame Decoder</td>
<td>88%</td>
</tr>
<tr>
<td>ADSL</td>
<td>85%</td>
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<tr>
<td>DSP Kernels</td>
<td>L1P Hit Ratio</td>
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<tr>
<td>IIR filter</td>
<td>92493/92517 (99.97%)</td>
</tr>
<tr>
<td>Vector Multiply</td>
<td>225696/225717 (99.99%)</td>
</tr>
<tr>
<td>MAC</td>
<td>171735/171158 (99.99%)</td>
</tr>
<tr>
<td>FFT</td>
<td>52366/52402 (99.93%)</td>
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<td>Telecom</td>
<td>240145/240171 (99.99%)</td>
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Conclusion

- My findings ≈ TI’s findings
- Caches do enhance performance
- Allows for faster development time
- Meets growing application needs