Project: **HDSL Standard Project**

Title: **Proposal to Break the FEC Logjam for HDSL2**

Source: **Adtran, Cicada, Siemens, Tellabs, Westell**

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Abstract

This proposal incorporates the various contributions from the many participants in the forward error correction debate ([1],[2],[3],[4],[5]). The rate-1/2 one-dimensional code features low latency, high performance, and straightforward decoder implementation. The programmable encoder ensures a future migration path and allows a variety of decoder structures (e.g. Viterbi or sequential). Normative text is given for direct inclusion in the HDSL2 standard.

Introduction

This proposal combines the results of the many contributors to the forward error correction effort for HDSL2. It will allow HDSL2 units to have low latency, high performance, straightforward decoder implementation, and good flexibility.

Normative Text

7.4.

Each symbol time, three bits shall be input from the scrambler, X1, X2, and X3, where X1 is the first in time. These three bits shall be applied to the encoder in Figure 7.4.1, forming bits Y0, Y1, Y2, and Y3. X1 shall then be shifted into the shift register, where T is a delay of one symbol time.

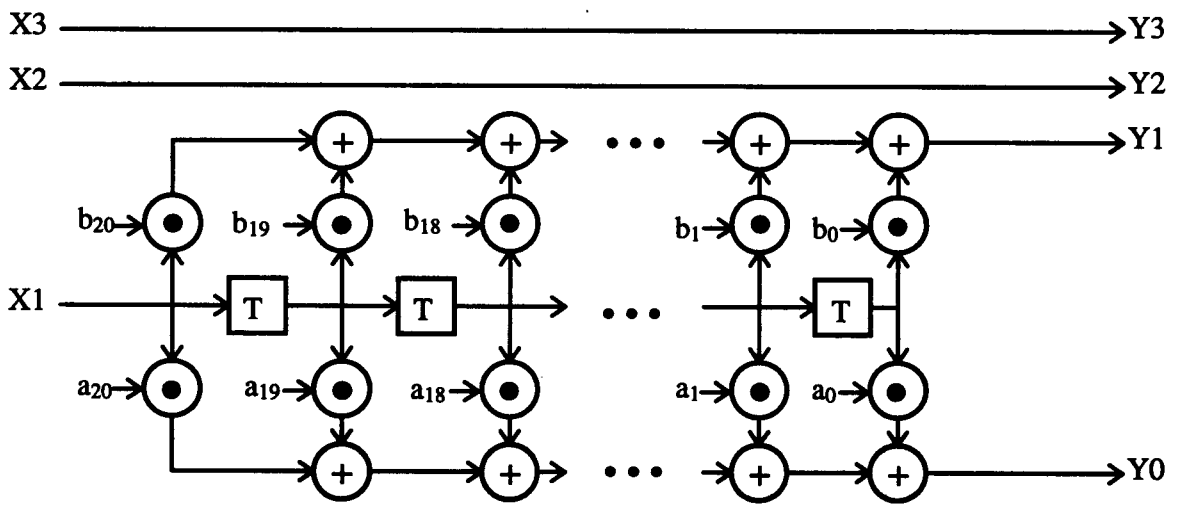

Figure 7.4.1 Block diagram of the encoder

The binary coefficients a_i and b_i shall be passed to the encoder from the receiver during the startup phase specified in §8.7. A numerical representation of these coefficients is A and B, where

$$A = a_{20} \bullet 2^{20} + a_{19} \bullet 2^{19} + a_{18} \bullet 2^{18} + \ldots + a_0 \bullet 2^0$$

and

$$B = b_{20} \bullet 2^{20} + b_{19} \bullet 2^{19} + b_{18} \bullet 2^{18} + \ldots + b_0 \bullet 2^0$$

The performance of the code specified by A and B shall be sufficient to meet the specifications in §14. The 512-state reference code which meets these requirements is A=6304000 octal and B=2670000 octal.

The bits Y3, Y2, Y1, and Y0 shall be mapped to a level C as specified in Table 7.4.1. C shall be processed by the channel precoder as specified in §7.5.

Table 7.4.1. Bit-to-Level Mapping

Trellis Encoder Output (Y3 Y2 Y1 Y0)	Level (C)
0000	-15
0001	-13
0010	-11
0011	-9
0100	-7
0101	-5
0110	-3
0111	-1
1100	1
1101	3
1110	5
1111	7
1000	9
1001	11
1010	13
1011	15

Conclusion

This proposal includes components from the various contributions that have been presented on one-dimensional trellis codes. It features excellent latency, performance, and flexibility.

Appendix

The values for A and B are calculated by taking the 10-bit code coefficients from [1] (g0=0556 octal and g1=1461 octal) and appending 11 binary zeros to the right-hand side.

References

[1] Mike Tu, Jack Liu, "A 512-State PAM TCM Code for HDSL2," PairGain, Sep. 1997, Minneapolis, T1E1.4/97-300.

[2] Jack Liu, Stanley Ling, Mike Rude, Chris Heegard "Proposal for HDSL2 Transmission: FEC Scheme," Joint contribution, Sep. 1997, Minneapolis, T1E1.4/97-301.

[3] Richard Goodson, "Performance and Characteristics of One-Dimensional Codes for HDSL2," Adtran, Sep. 1997, Minneapolis, T1E1.4/97-337.

[4] Richard Goodson, "Proposal for Programmable Trellis Encoder for HDSL2," Adtran, Sep. 1997, Minneapolis, T1E1.4/97-338.

[5] Chris Heegard, Stan Ling, Hiroshi Takatori, "Simulation Results of 1-D TCM for HDSL2," Level One, Sep. 1997, Minneapolis, T1E1.4/97-354.