ADSL Receiver Modelling

- Vikas Agarwal
- Rajagopalan Desikan
- Karthikeyan Sankaralingam

Decoder and Bit Buffer

- Splits the digital input into channels. Reverse it in Receiver end.
- Bandwidth optimization. Choose which of the channels can be used from the available ones based on SNR.
- Based on maximizing bit rate, minimizing input power level.
- G.Lite − sub channels − 256

Cyclic Prefix (CP)

- Adds padding information during modulation.
- Padding added because of the impulse response of the physical channel.
- Length of impulse response <= Length of CP (v) + 1
- Disadvantage − Reduces efficiency by a factor N/(N+v)
- Reduce memory of channel with a finite impulse response filter − TEQ.
- Best throughput for given complexity is got with a combination of CP + equalizer.
- Full equalization to a memoryless channel is very complicated.