Simulation and Modeling of an ADSL modem – Channel Model and Receiver Initialization

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Abstract

In this project, I will design a channel model and the systems needed for receiver initialization of a ADSL G.lite modem in the Agilent HP EESof design environment. One of the significant problems in ADSL modem design is the inherent complexity of the system. The ultimate objective of this project is to build a high level abstraction of the design of an ADSL G.lite modem. This will make it easy to simulate the operation of the modem, to evaluate the design and with powerful synthesis tools may even be used to synthesize a working design. The channel model is needed to accurately simulate the effect of transmission of an electrical signal through a twisted pair of copper cables. For optimal performance the receiver and transmitter must adapt to the channel and noise characteristics during initialization. The receiver must estimate the channel and noise, perform channel equalization and also synchronize to the transmitter.

1 Introduction

The demand for bandwidth for high speed data communications and interactive media transmission has been growing explosively. Digital subscriber line (DSL) technologies reuse the existing twisted pair copper cables that already reach most of the customers for telephone connections to provide cost-effective, dedicated uninterrupted high data rate connections that are secure and are always on.

Typical bandwidth requirements of residential customers and small businesses are asymmetric. Consumers require a higher bandwidth in the downstream direction (from the telecommunication provider to the consumer) than the upstream direction (from the user to the provider). Asymmetric digital subscriber line (ADSL) is a form of DSL that caters to this market. The operation of an ADSL modem, as standardized by the American National Standards Institute (ANSI), can support up to 6MB/s downstream and up to 1.5MB/s downstream simultaneously along with voiceband data [1]. However, a splitter is required to separate the voiceband from the ADSL data transmission. The need for a splitterless version of ADSL was felt to make customer installation easier. Splitterless ADSL uses lesser power to reduce interference and can therefore only support lower data rates of up to 1.5MB/s downstream. This version of ADSL, called G.lite was standardized by the International Telecommunication Union recently [2].

One of the significant problems in ADSL modem design is the inherent complexity of the system. The objective of this project is to build a high level abstraction of the design of an ADSL G.lite modem. The which will make it easy to simulate the operation of the

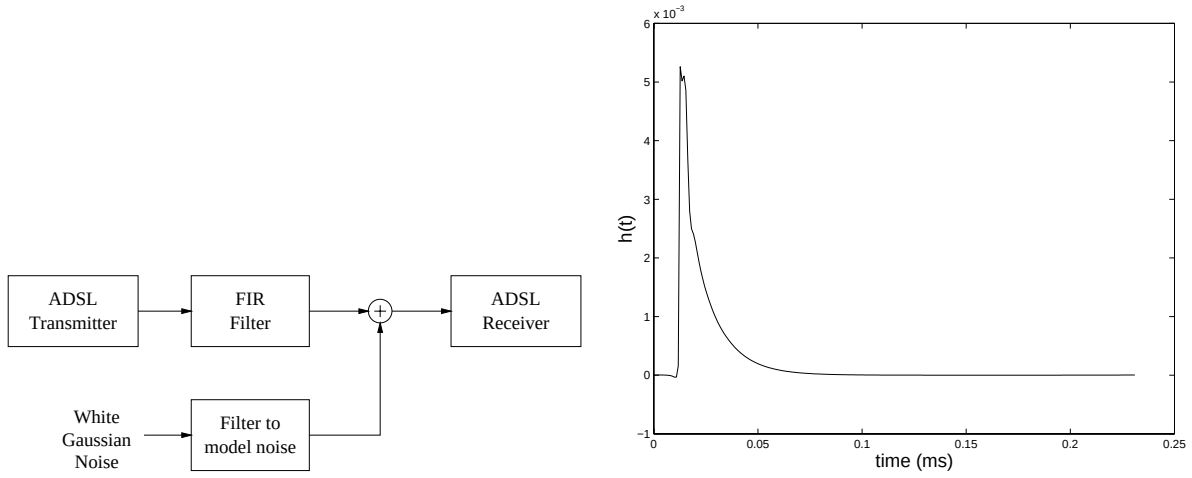
modem, to evaluate the design and with powerful synthesis tools may even be used to synthesize a working design. I will be working with two other groups and we will be using the Agilent HP EEsof design environment [3]. My contributions to the project are to build a channel model and the systems needed for the initialization of an ADSL receiver. The channel model is needed to accurately simulate the effect of transmission of an electrical signal through a twisted pair of copper cables. For optimal performance the receiver and transmitter must adapt to the channel and noise characteristics during The receiver must estimate the channel and noise, perform channel equalization and also synchronize to the transmitter.

2 Background

2.1 Channel characteristics

The channel characteristics are determined by several factors including cable length, cable gauge, bridge taps, different resistor capacitor terminations and shunt resistances [4]. The signal is subject to crosstalk, electromagnetic interference from other cables in the same bundle. Relatively less distortion is further caused by external sources and thermal noise.

The effect of the channel can be modeled as a linear shift invariant filter and additive colored noise as shown in Fig. 1(a). The linear filter can be computed by modeling the elements of the line using the ABCD parameter model for 2-port networks Fig. 1 shows the linear model for ANSI specified test case carrier-serving-area loop1 (csaloop1) [4]. The



(a) (b)

Figure 1: (a) Modeling of channel (b) Channel model for ANSI specified test case csaloop1

crosstalk can be modeled as colored Gaussian noise [4, 5]. The frequency response of the coloring filter is given by

$$H(f) = 10^{-13} \left(\frac{N}{49}\right)^6 f^{1.5} \tag{1}$$

where N is the number of disturbers in the bundle and f is frequency in Hertz. Other external sources of noise are modeled as additive white Gaussian noise.

3 Overview of G.lite ADSL modem

A bandwidth of 28kHz to 552kHz is used by ADSL G.lite modems [2]. Lower frequencies are avoided to prevent interference from voiceband data. The lower part of this bandwidth up to 138kHz is used by upstream data and the rest by downstream data. Using discrete multitone modulation (DMT) the modem modulates data into 128 subbands of size 4.3125kHz. The modem operates in two modes, data transmission and initialization.

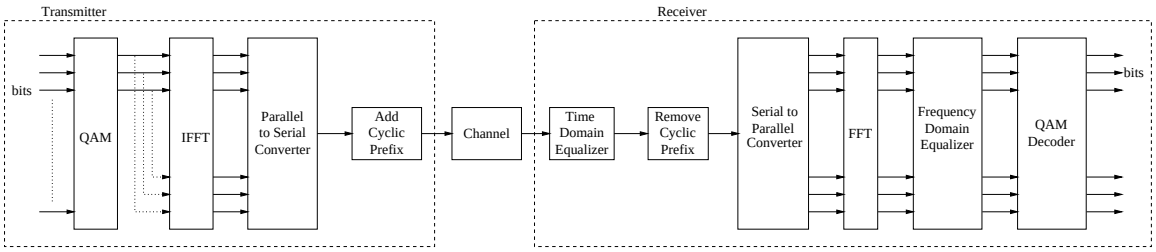


Figure 2: Block diagram of ADSL transmitter and receiver

3.1 Data Transmission mode

Fig. 2 shows a simplified schematic of the operation of an ADSL transmitter and receiver during data transmission [2]. The input bitstream is first sent through several stages like error correction coding, interleaving and scramblers. The power level and number of bits in each sub-channel is chosen to maximize data rate at a fixed bit error rate. One of the sub-channels is dedicated to transmitting a pilot signal that is used by the receiver for synchronization. The bit streams are modulated by baseband quadrature amplitude modulation (QAM). The outputs are mirrored and then modulated into higher frequencies using a 256 point inverse fast Fourier transform (IFFT). The output of the IFFT is guaranteed to be real. A cyclic prefix of 16 samples is added to the 256 samples to create a frame. The cyclic prefix accounts for inter-symbol interference (ISI) due to transmission over a channel with memory. Every 69^{th} frame is a synchronization symbol and carries no data.

The receiver uses a time domain equalizer which is usually a finite impulse response filter (FIR) filter to reduce the memory of the effective channel to less than the cyclic prefix. The cyclic prefix is removed and then the data is sent through a FFT block and

a frequency domain equalizer. The frequency domain equalizer is a point wise scaling operation to compensate for the effect of the shortened channel. The 128 outputs are then sent to QAM decoders, followed by the error detection and correction systems.

3.1.1 Initialization mode

During initialization known data sequences are transmitted to train the receiver and transmitter. The G.lite standard specifies a detailed list of states and the signals to transmit and expect to receive while in each state [2]. The initialization sequence consists of four steps described below.

1. **Handshake** : The transceivers establish a connection in this mode. They negotiate settings and determine the functionalities present in each other like the kind of modem - G.lite or regular ADSL, ability to perform certain kinds of error control coding and so on.

2. **Transceiver training** : The first pulse transmitted is a sinusoid at 276kHz and is used for synchronization. The next set of pulses are wideband and are used to determine received signal powers and for adjustment of the automatic gain control system. The receiver can train its equalizer at this step.

3. **Channel Analysis** : The transmitters convey information about their settings like the parameters of the error control coders, minimum required signal to noise ratio (SNR) margins and maximum number of bits per carrier that is supported. A

wideband pseudo random sequence is transmitted to measure signal to noise ratio in each sub-channel.

4. **Exchange**: Now the receivers recompute margins and loop attenuations. The receivers calculate the bit loading and gains for each channel and the information is exchanged between the modems.

4 Modeling and proposed work

4.1 Channel Model

A C program will be used to compute the channel model as a discrete time FIR filter given the parameters of the cable [6]. Crosstalk will be modeled as additive white Gaussian noise filtered through infinite impulse response filter modeled according to (1). The channel model will be in the synchronous data flow domain [7]. To simulate timing offsets a dynamic data flow model will be used in an interpolater at the front end of the receiver [7].

4.2 Receiver initialization

The power of the received signal and noise power estimation can be done simply by computing the mean and variance of the received signal spectrum over the periodically repeating data sequences. From these the channel and the SNR can be easily computed [4]. The computation can be expressed as synchronous data flow. The channel and SNR

estimates are used to compute optimal bit loading [8].

Several techniques for channel equalization have been proposed. The most effective methods attempt to maximize channel capacity or approximations to it [9, 10]. The most successful method in terms of maximizing capacity has been to minimize ISI [11]. I will be implementing this method. A channel estimate is needed to compute the optimal filter. The computation involves an eigen-value decomposition and can be expressed as synchronous data flow [12].

Synchronization can be achieved using a phase locked loop. One of the subchannels is reserved for a pilot symbol. This pilot symbol is a sinusoid at a fixed frequency in a better part of the channel. The bandpass filtering is easily achieved by a using the FFT block. This gives a clean estimate of phase offset that is free from data dependent jitter [4]. This is then used to modulate the frequency of the clock signal.

Synchronization of frame boundaries is achieved during the initialization mode. The synchronization frame is used to compute a phase offset in the frequency domain. This is later used to adapt the frame marker.

All the individual systems mentioned above can be modeled as synchronous data flow. A finite state machine is needed to trigger the operation of these systems at the appropriate instants and to track the state of the receiver during initialization.

References

[1] ANSI T1.413-1995, "Network and customer installation interfaces: Asymmetrical digital subscriber

line (ADSL) metallic interface."

[2] ITU-T G.992.2, "Splitterless asymmetric digital subscriber line (ADSL) transceivers."

[3] Agilent Technologies Inc., "Agilent HP EEsof Web site." http://www.tm.agilent.com/tmo/hpeesof/.

[4] T. Starr, J. M. Cioffi, and P. J. Silverman, *Understanding Digital Subscriber Line Technology.* Prentice-Hall PTR, 1999.

[5] K. J. Kerpez, "Near end crosstalk is almost Gaussian," *IEEE Trans. on Comm.*, vol. 41, pp. 670–672, May 1993.

[6] Information Systems Laboratory, Stanford University, "The linemod program." http://www-isl.stanford.edu/people/cioffi/linemod/linemod.html.

[7] B. L. Evans, "Class notes for ee382c: Embedded software systems, spring 2000," The University of Texas at Austin.

[8] P. S. Chow, J. M. Cioffi, and J. A. C. Bingham, "A practical discrete multitone transceiver loading algorithm for data transmission over spectrally shaped channels," *IEEE J. on Selected Areas in Comm.*, vol. 43, pp. 773–775, Feb./Mar./Apr 1995.

[9] N. Al-Dhahir and J. M. Cioffi, "Optimum finite-length equalization for multicarrier transcievers," *IEEE Trans. on Comm.*, vol. 44, pp. 56–63, Jan. 1996.

[10] N. Al-Dhahir and J. M. Cioffi, "Bandwidth-optimized reduced-complexity equalized multicarrier transceiver," *IEEE J. on Selected Areas in Comm.*, vol. 45, pp. 948–956, Aug. 1997.

[11] P. J. W. Melsa, R. C. Younce, and C. E. Rohrs, "Impulse response shortening for discrete multitone transceivers," *IEEE Trans. on Comm.*, vol. 44, pp. 1662–1672, Dec. 1996.

[12] G. H. Golub and C. F. V. Loan, *Matrix Computations.* Baltimore, MA: The Johns Hopkins University Press, 3 ed., 1996.