Simulation and Modeling of an ADSL Modem - Channel Model and Receiver Initialization

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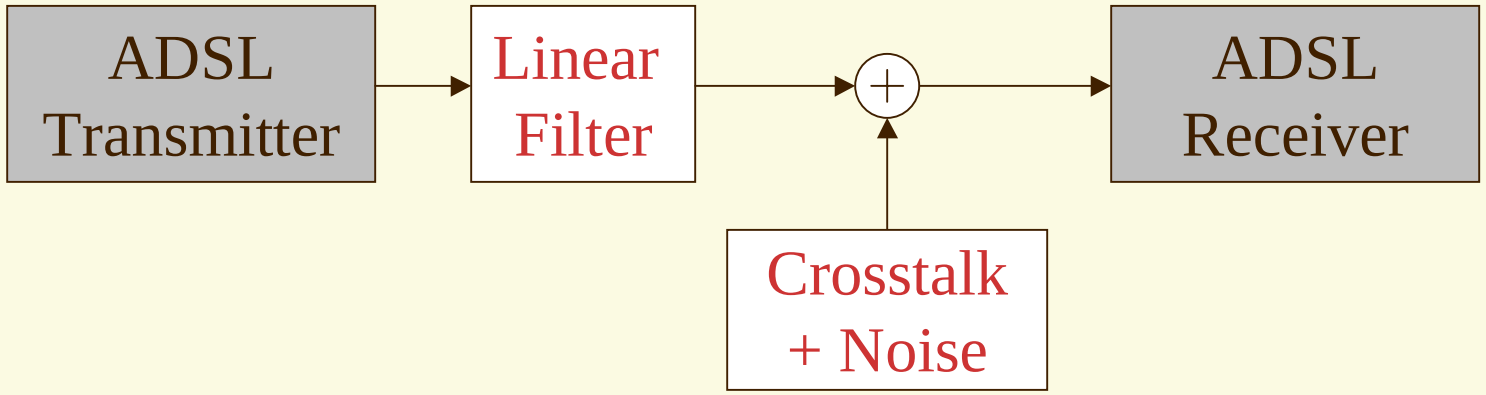
Channel Model



- ✔ Model transmission over copper cable
  - Linear shift invariant (FIR) filter
  - Crosstalk - additive colored noise
- ✔ Modeled as synchronous data flow (SDF)

Receiver Initialization

- ✔ Subcarrier detection
  - Handshake signals
  - Pilot phase for phase locked loop
- ✔ Input power estimation for gain control
- ✔ Channel delay estimation
  - frame synchronization during initialization
- ✔ Channel and signal to noise ratio estimation
  - Channel equalization (without cyclic prefix)
  - Bit loading (with cyclic prefix)

Modeling Strategy

- ✔ Front End
  - Synchronize sample input and output
  - Buffer input samples to achieve variable delay
    - Frame synchronization
    - Enable/disable cyclic prefix
- ✔ Back End
  - Frame synchronize transmitter and receiver
    - One iteration handles one frame of input/output
    - Simultaneously switch to cyclic prefix mode

Modeling

- ✔ Model ADC/DAC as one SDF block
  - force synchronized operation
- ✔ Dynamic dataflow for input data buffer
- ✔ Back End
  - Processing in SDF blocks
  - Dataflow controlled by boolean logic
    - Boolean dataflow
  - Finite state machine embedded in SDF block

Modeling

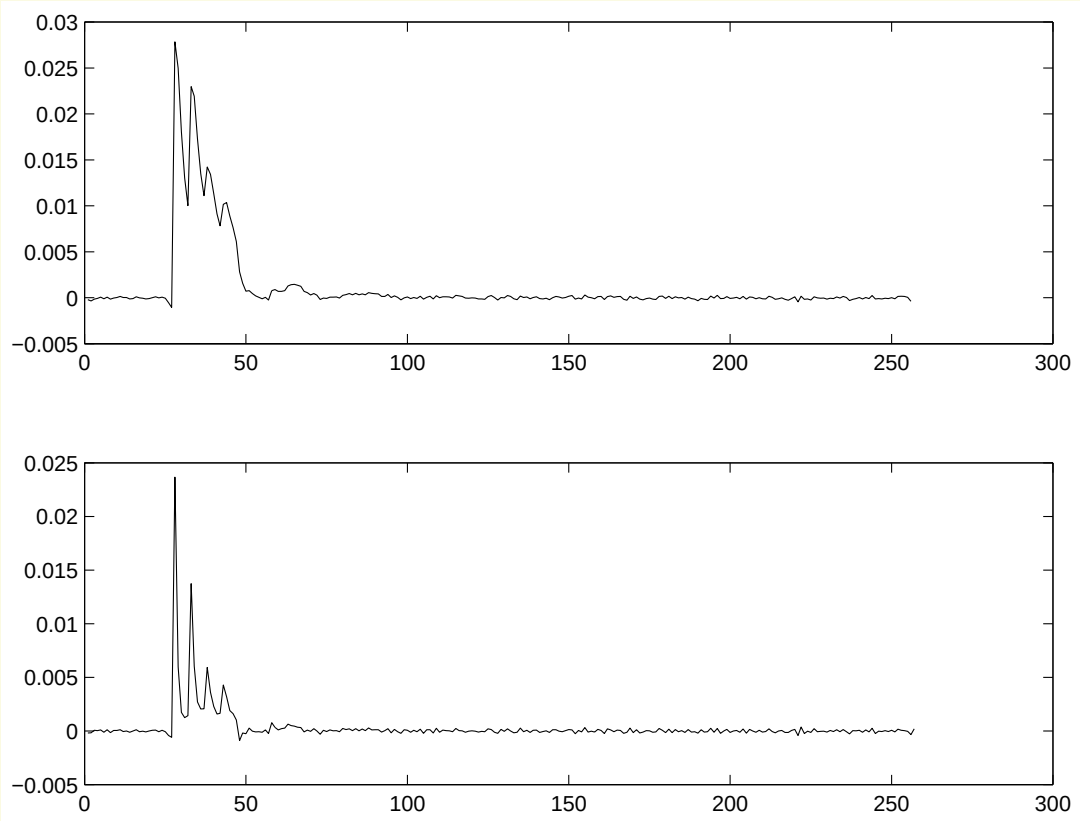
- ✔ Front End
  - Requires dynamic scheduler
    - dynamic data management
- ✔ Back End
  - Annotated static schedule (SDF, BDF & FSM)
  - All computation intensive units in SDF
- ✔ Increase in signal processing delay

Results

Channel Response

Channel Length : 256
Cyclic Prefix : 16

Shortened Channel Response



Conclusions

- ✔ Deliverables:
  - Channel model for ADSL transmission
    - User definable parameters
  - Model for ADSL receiver during initialization
    - Statically schedulable except for dynamic data management
    - Dynamically compute optimal settings