Modeling and Simulation of Discretized Data Transmission in Very High-Speed Digital Subscriber Line

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Problem Statement

- Design a Synchronous Dataflow (SDF) model for discretized data transmission in Very High-Speed Digital Subscriber Line (VDSL)
 - Create an abstraction for Discrete Multitone (DMT) based VDSL modems compliant with the standards
- Implement and simulate discretized data transmitter and receiver in an electronic design automation tool
 - Implement physical layer functional blocks
 - Open issue: Enable designers to build and optimize transceiver sub-systems without having to re-implement the whole design

Modeling the System

- Typical communication system, directly mapped to SDF
 - One token corresponds to one DMT sub-symbol (complex number)
 - "e" is the cyclic extension
 - A model that uses 512 sub-carriers



QE: Bank of QAM encoders WIN: Windowing CER: Cyclic extension removal SE: Conjugate symmetric extension CE: Cyclic extension CH: Channel PF: Pre-filter FEQ: Frequency-domain equalization QD: Bank of QAM decoders

The VDSL Channel

• VDSL channel is complicated

- Channel impulse response modeled as a Finite Impulse Response (FIR) filter
- Crosstalk: Near-end crosstalk (NEXT) and far-end crosstalk (FEXT) modeled as outputs of FIR filters whose inputs are White Gaussian Noise (WGN)



Solution: Implementation in ADS

- Implement the SDF model for discretized transmission using Agilent Advanced Design System (ADS)
 - Create a hierarchical design
 - Higher levels: Use mainly built-in dataflow library actors of ADS
 - Use MATLAB for implementing customized actors in subcomponents
- Given a VDSL channel, design the pre-filter and frequency domain equalizer (FEQ)
 - Use MATLAB to design filters
 - Filter coefficients directly exported to ADS
- Design a bank of Quadrature Amplitude Modulation (QAM) encoders/decoders based on the bit allocation table
 - Each encoder/decoder uses a lookup table to encode/decode subsymbols

Evaluation

- Testing our ADS system design
 - System parameters
 - A VDSL line (Loop 5): 300 m in length
 - 512 sub-carriers (FFT/IFFT size 1024)
 - 80 sub-symbols for cyclic extension
 - Sampling frequency of 4.416 MHz
 - Assumed perfect synchronization of the receiver and transmitter
 - Designed a pre-filter: A 5-tap time-domain equalizer to shorten the channel impulse response
 - Designed a 1-tap Frequency Domain Equalizer per subcarrier
 - Achievable bit rate was 17.9 Mbps for a bit error rate of 10^{-7}

Conclusion

- Deliverable:
 - Synchronous Dataflow model for discretized VDSL transmission implemented in ADS
 - MATLAB scripts for co-simulation
 - Flexible framework for testing designs
 - European Telecommunication Standards Institute (ETSI) compliant
- Impact: Accelerate product development
 - Given the high-level design, sub-components can be easily upgraded and tested
 - Powerful tool when coupled with ADS's Verilog and VHDL code synthesis capability
 - Major requirement for the DSP-based solutions