H.26L Video Server Modeling Using Computational Process Networks

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Embedded Software Systems

Class Project: Final Presentation



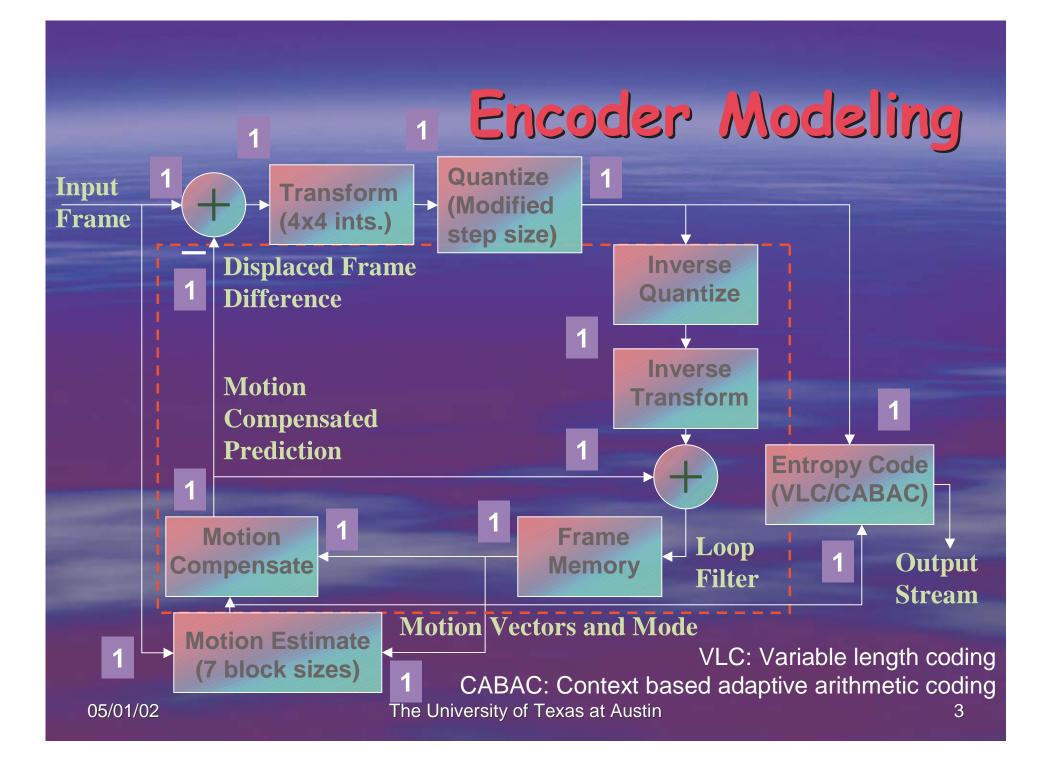
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Problem Statement

H.26L Video Encoder Modeling

- Model computation and communication in encoder
- Exploit inherent parallelism
- Preserve functional precedence
- Bounded memory implementation exists
- Design Domain
 - Computational process networks [Allen and Evans; 1999]
 - C code for H.26L video encoder [PictureTel Corp.; 2002]



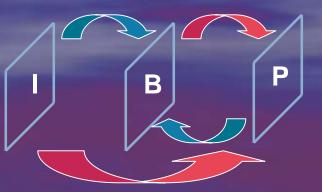
Implementation

Domain: CPN

- Scalable design
- Precedence preserving

'Foreman' Input Sequence

- QCIF resolution (176 x 144)
- 3 frames: Intra (I), Bi-directional (B), and Predicted (P)



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Results

Successful Encoding

- Nodes and queue designs [He and Zhong; 2000]
- Generated sequence decoded with H.26L decoder

Timing

- Speedup could be obtained for encoding more frames
- Parallel execution of I-frames on multiple processors

Compression Results



Original frame 2 of QCIF (176 x 144) resolution foreman sequence



Decoded frame 2 of QCIF (176 x 144) resolution foreman sequence

Compression: 25:1 (comparing file sizes)
Time: 20 sec for 3 frames with 10 sec for B-frame

Applications

Video and POSIX Threads

- On-line scene change detection in multicast video
 - Buffering of frames, and processing of frames can be modeled on separate processors for scene change detection
- Video conferencing
- Video streaming
- Real-time H.26L Encoding Products [2002]
 - Texas Instruments with UB Video Inc. and Ingenient Technologies: On TMS320C64x digital signal processor

Conclusions

Deliverables

- Data and control flow modeling of H.26L encoder
- Computational process networks modeling
- Applications where parallelism can be exploited

Results Summary

- Time taken is more than expected
 - Unoptimized code
 - Number of frames being processed is less
- Compression is 50% more than state-of-the-art (H.263, MPEG-2, MPEG-4) encoders for same quality