Modeling and simulation of H.26L Encoder

Mrudula Yadav and Gayathri Venkat

EE382C : Embedded Software Systems

Class Project : Final Presentation

The University of Texas at Austin

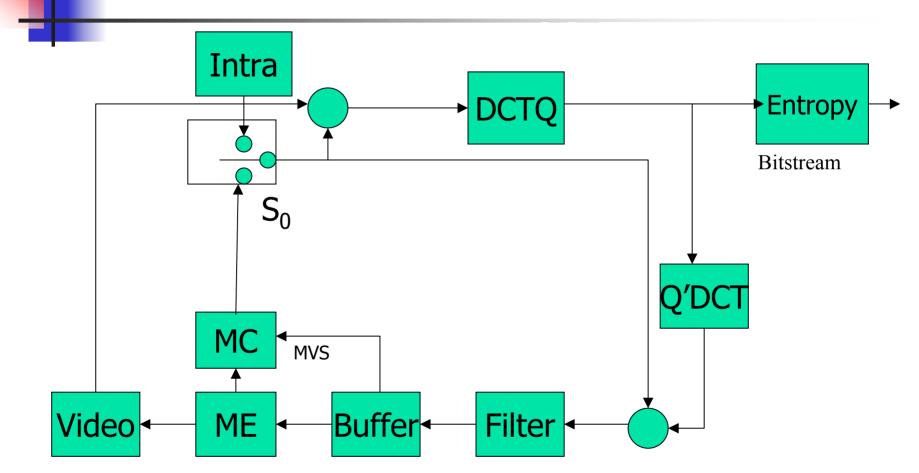
May 1, 2002



Problem Statement

- Exploit inherent parallelism of existing implementation
- Achieve higher Speed up by distributing the computation in different processors
- Improve scalability and flexibility





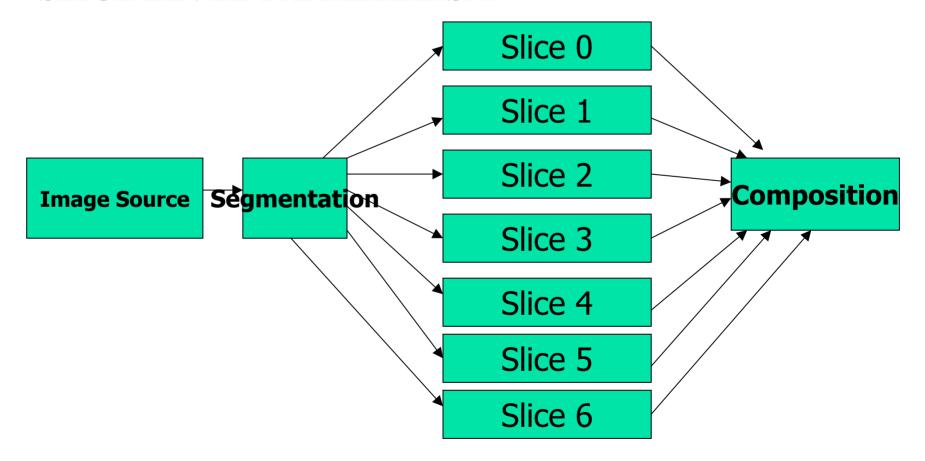


Our Approach

- Identify Computation Intensive blocks
- Exploit image slicing in H.26L
- Modeling in Ptolemy
 - Synchronous Dataflow (SDF) for simulation
 - Code Generation Domain (CGC) for implementation

Our solution

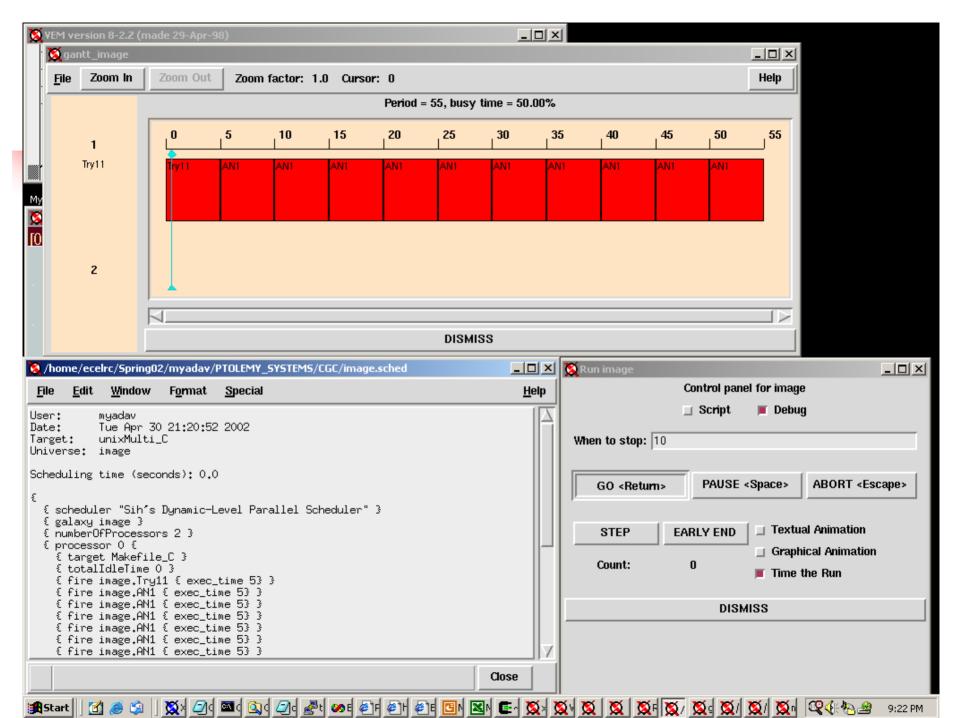
SLICE LEVEL PARALLELISM





Software Implementation

- Transport C code to SDF model in Ptolemy
- Migrate SDF domain to CGC domain
- Test Under Multi Processor Conditions
- Generate Gantt Chart



Results

Existing Codec	141.1 sec
SDF Model	133.13 sec
CGC	74.14 sec

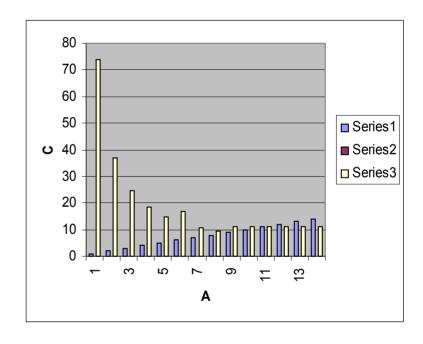


Image Size (176 * 144), 99 Macroblocks (16*16) Each Slice = 11 blocks TotalNo. Slices = 9

Conclusion

- Our approach
- Linear SpeedUp with the Number of Processors
- InterProcessor Communication is close to zero
- Future Work
- Block Level parallelism in Transform calculations, MV computation and Entropy Coding (UVLC Universal Variable Length Coding)
- Migration of the above model in other Code Generation domains