Modeling of an ADSL Transceiver Data Transmission Subsystem

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ABSTRACT

Recently, there has been an increase in demand for digital services provided over the public telephone line network. Asymmetric digital subscriber lines (ADSL) transmit high bit rate data in the forward direction to the subscriber, and lower bit rate data in the reverse direction to the central office, both on a single copper telephone loop. In this paper I present a survey on the recent research and standardization of ADSL transceivers. I propose to model and simulate an ADSL transceiver using Synchronous Data Flow (SDF).

1. INTRODUCTION

With the emergence of the Internet as the cornerstone to most of the communications in this age, the demand for high speed Internet access has only been increasing. Asymmetric digital subscriber lines (ADSL) is one of the technologies that provide high-speed Internet access in residences and offices [1]. It facilitates the use of normal telephone services, Integrated Services Digital Network (ISDN), and high-speed data transmission simultaneously. Hence, bandwidth-demanding technologies, such as video-conferencing and Video-on-demand, are enabled over ordinary telephone lines.

The European Telecommunications Standards Institute (ETSI) and the American National Standards Institute (ANSI) have defined standards for ADSL transceivers. Both of these standards propose the use of discrete multi-tone (DMT) as the modulation technique for ADSL transceivers. DMT divides the effectively band-limited communication channel into a larger number of orthogonal narrowband subchannels. This allows for maximizing the transmitted bit rate and adapting to changing line conditions.

In this literature survey, I briefly discuss the recent research and standardization of ADSL transceivers. I also propose to model and simulate an ADSL transceiver using Synchronous Data Flow (SDF).

2. BACKGROUND

2.1. ADSL Architecture

ADSL transmits data over frequencies up to 1.1 MHz. The limit of 1.1 MHz is due to power constraints imposed by the Federal Communications Commission (FCC). The 1.1 MHz bandwidth is divided into 256 narrowband subchannels downstream (from the service provider to the customer) and 32 subchannels upstream (from the customer to the service provider). Each 4.3 kHz narrowband subchannel has a separate carrier, and the carriers are harmonically related. This type of data transmission is known as DMT modulation, which is the type of multicarrier modulation proposed in the ADSL technical specification.

The first channel in ADSL (0-4.3 kHz) is always dedicated for voice. The rest of the channels are specified differently according to two different methods: 1) Frequency Division Multiplexing, where upstream and downstream channels use different frequencies, and 2) Echo Cancellation, where upstream and downstream channels overlap. In the latter case, echo cancellation techniques make the channels independent.

2.2. ADSL Impairments

The performance of ADSL systems faces degradations due to severe channel attenuation, Intersymbol interference (ISI) or Interblock Interference (IBI), and other line impairments including crosstalk, additive white Gaussian noise and impulse noise. The effective length of the channel impulse response ν will cause IBI as the tail of the previous ADSL block symbol will corrupt the beginning of the current block symbol, hence the name IBI [2].

Crosstalk is caused by electromagnetic radiation due to other signals that are traveling in adjacent or nearby cables. Near-end crosstalk (NEXT) is caused by signals that are traveling in the same direction, while far-end crosstalk is caused by signals traveling in the opposite direction. Both NEXT and FEXT increase with frequency. Table 1 shows the attenuation of a signal traveling at 1.1 MHz in a 24 gauge wire relative to the length of the wire.

Table 1. Attenuation of a 24 gauge wire signal at 1.1 MHz.

Length of line (in kft)	Attenuation (in dBm/Hz)
10	-70
12	-90
14	-100
16	-110
18	-120

2.3. Discrete Multi-tone Modulation

The fundamental goal of multicarrier modulation techniques is to partition a data transmission channel with ISI into a set of orthogonal, memoryless subchannels, each with its own “carrier” [2]. Data is transmitted through each subchannel independently of other subchannels. Previous research has shown that such a system is capable of transmitting at the highest data rate when allocating more bits and energies to subchannels with higher signal-to-noise ratio (SNR) [3, 4]. DMT modulation is one of many multicarrier techniques including Vector Coding, Structured Channel Signaling, and Discrete Wavelet Multi-tone Modulation.

DMT based systems uses Quadrature Amplitude Modulation (QAM) to encode the input bit stream into a finite set of symbols in a one-to-one mapping of integers in [0, N-1] to complex numbers, where N is a power of 4. Each subchannel carries one QAM symbol. The number of bits that can be used to generate the QAM symbol in the *i*th subchannel with an estimated SNR_n is approximately given by

$$b_n = \log_2(1 + \frac{SNR_n}{\Gamma}) \tag{1}$$

where the gap $\Gamma = 9.8$ dB – $\gamma_m - \gamma_c$ for a bit error rate of 10^{-7} [4]. The quantity γ_c is coding gain of the applied code and γ_m is the margin. The optimum assignment of bits to each subchannel, which is not necessarily an integer value, is found using bit loading algorithms [4]. In the case of non integer assignment, bits are truncated or rounded to the nearest fraction that can be implemented by multidimensional trellis codes.

DMT modulation and demodulation is implemented using the Inverse Discrete Fourier Transform (IDFT) and Discrete Fourier Transform (DFT). To implement an N/2 subchannel DMT system, an N size IDFT/DFT is required. The size is doubled by mirroring the data to impose conjugate symmetry in the frequency domain, which results in real-valued signal in the time domain after applying the IDFT. The general structure of a DMT system is illustrated in Figure 1, where $\{X_0, X_1, \ldots, X_{N-1}\}$ are the original complex QAM symbols, $\{x_n\}$ is the modulated data sequence, $\{y_n\}$ is the received sequence, and $\{Y_0, Y_1, \ldots, Y_{N-1}\}$ are the decoded complex QAM symbols. The IDFT and DFT are implemented very efficiently using the well known Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) algorithms.

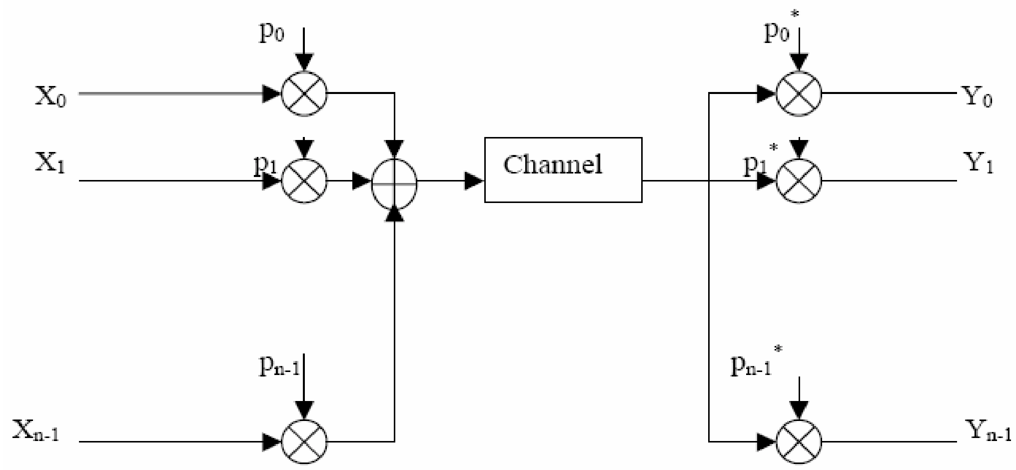

Figure 1. Basic Discrete Multi-tone scheme.

2.4. Initialization and Channel Identification

In order to optimize the bit allocation in the subchannels, the transmitter acquires an estimate of the channels' impulse response and crosstalk noise spectrum before the data transmission begins. This process is known as the initialization phase if it was before the first ADSL block symbol. Otherwise, if the estimates are acquired in the middle of the communication process between the transmitter and receiver, the process is known as channel identification phase. During these two phases the transmitter and receiver do the following: 1) Define a common mode of operation and clock and symbol synchronization, 2) identify the channel, 3) calculate the optimal bit and energy allocations for each subchannel, and 4) exchange the bit and energy allocation tables [5].

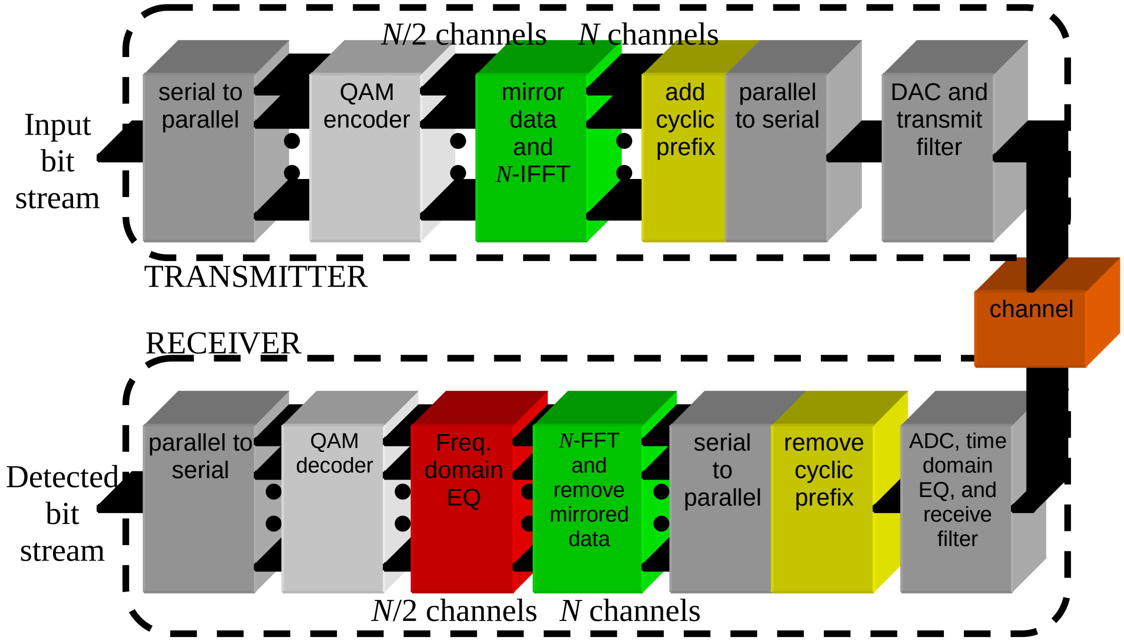

Figure 2. A block diagram of an ADSL Transceiver [6]

3. MODELING AND SIMULATION

3.1. ADSL Transmitter

In the ADSL transmitter shown in Figure 2, an input bit stream is first partitioned into substreams using a serial-to-parallel (S/P) converter. Each substream is then encoded using quadrature amplitude modulation (QAM), which produces a complex number representing each encoded bit substream as mentioned in an earlier section. The outputs of the QAM encoder are mirrored and conjugated before they enter an *N* point IFFT, where *N*/2 is the number of subchannels. The mirroring creates real values at the output of the IFFT. To mirror the data for M subchannels, N = 2M, the QAM symbols Xi are given by [1] as

$$X_i = \begin{cases} X_i & i = 1, \ldots, M-1 \\ \mathrm{Re}(X_M) & i = 0 \\ \mathrm{Im}(X_M) & i = M \\ X^*_{N-i} & i = M+1, \ldots, N-1 \end{cases} \quad [$$

.

The IFFT then maps each QAM symbol into orthogonal frequency bins producing a discrete multitone symbol of N samples. To form a frame, the last v samples of the symbol, known as the cyclic prefix (CP) are copied and prepended to the symbol. This provides a buffer against Interblock Interference (IBI), which was discussed earlier. Unfortunately the addition of the CP decreases the transceiver power efficiency by a factor of $N/(N+\nu)$ [7]. The final two stages serialize the data and convert it to analog via the parallel-to-serial (P/S) converter and digital-to-analog (DAC) converter respectively.

3.2 ADSL Receiver

An ADSL receiver receives the data through the channel, which is modeled as an FIR filter. The operation of the receiver is the dual of that of the transmitter, plus the addition of an equalizer. The equalizer has two tasks: 1) reduce ISI in the time domain and shorten the channel impulse response to the CP limit, and 2) compensate for magnitude and phase distortion in the frequency domain [7]. The first task is done by the time-domain equalizer (TEQ), while the latter is performed by the frequency-domain equalizer (FEQ).

4. PROPOSED WORK

The three models of computation that can be used to model the ADSL transceiver are Dynamic Data Flow (DDF), Synchronous Data Flow (SDF), and Timed Synchronous Dataflow (TSDF). Figure 3 illustrates the model that is used for each of the blocks in the ADSL transceivers based on the color of the node.

SDF is best for modeling Digital Signal Processing (DSP) communication systems because of the static number of inputs and outputs in each node, and the sequential transfer of data from one node to the next in an acyclic graph [8]. DDF is used in this model due to the initialization and channel identification phases, which dynamically change the bit allocation for each subchannel based on the channel estimates. TSDF is used to model continuous time after the conversion of data from digital to analog via the DAC.

My goal for this project is to model and simulate ADSL transceivers using SDF as the model of computation. If time permits, I will try to extend the modeling to include DDF and TSDF. In my simulations, I will attempt to evaluate the bit error rate for different combinations of channel models, TEQs, and bit allocation tables.

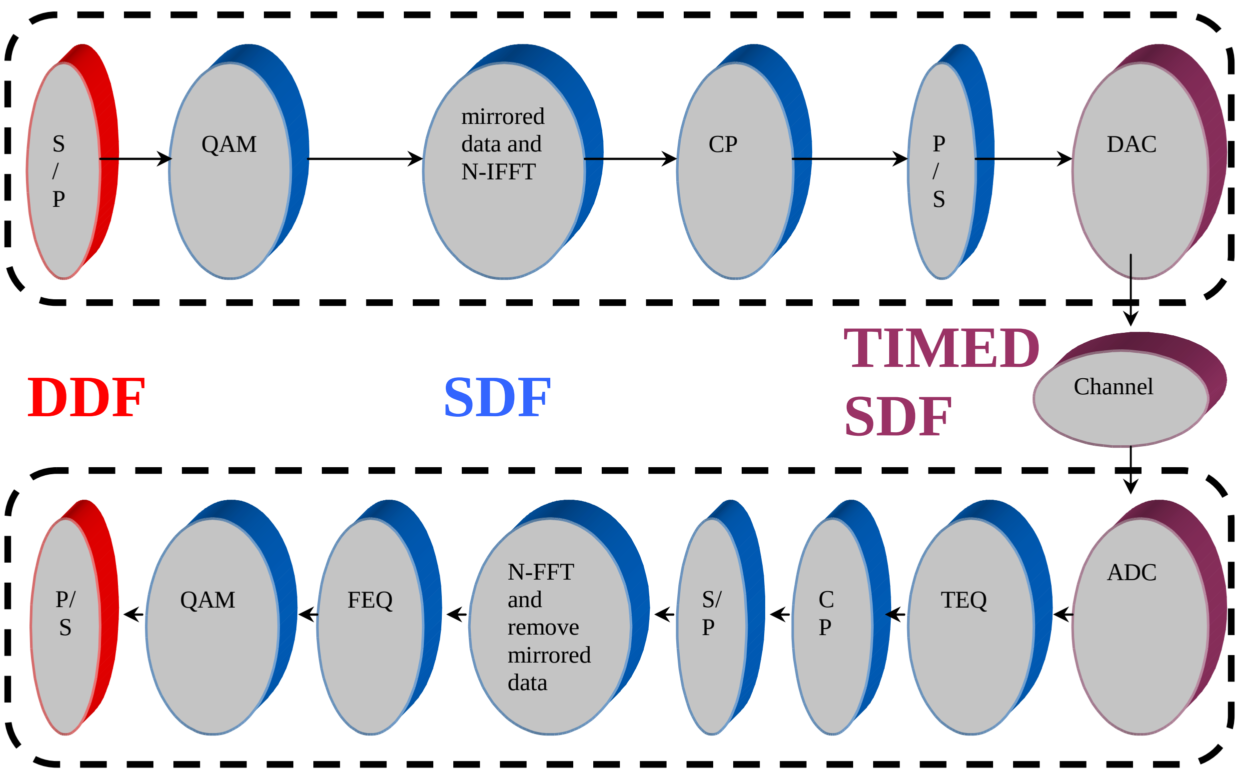

Figure 3. Models of Computations

5. REFERENCES

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