Embedded digital systems architecture — 2

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Pipelining

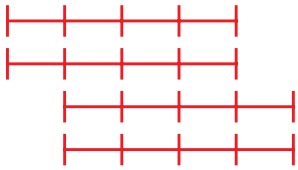
sequential

pipelined

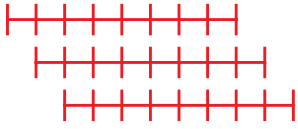
Typical DSP:

Fetch, Decode, Read, Execute

superscalar



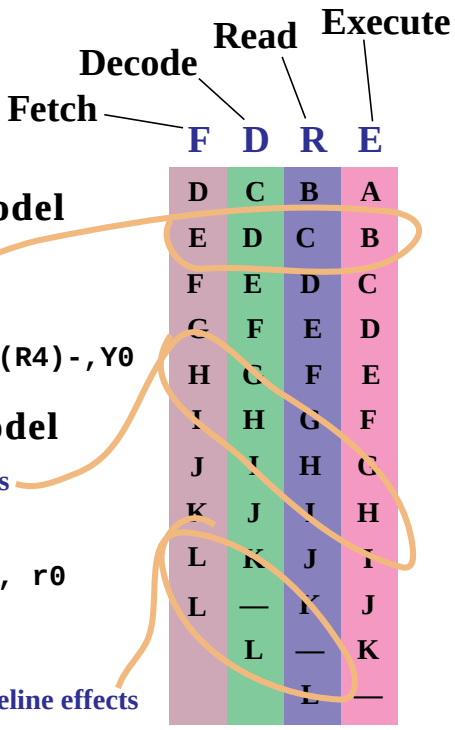
superpipelined



Managing pipelines

- compiler or programmer
- interlocking
- hardware instruction scheduling

Pipeline operation and programming style



- **Time-stationary** pipeline model
  - Programmer controls each cycle
  - Motorola DSP56001:

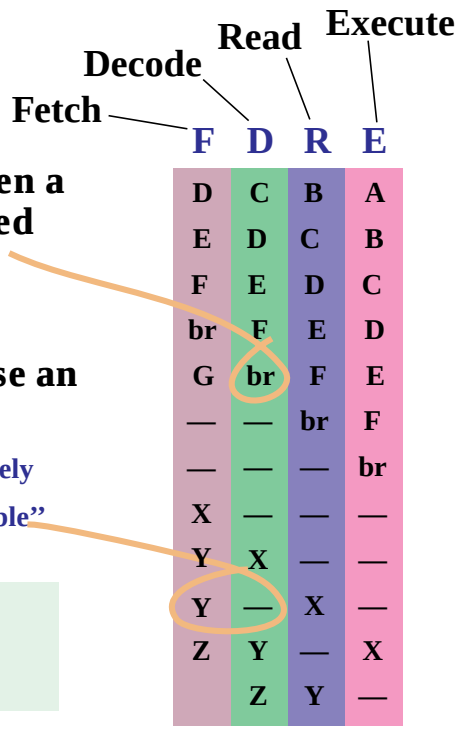
```
MAC X0,Y0,A  X:(R0)+,X0 Y:(R4)-,Y0
```

- **Data-stationary** pipeline model
  - Programmer specifies data operations
  - TMS320C30/40

```
mpyf *++ar0(1),*++ar1(ir0), r0
```

- **Interlocking** pipeline
  - Programmer is "protected" from pipeline effects

Pipeline hazards



- A **control** hazard occurs when a branch instruction is decoded
  - "Flush" the pipeline
  - or: Delayed branch (expose pipeline)
- A **data** hazard occurs because an operand cannot be read yet
  - Assume programmer did it deliberately
  - or: Interlock hardware inserts "bubble"

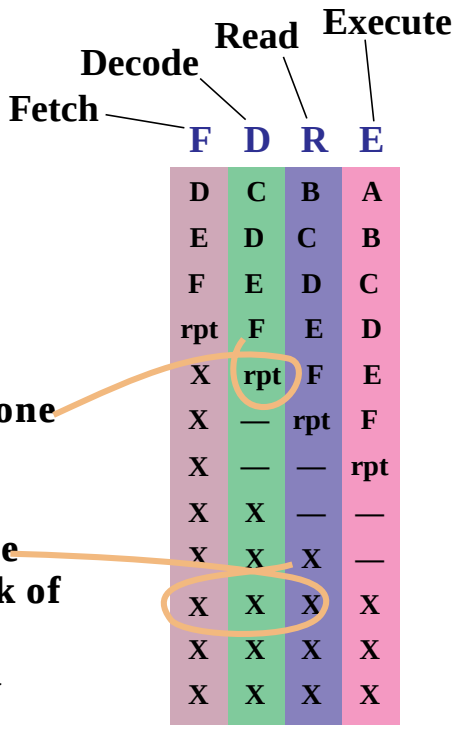
```
LAC #064h
SAMM AR2
NOP
NOP
LACC *-
```

```
LAR
AR2,DATA
LACC *-
```

Avoiding control hazards: hardware looping

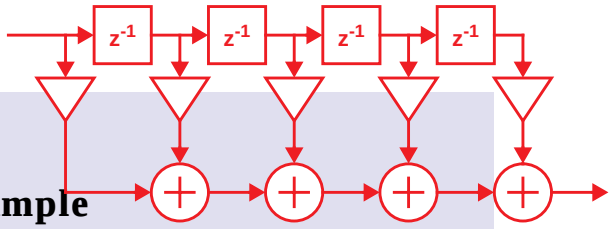
A key factor in the numeric performance of DSPs is the provision of special hardware to perform looping.

```
RPT   COUNT
TBLR  *+
```



- A repeat instruction repeats one or a block of following instructions
- The pipeline is filled with the repeated instruction (or block of instructions)
- Cost: one pipeline flush only

Overemphasized DSP benchmark: an FIR filter



Each tap requires

- fetching one data sample
- fetching one operand
- multiplying
- accumulating
- shifting one sample in the delay line

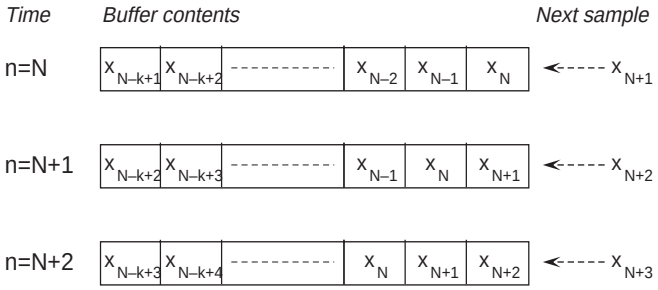
Implies of the architecture:

- at least 3 memory accesses per instruction
- auto-increment or decrement addressing modes

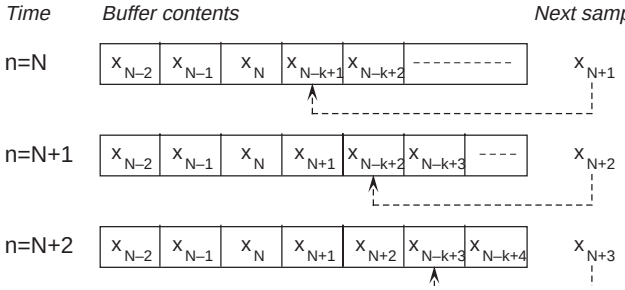
DSP-specific addressing features

- **modulo addressing**
  - implements circular buffers and delay lines
- **bit reversed addressing**
  - used to implement the radix-2 FFT

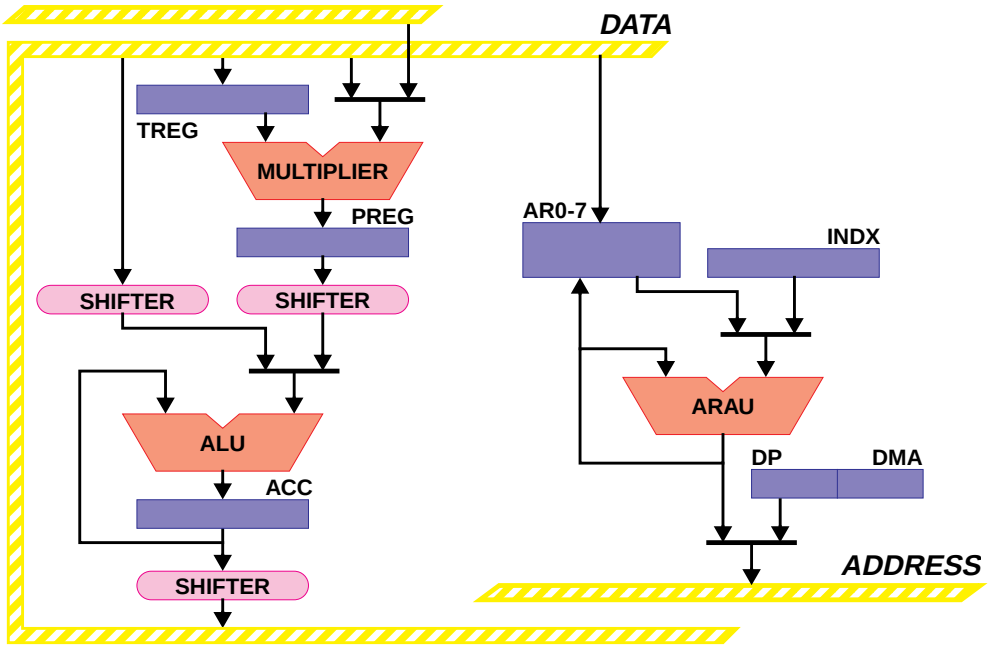
Data-shifting



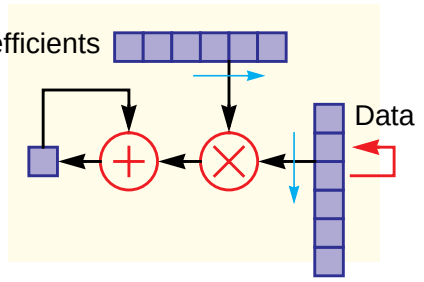
Modulo addressing



Simplified TMS320C50 Architecture



FIR Filter in TMS320C50



Memory locations

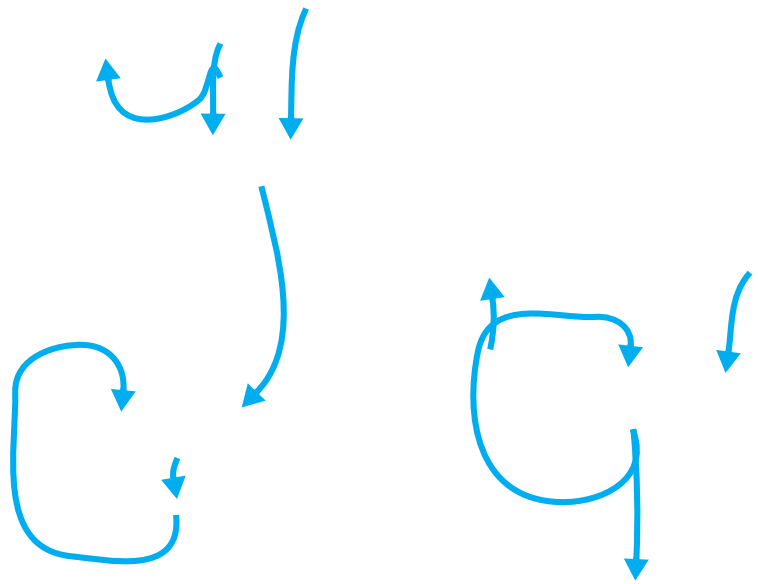
```
COEFFP  .set 02000h     ; Program mem address
X       .set 037Fh      ; Newest data sample
LASTAP  .set 037FH      ; Oldest data sample

        ...
        LAR   AR3,#LASTAP   ; Point to oldest sample
        RPT   #127
        MACD  COEFFP,*-     ; Do the thang
        APAC
        SACH  Y,1           ; Store result -- note shift
```

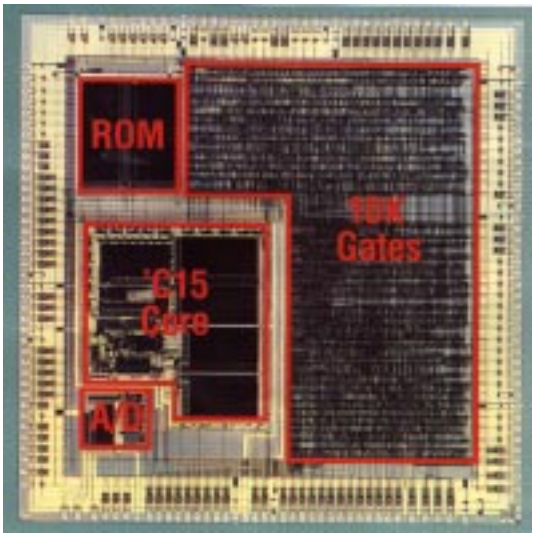
Single-cycle loop

Clean-up

Initialize



DSP Cores



TMS320 cDSP (Customizable DSP)
from Texas Instruments

Graphic courtesy of Texas Instruments, Inc.

ASIC with:

- **Programmable DSP**
- **RAM**
- **ROM**
- **Standard Cells**
- **Codec**
- **Peripherals**
- **Gate array**
- **Microcontroller**