Design of Sparse Filters for Channel Shortening

Aditya Chopra and Prof. Brian L. Evans

Department of Electrical and Computer Engineering
The University of Texas at Austin

Introduction

Finite Impulse Response (FIR) model of transmission media

- Signal distortion during transmission
- Frequency selectivity of communicating medium
- Multipath and reverberation
- Typically referred to as 'channel'

Channel delay spread

- Duration of time for which channel impulse response contains significant energy
- Large delay spread may be detrimental to high-speed communications
 - Leads to inter-symbol interference [Bingham, 1990]

Introduction

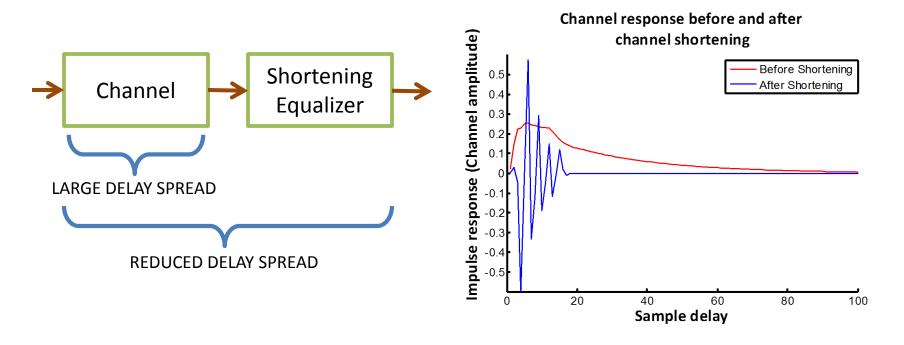
Discrete Multi-Tone (DMT) Modulation

- Typically used in high-speed wireline communications (eg. ADSL)
- Data transmission in parallel over multiple carriers
- Cyclic prefix (CP) is used to combat ISI
 - Effective if channel delay spread shorter than CP length



Channel Shortening

- Signal processing algorithms designed to reduce delay spread
 - Equalizer design to reduce delay spread of combined channel and shortening filter



Channel Shortening Equalizer Design

Maximum shortening SNR criterion [Martin et al., 2005]

- Shortening SNR (SSNR) defined as ratio of channel energy within cyclic prefix to channel energy outside cyclic prefix of length $L_{\it CP}$
- For a discrete time channel h

$$\mathbf{h}_{win} = \mathbf{h}_{(0,1,\cdots L_{CP}-1)}$$

$$\mathbf{h}_{wall} = \mathbf{h}_{(L_{CP},L_{CP}+1,\cdots \infty)}$$

$$SSNR = \frac{Channel\ Energy}{ISI\ Energy} = \frac{\mathbf{h}_{win}^H \mathbf{h}_{win}}{\mathbf{h}_{wall}^H \mathbf{h}_{wall}}$$

Design Problem

Design equalizer \mathbf{w}_{opt} constrained to length L to maximize SSNR of $\mathbf{h} * \mathbf{w}_{opt}$

Channel Shortening Equalizer Design

Optimal solution [Melsa et al., 1996]

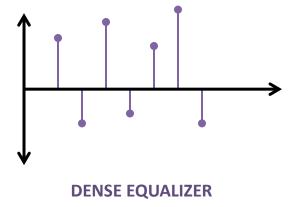
$$\mathbf{w}_{opt} = \sqrt{\mathbf{H}_{win}^H \mathbf{H}_{win}}^{-T} \mathbf{q}_{min}$$

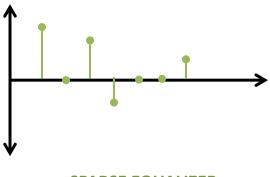
- \mathbf{q}_{min} is the eigenvector corresponding to minimum eigenvalue of $\sqrt{\mathbf{H}_{win}^H\mathbf{H}_{win}}$ $\mathbf{H}_{wall}^H\mathbf{H}_{wall}\sqrt{\mathbf{H}_{win}^H\mathbf{H}_{win}}$
- \mathbf{H}_{win} and \mathbf{H}_{wall} are Toeplitz matrices corresponding to vectors \mathbf{h}_{win} and \mathbf{h}_{wall} respectively

Sparse Filters

FIR filters with non-consecutive non-zero taps

- Typically referred to as sparse filters
- Larger delay spread than dense filters
- Filtering requires same complexity as dense filter with equal number of non-zero taps
- E.g. RAKE receiver structure in CDMA communications





SPARSE EQUALIZER

Sparse Equalizer Design

Design problem

- Design equalizer \mathbf{w}_{opt} , constrained to L non-zero taps and maximum delay of M, to maximize SSNR of $\mathbf{h} * \mathbf{w}_{opt}$

Optimal solution (exhaustive search)

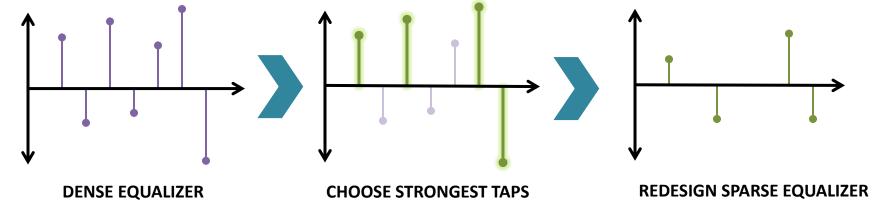
- 1. Define a set S of indexing matrices P_i $P_i(j,k) = \begin{cases} 1 & \text{if the } j^{th} \text{ non-zero tap of } \mathbf{w} \text{ is at sample delay } k \\ 0 & \text{otherwise} \end{cases}$
- 2. Design $\mathbf{w}_{i,opt}$ using $\mathbf{H}_{win}\mathbf{P}_i$ and $\mathbf{H}_{wall}\mathbf{P}_i \ \forall i = 1, ... |\mathcal{S}|$
- 3. \mathbf{w}_{opt} is the equalizer $\mathbf{w}_{i,opt}$ with highest SSNR $\forall i = 1, ... |\mathcal{S}|$

$$- |\mathcal{S}| = \binom{M-1}{L-1}$$

Low Complexity Equalizer Design

'Strongest tap selection' method

- 1. Design large length dense filter and choose a subset of strongest taps
- 2. Design sparse filter on the selected locations



Features

- Suboptimal
- Lower computational complexity than optimal design method
- Similar approach used in G-RAKE receiver [Fulghum et al.,2009]

Computational Complexity Analysis

Design + Runtime model of communication

- Modem performs channel estimation and equalizer design during initial training stage
- Equalizer coefficients are stored and used during data transmission
- Assumption: Data transmission duration is much longer than training

TEQ Stage (Equalizer type)	Computational Complexity (Multiplications)
Design (Original)	$\mathcal{O}(L^3)$
Design (Sparse – Exhaustive)	$\mathcal{O}\left(L^3 \binom{M-1}{L-1}\right)$
Design (Sparse – Heuristic)	$\mathcal{O}(L^3 + M^3)$
Runtime	$\mathcal{O}(LR)$

L: NUMBER OF NON-ZERO TAPS M: MAX FILTER DELAY R: SAMPLING RATE

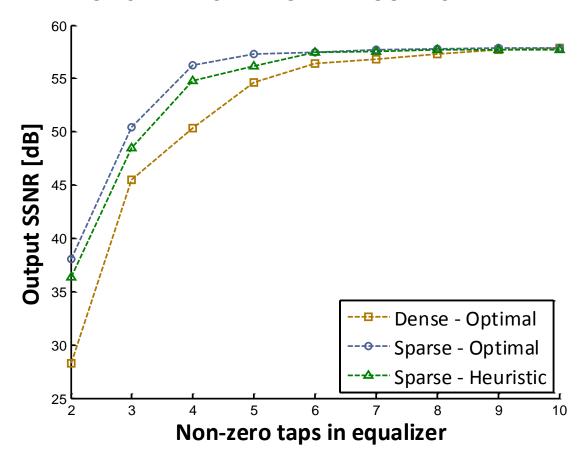
Simulation Parameters

- Simulate sparse equalizers on Carrier Serving Area Loop channel models
 - Typically used in DMT

Parameter	Value	
Sampling Rate	2.208 MHz	
Symbol Length	512 samples	
Cyclic Prefix Length	32 samples	
Maximum tap delay (M)	10	
Channel Model	ADSL Carrier Serving Area Loop 1	

Channel Shortening Performance

CHANNEL SHORTENING SNR PERFORMANCE VS. NUMBER OF NON-ZERO EQUALIZER TAPS
FOR CARRIER SERVING AREA LOOP 1 CHANNEL



Computation Complexity

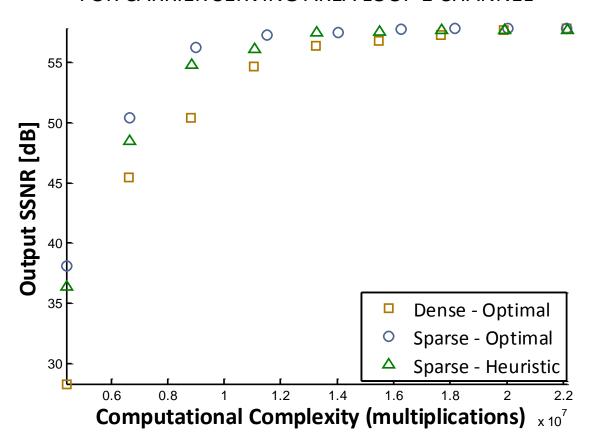
Comparison of computational complexity for various equalizer design methods

- Filter Length is number of non-zero taps in equalizer
- M = 10 for sparse equalizers
- Design complexity is number of multiplication operations
- Design + Runtime complexity is multiplication operations required for filter design and 1 second of filter operation at R = 2.208 MHz

Equalizer Type	Filter Length	Design Complexity	Design + Runtime Complexity
Dense	L = 8	14106	18254016 (100%)
Sparse – optimal	L = 6	780192	14460192 (79.22%)
	L = 4	169344	9289344 (50.89%)
Sparse – heuristic	L = 6	32832	13712832 (75.12%)
	L = 4	28656	9148656 (50.12%)

Equalizer Design Tradeoff

CHANNEL SHORTENING SNR PERFORMANCE VS. DESIGN + 1 SEC. RUNTIME COMPLEXITY FOR CARRIER SERVING AREA LOOP 1 CHANNEL



Summary

Sparse shortening equalizer design

- High computational complexity requirements for design
- Favorable for few non-zero coefficients
- Reconcile increased design computation by improved communication performance during data transmission

Applications

- Channel shortening equalizers in ADSL systems
- RAKE receivers in CDMA systems
- Equalizers in underwater acoustic communications

References

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Thank you!