Analog-to-Digital Converter Circuit and System Design to Improve with CMOS Scaling

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PHD DEFENSE

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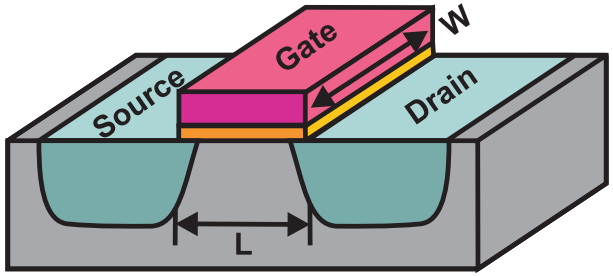
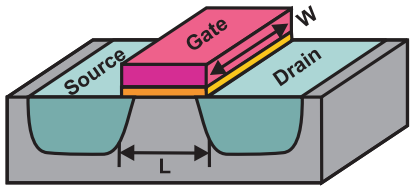
Wireless Networking & Communications Group

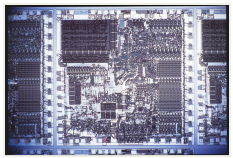
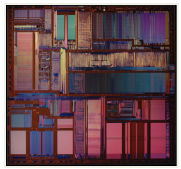
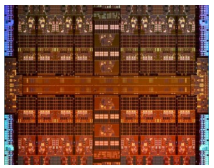
CMOS Scaling of Digital Integrated Circuits





Metal-Oxide-Semiconductor (MOS) Transistor

- Scaling CMOS transistor dimensions results in
  - exponential increase in number of transistors per chip [Moore's law]
  - lower capacitance, delay, active power dissipation, cost

Feature size	3 µm	0.8 µm	16 nm
# of Transistors	29K	3.1M	10B+
Die Photo/Year	 Intel x86 (1978)	 Intel Pentium (1993)	 Oracle Sparc M7 (exp: 2015)

Source: http://en.wikipedia.org/wiki/Transistor_count

CMOS Scaling of Mixed-Signal/Analog Circuits

- Analog circuits generally don't scale like digital circuits
- State-of-the art CMOS processes are digital-friendly, but analog-hostile

Good:

reduced: capacitance, active power
increased: speed

Bad:

reduced: supply voltage, voltage headroom

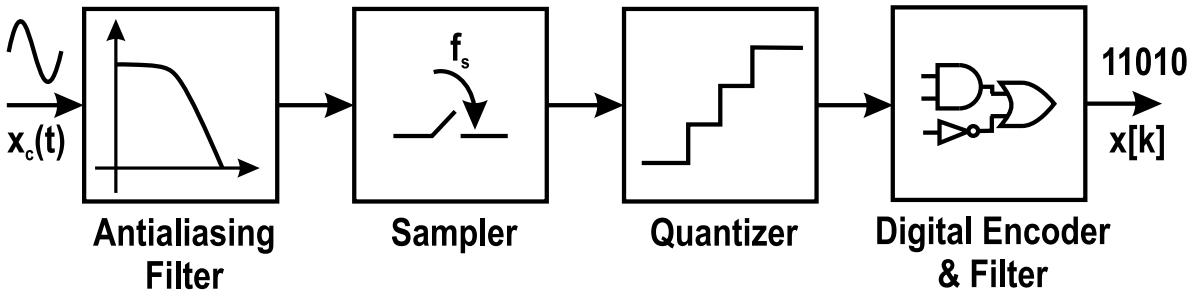
Ugly:

increased: mismatch, noise, short-channel effects, nonlinearity
reduced: intrinsic transistor gain, signal-to-noise ratio, dynamic range

"Good, Bad, Ugly" sketch courtesy of Kevin Graham: http://www.kevingrahamart.com/

Analog-to-Digital Converters

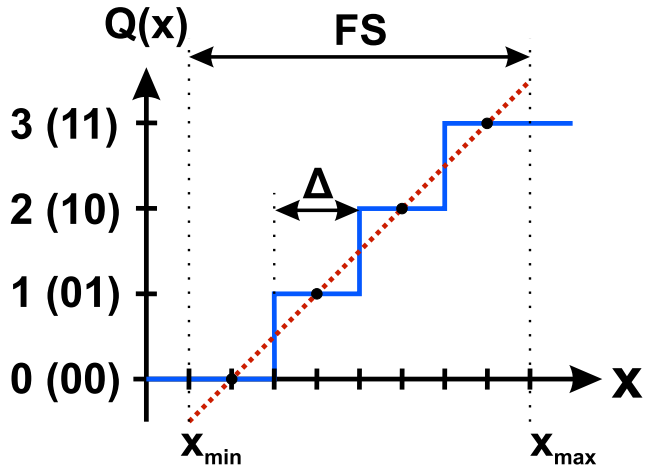
- Typical ADC:



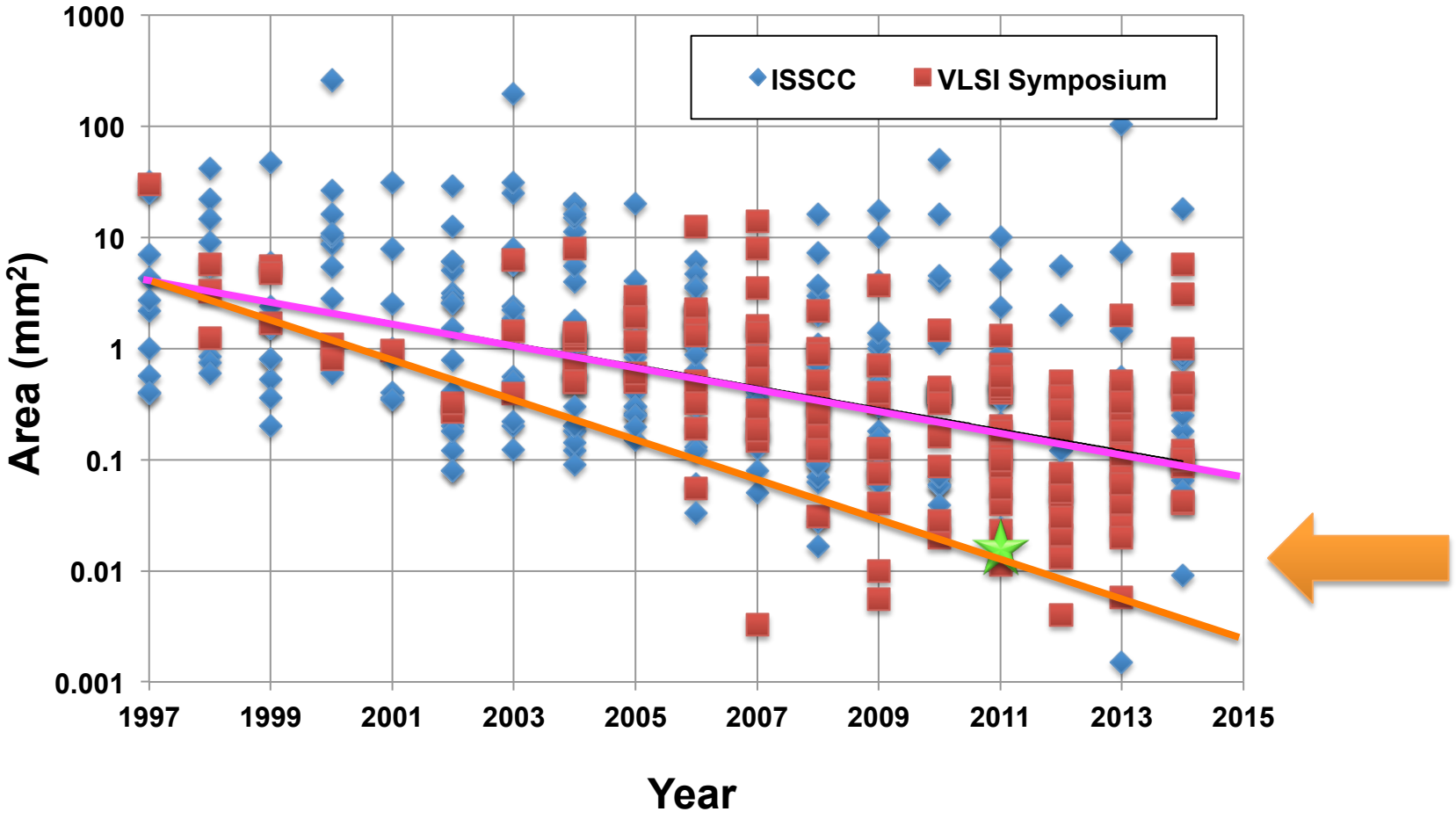
- Antialiasing filter (ideally) enforces band-limitedness to BW
- Sampling is lossless if $f_s > 2$ BW (Nyquist rate)
- Quantization is lossy, *i.e.* it adds noise

$$\sigma_q^2 = \frac{\Delta}{12} \qquad \Delta = \frac{FS}{2^N}$$

- Signal-to-quantization noise ratio:
  SQNR = 6.02 N + 1.76 (dB)



Analog-to-Digital Converter Area Trend



B. Murmann, "ADC Performance Survey 1997-2015," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

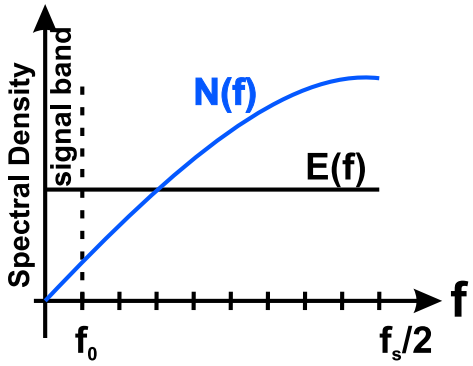
Contributions

Analog-to-Digital Converter Circuit and System Design to Improve with CMOS Scaling

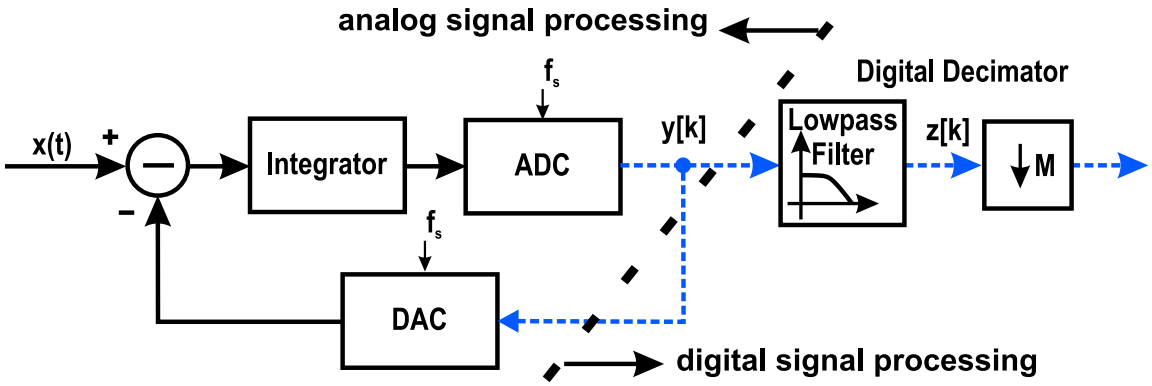
Time-Based Delta Sigma ADC Architecture & Modeling	• Novel architecture with loop delay calibration • Combines time-based information processing & noise shaping
Two Prototype ADC Chips	• Prototype chips demonstrate proof of concept • Among smallest area in literature
Nonlinearity Estimation and Correction	• Up to 16 dB improvement in SNDR with digital calibration • Diagnostic tool for identifying linearity bottleneck

Delta Sigma Modulation (DSM)

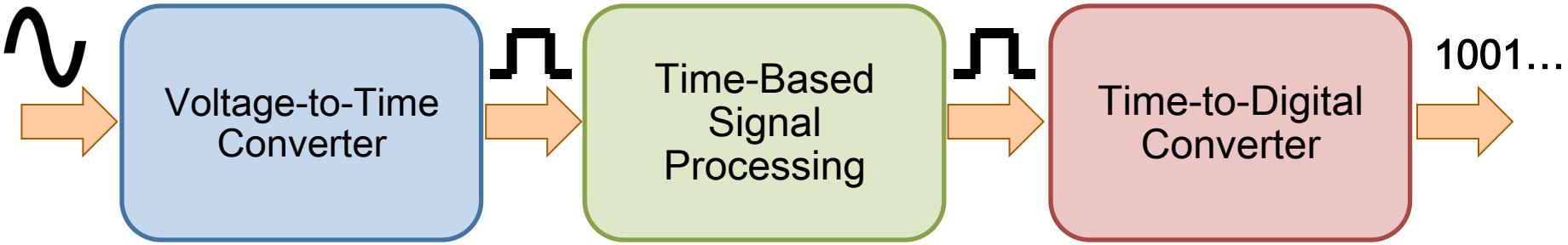
- Idea:
  - start with low-resolution quantizer (1 to few bits)
  - use feedback to shape noise spectrum as high-pass, and
  - use oversampling and digital lowpass filtering to reduce noise



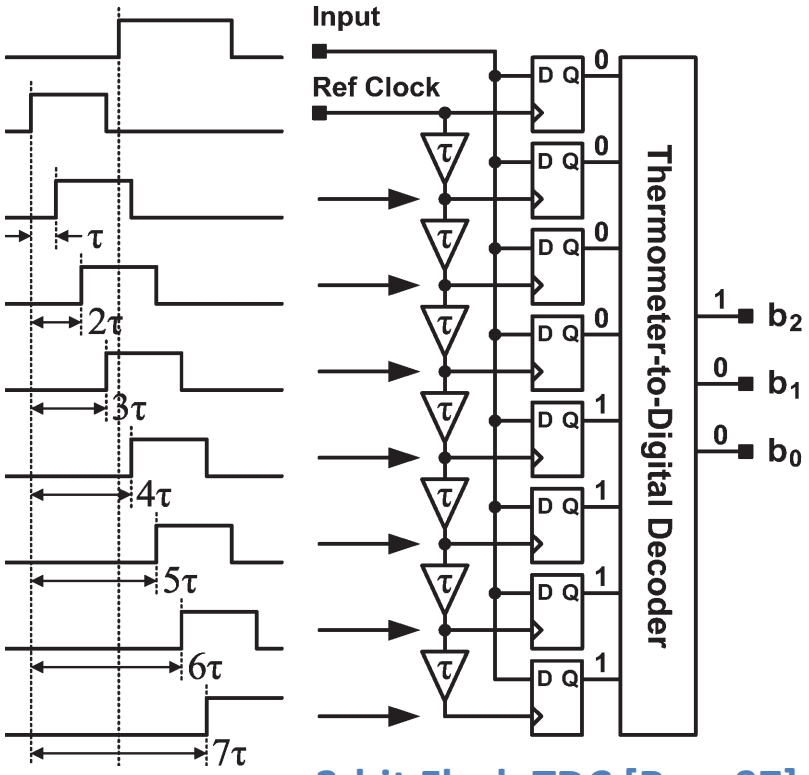
1st Order DSM



Time-Based Signal Processing



- Benefits from scaling perspective:
  - Improved timing accuracy with CMOS scaling
  - Digital implementation
  - Not thermal noise limited, no need for large capacitances



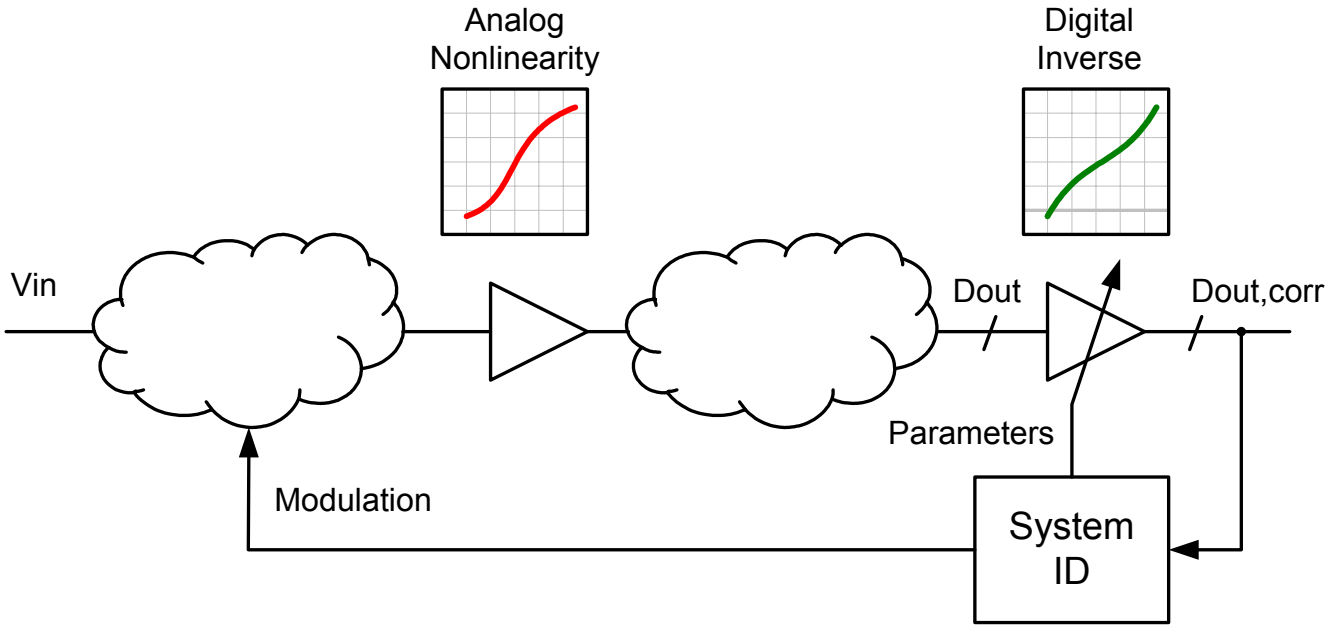
3-bit Flash TDC [Roza97]

Digitally-Assisted Analog Scheme

- A trend in the literature, to improve analog circuit performance through digital methods [Murmann2010]

- The availability of cheap (power/area) digital circuits makes these methods more attractive as processes scale.

- Example:

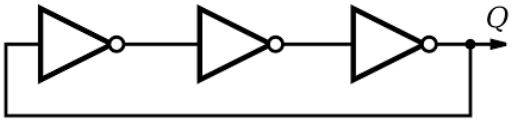


Thesis Statement

Architect low-area delta-sigma data converters that scale with CMOS technology by replacing voltage-domain with time-domain processing.

Prior Art

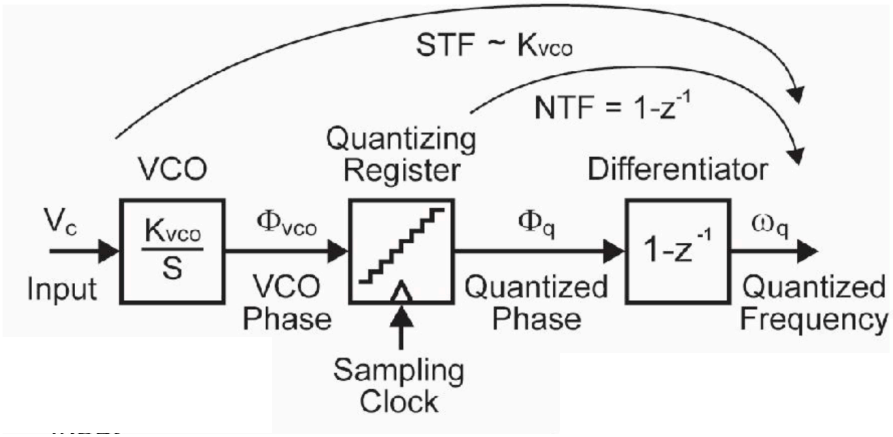
- Voltage Controlled Oscillator (VCO)-Based Delta Sigma ADC

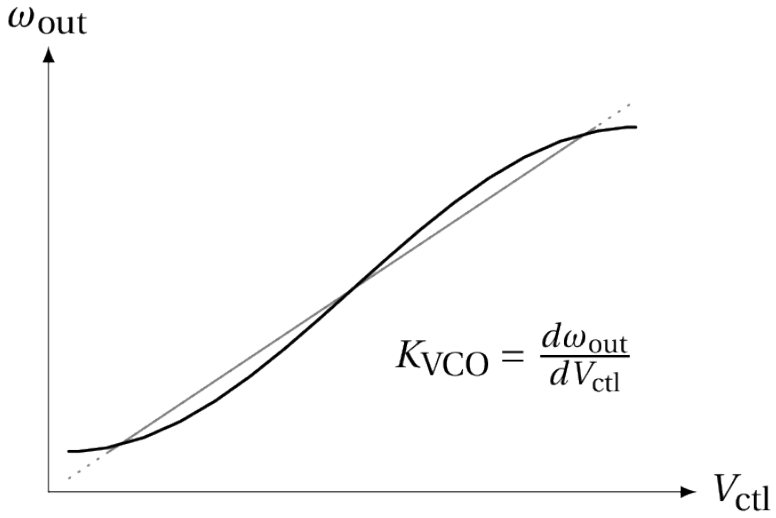


- Time-Based Delta Sigma ADCs
  - Using asynchronous delta sigma modulator
  - Time-to-Digital Converters (TDCs)

VCO-Based Delta Sigma ADC

- Continuous-time integration (1/s) is inherent.
- Sampling VCO phase at periodic intervals gives quantized phase.
- VCO nonlinearity (K_{VCO}) is an important limitation.
  - [Rao2011] proposes two-level PWM modulator to avoid the problem
  - [Taylor2013] uses digital calibration and post-correction to mitigate the problem

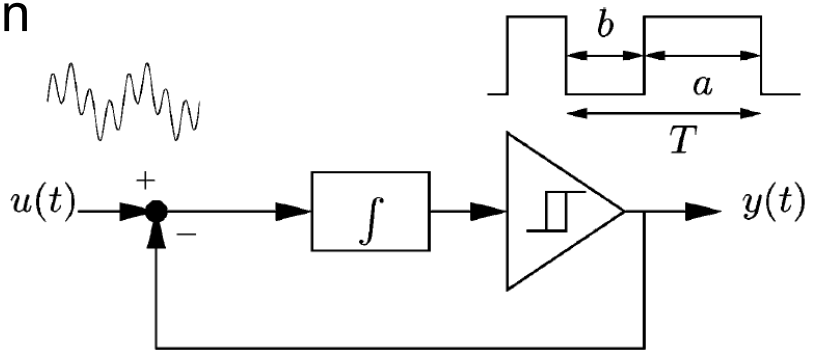




Prior Art

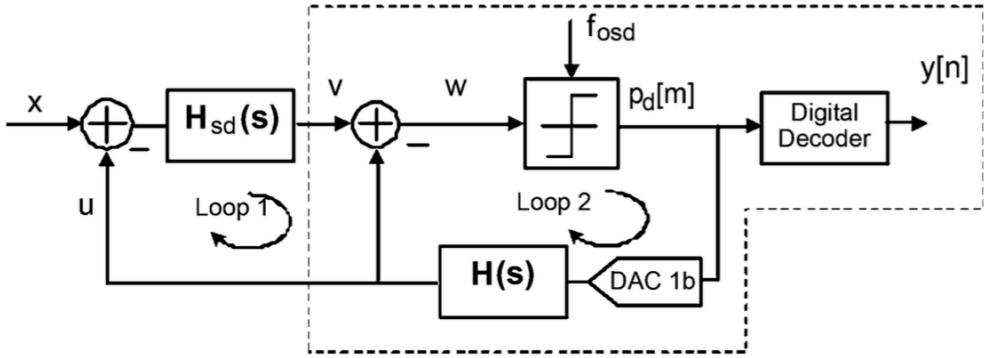
- Time-Based Delta Sigma ADCs
  - Asynchronous delta-sigma modulation

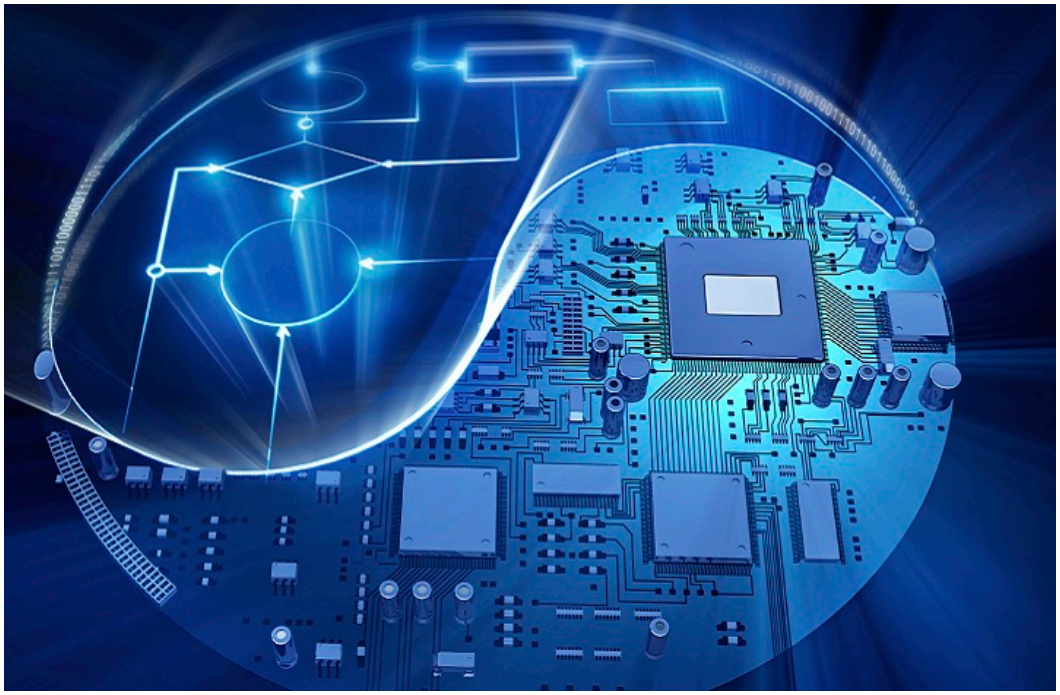
    [Dhanasekaran2009, Taillefer2009, Daniels2010]



  - Time Encoding Quantizer (TEQ)-based ADCs

    [Prefasi2009]





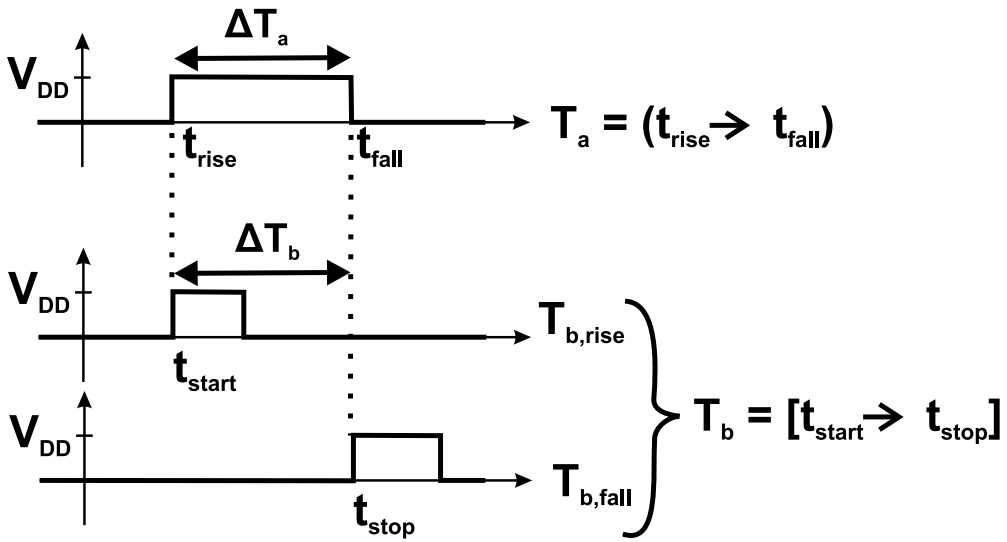
Time-Based Delta Sigma ADC Architecture & Modeling

Image source: http://www.intel.de/content/www/de/de/cofluent/intel-cofluent-studio.html

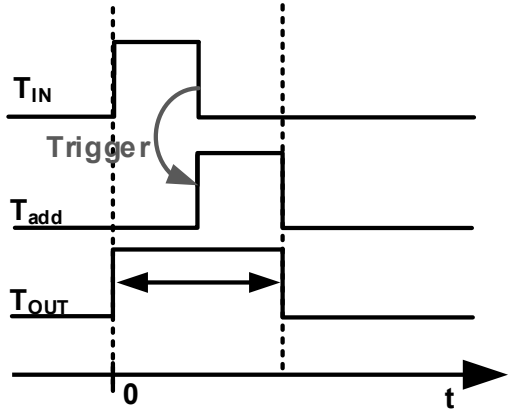
Time-Based Processing Encoding/Operands

Conventional Pulse

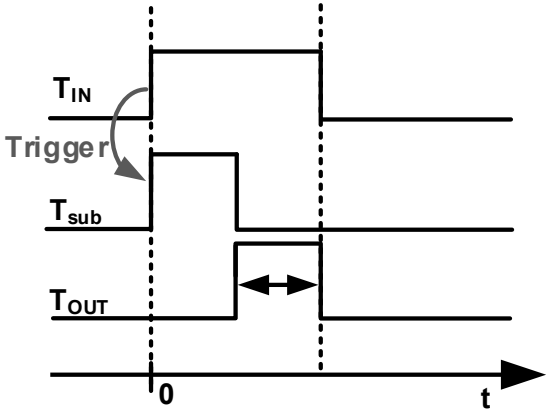
Pseudo-Differential Pulses



Pulse Width Addition



Pulse Width Subtraction



System Model

Voltage-to-Time Converter (VTC)/Adder

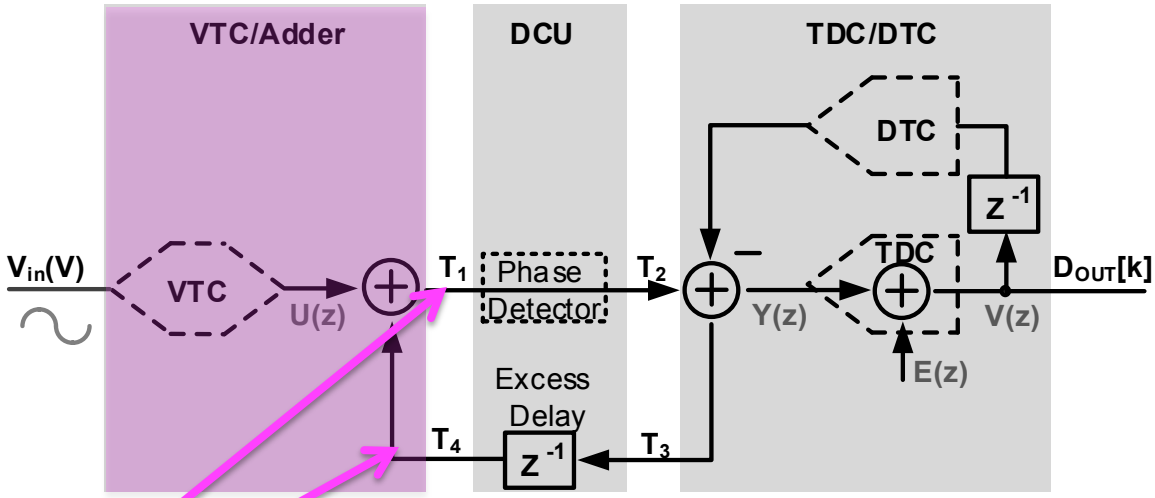
Samples

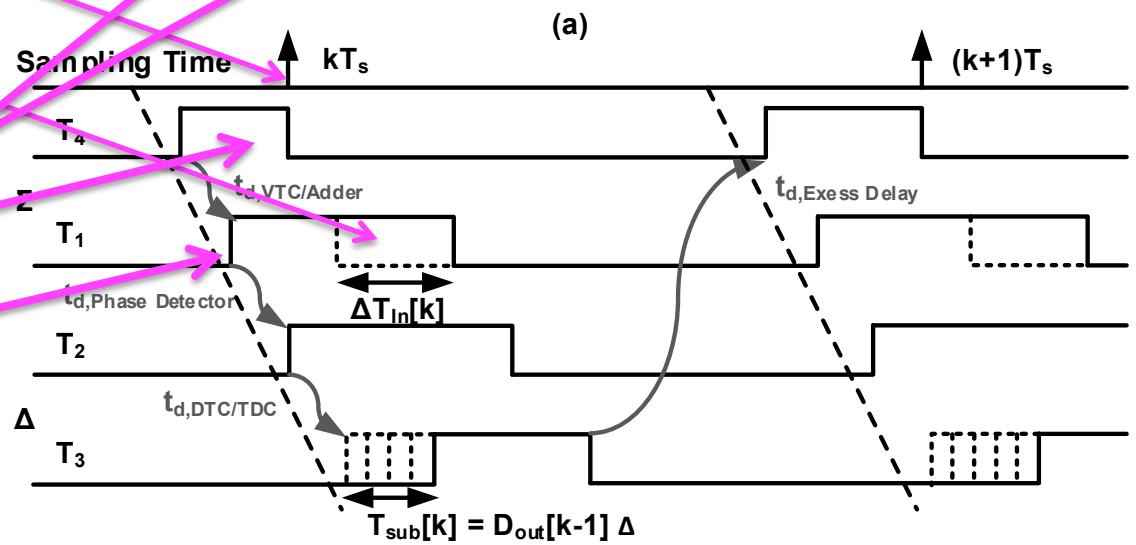
Vin @ t = kT_s

Converts it to $\Delta T_{in}[k]$

Adds it to the feedback pulse T_4

Result = T_1





System Model

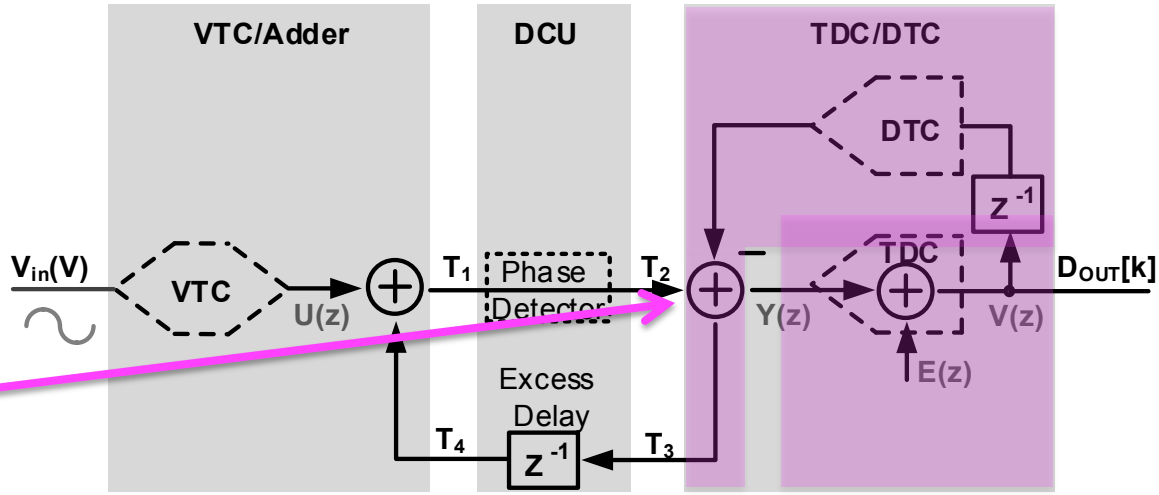
Digital-to-Time Converter (DTC)

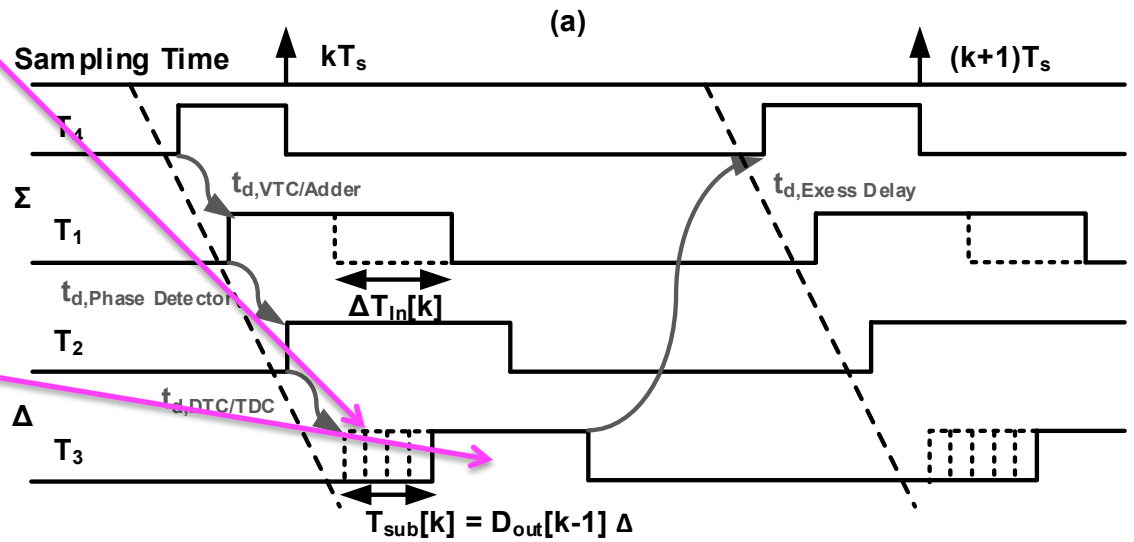
Subtracts from T_2 $D_{out}[k-1]$ units

Time-to-Digital Converter (TDC)

quantizes the result to get

$D_{out}[k]$





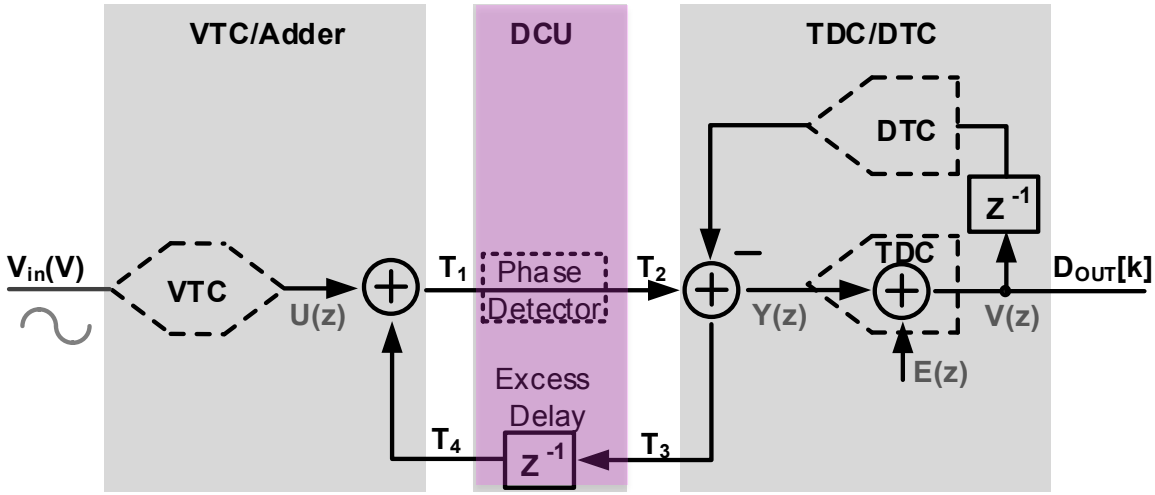
System Model

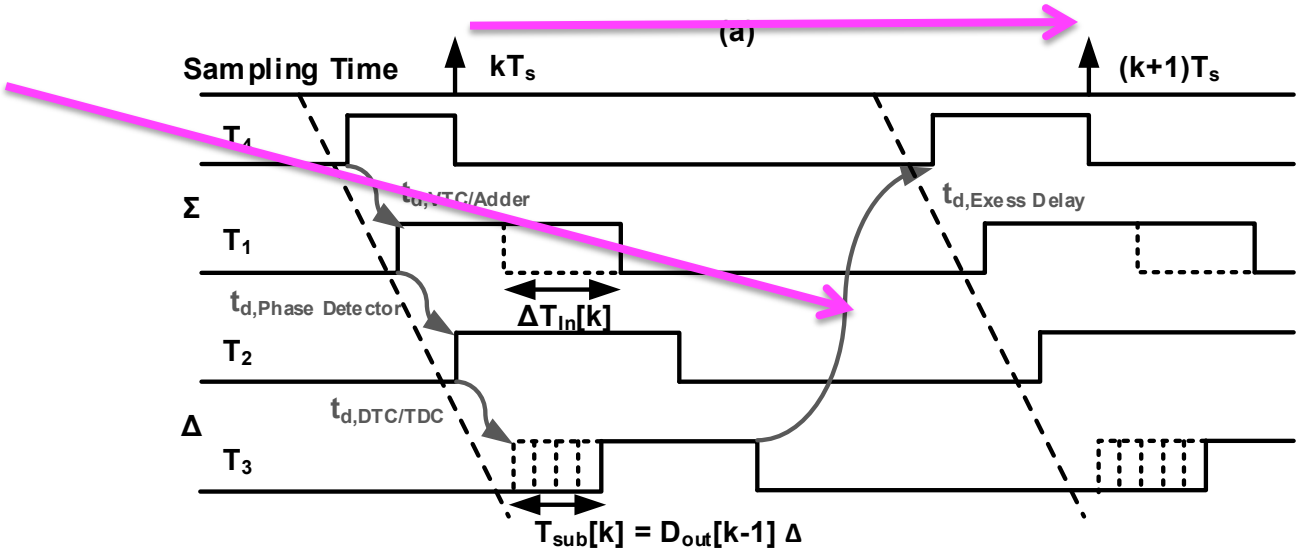
Delay Control Unit (DCU) and **Excess Delay**

ensure uniform sampling

by adjusting

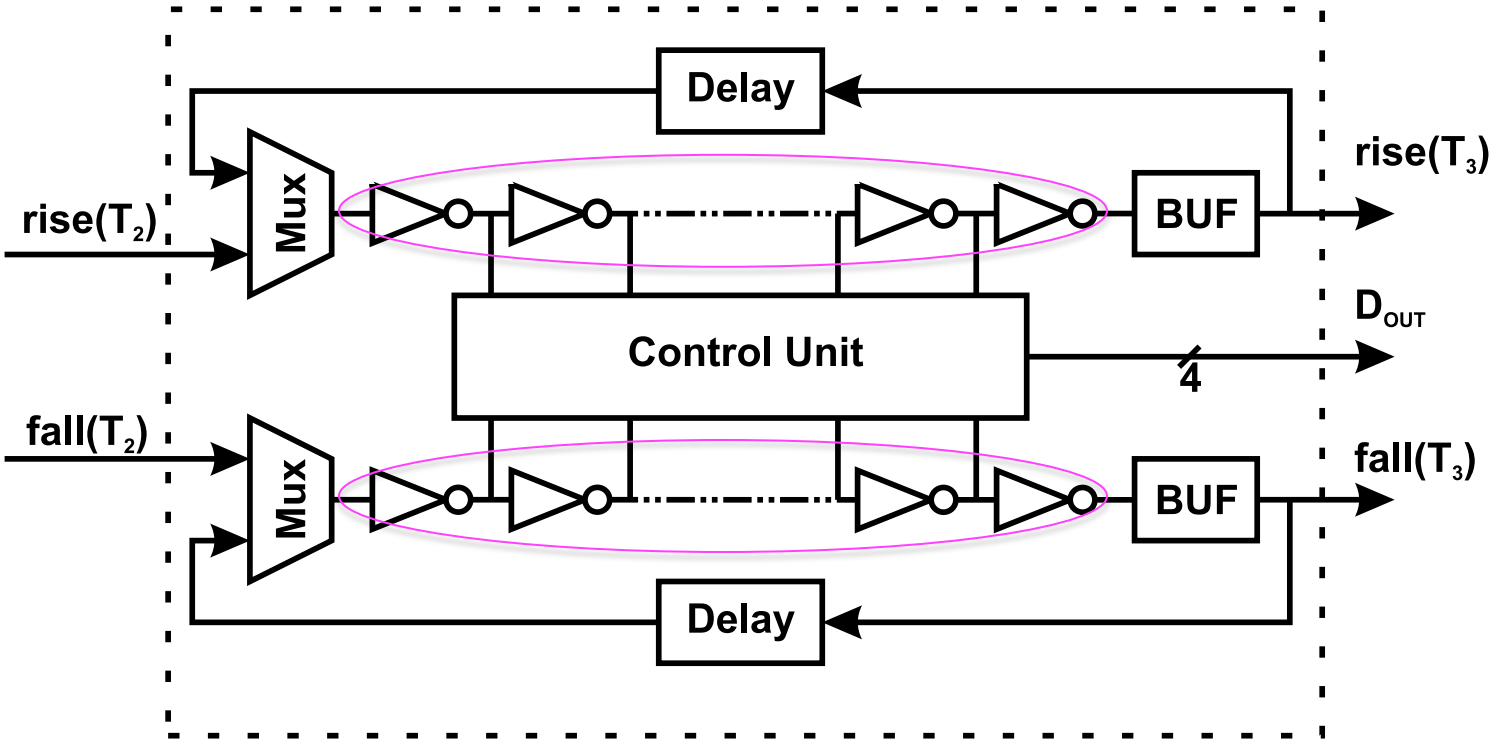
$t_{d,\ Excess\ Delay}$



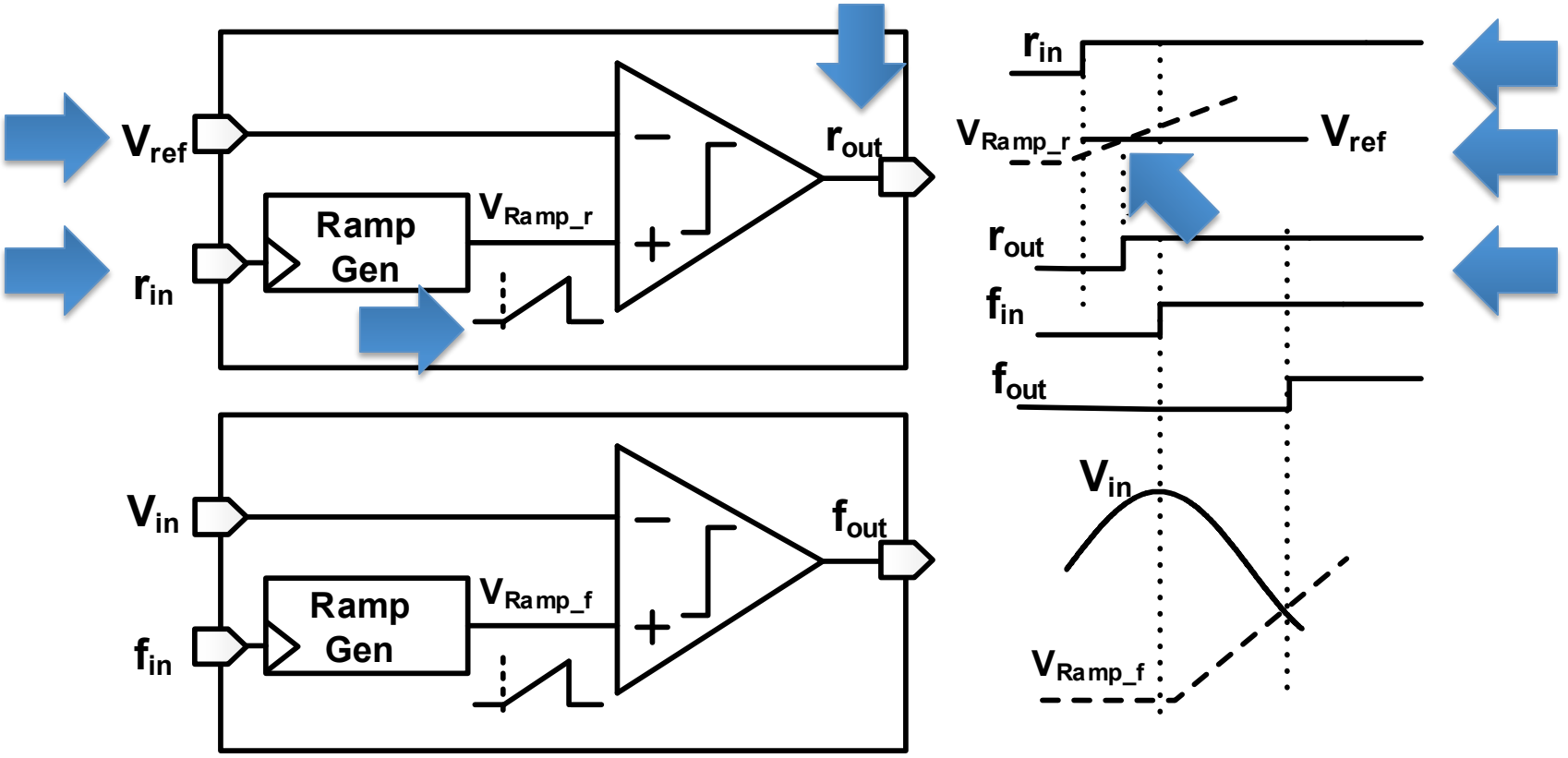


TDC/DTC

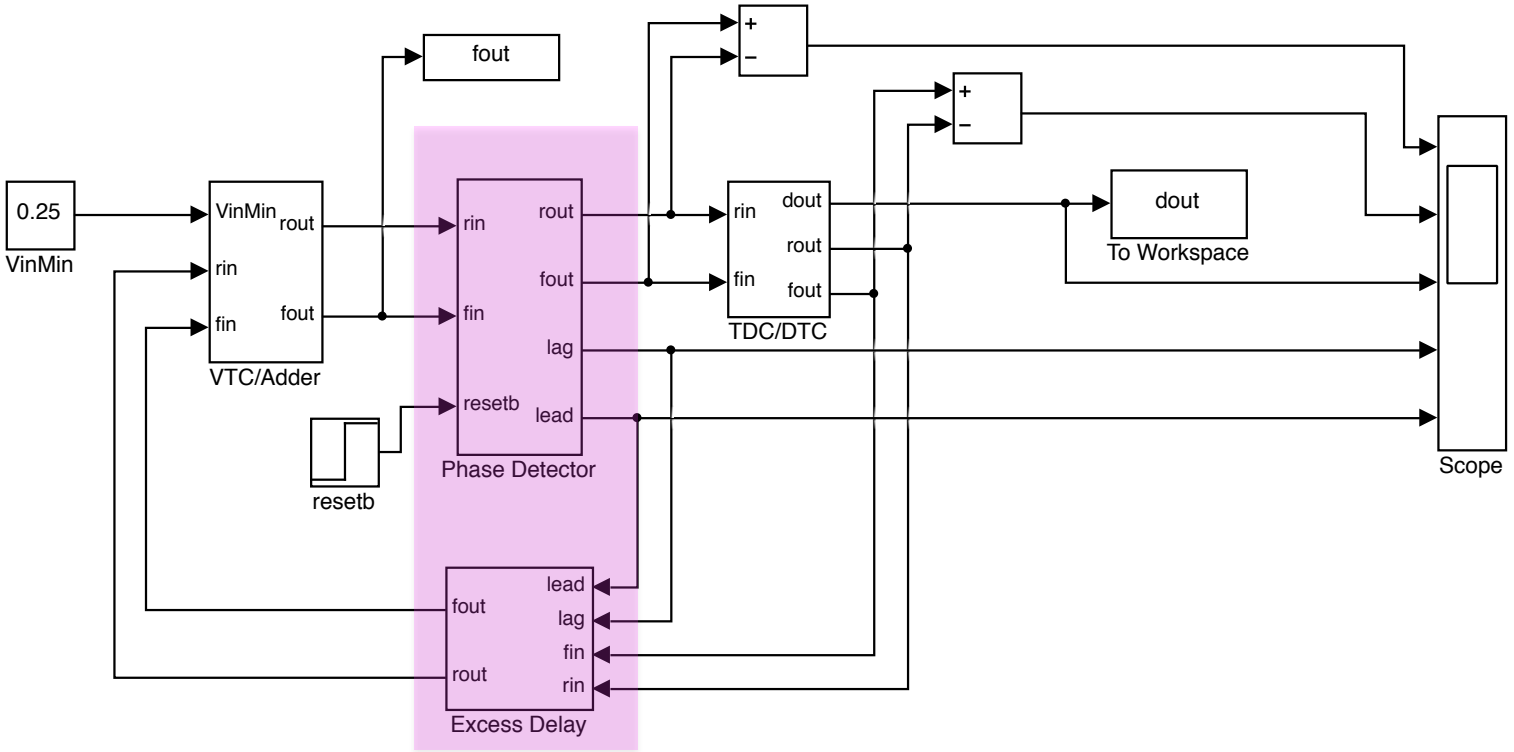
- TDC = Time-to-Digital Converter
- DTC = Digital-to-Time Converter



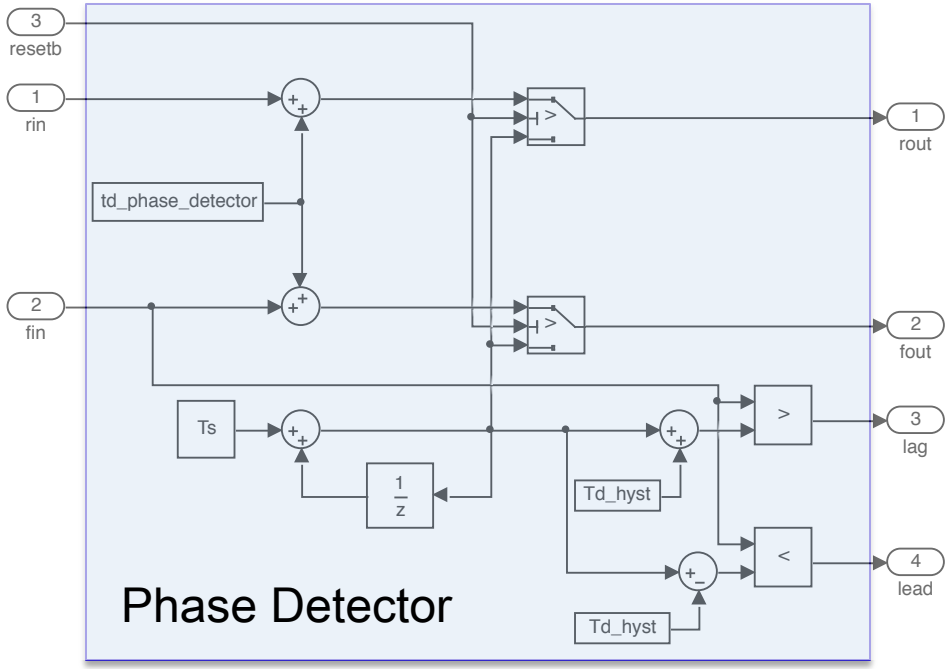
Voltage-to-Time Converter/Adder

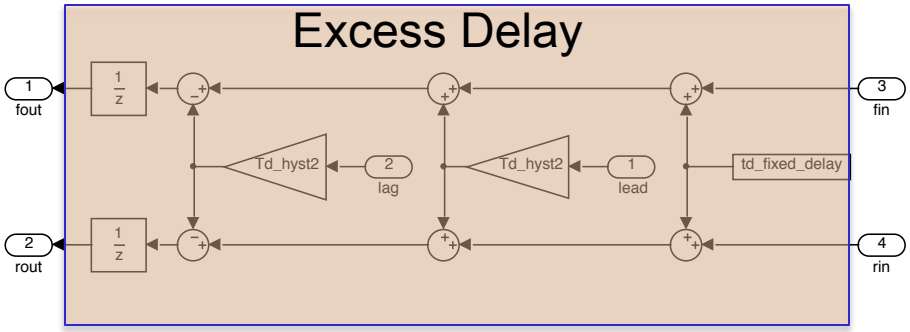


Simulink Modeling

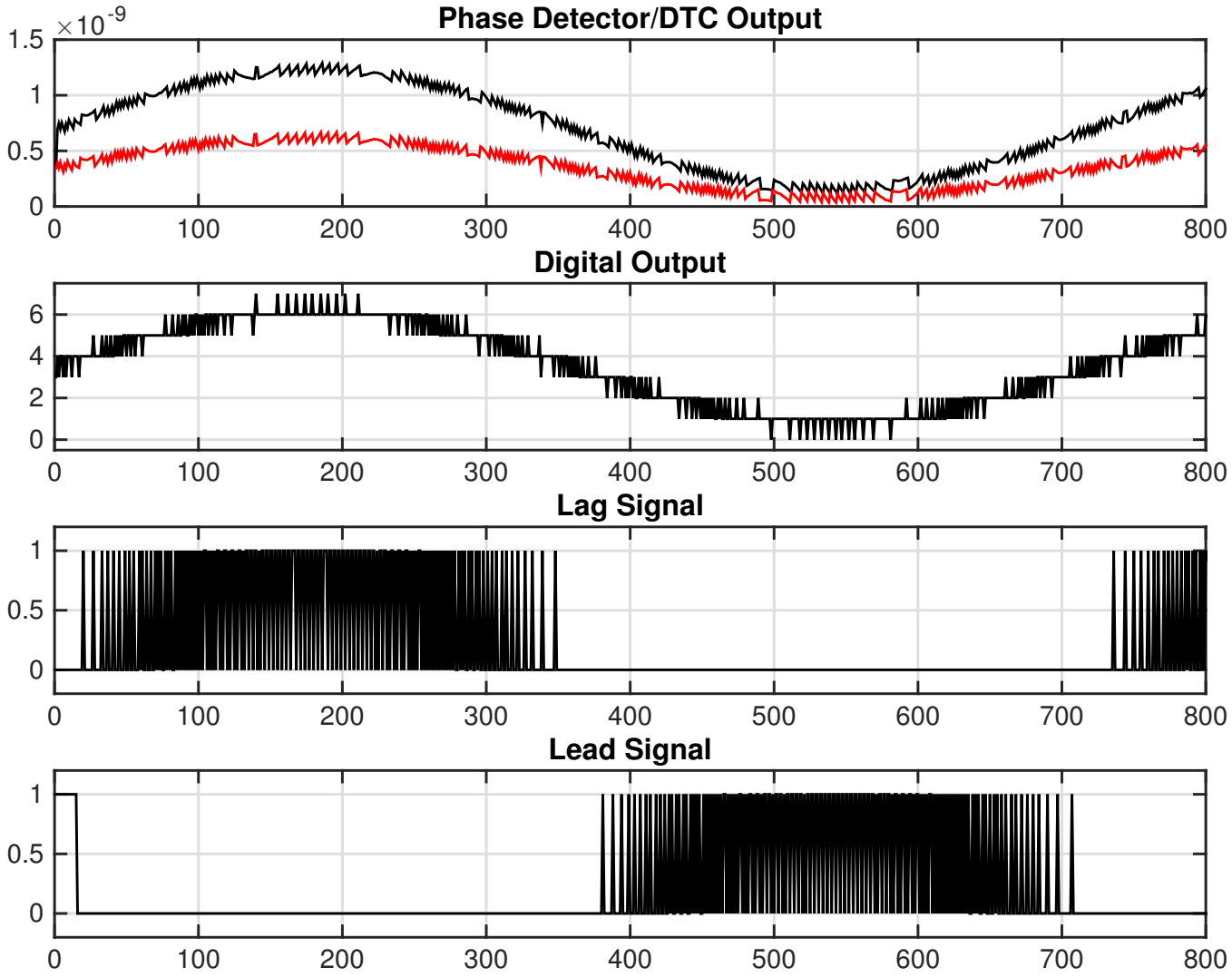


Simulink Modeling - DCU





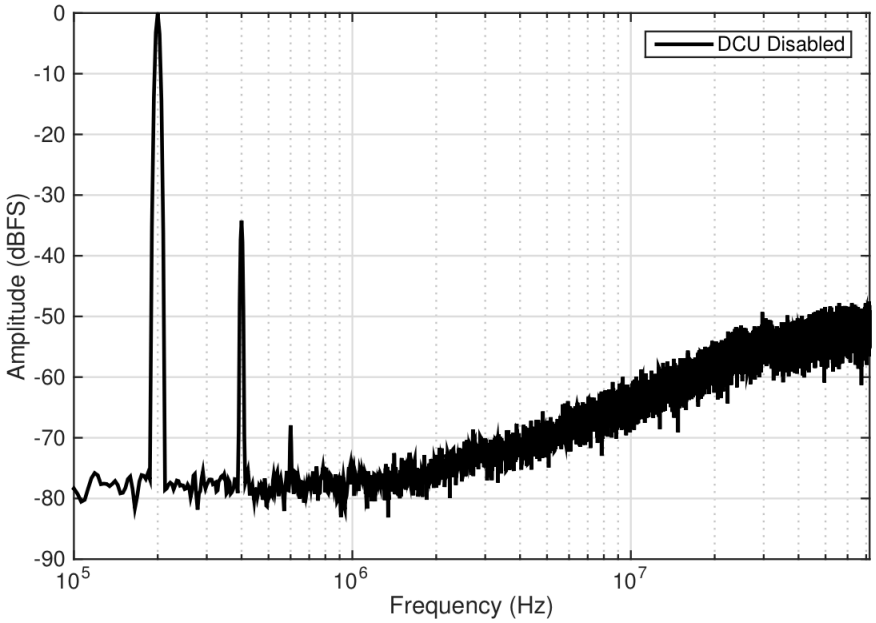
Simulink Modeling



Role of DCU in Reducing Distortion

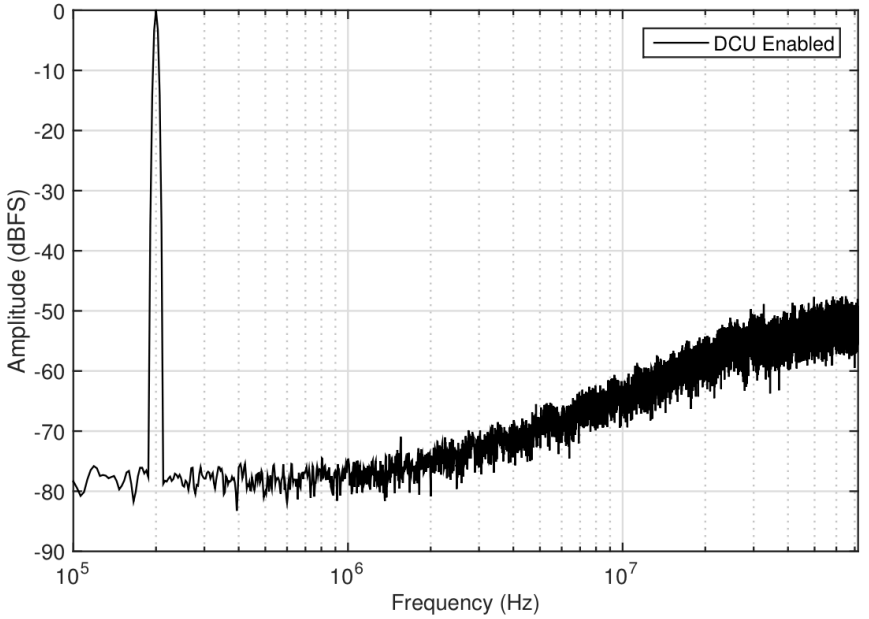
DCU Disabled

Spectrum exhibits major harmonic distortion due to non-uniform sampling



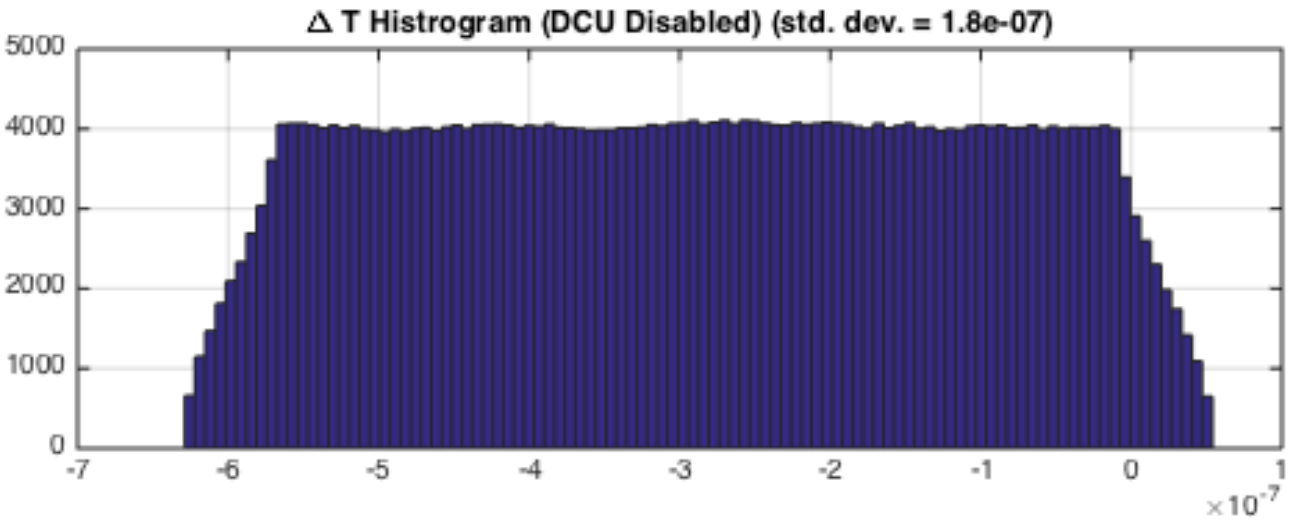
DCU Enabled

Spectrum is virtually distortion free

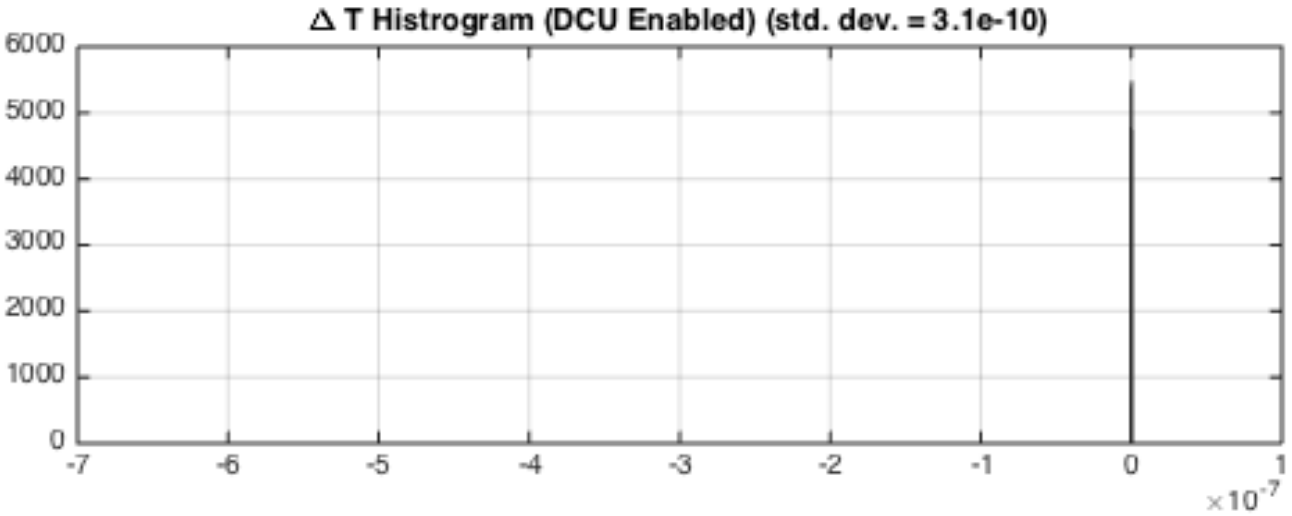


Role of DCU in Reducing Distortion

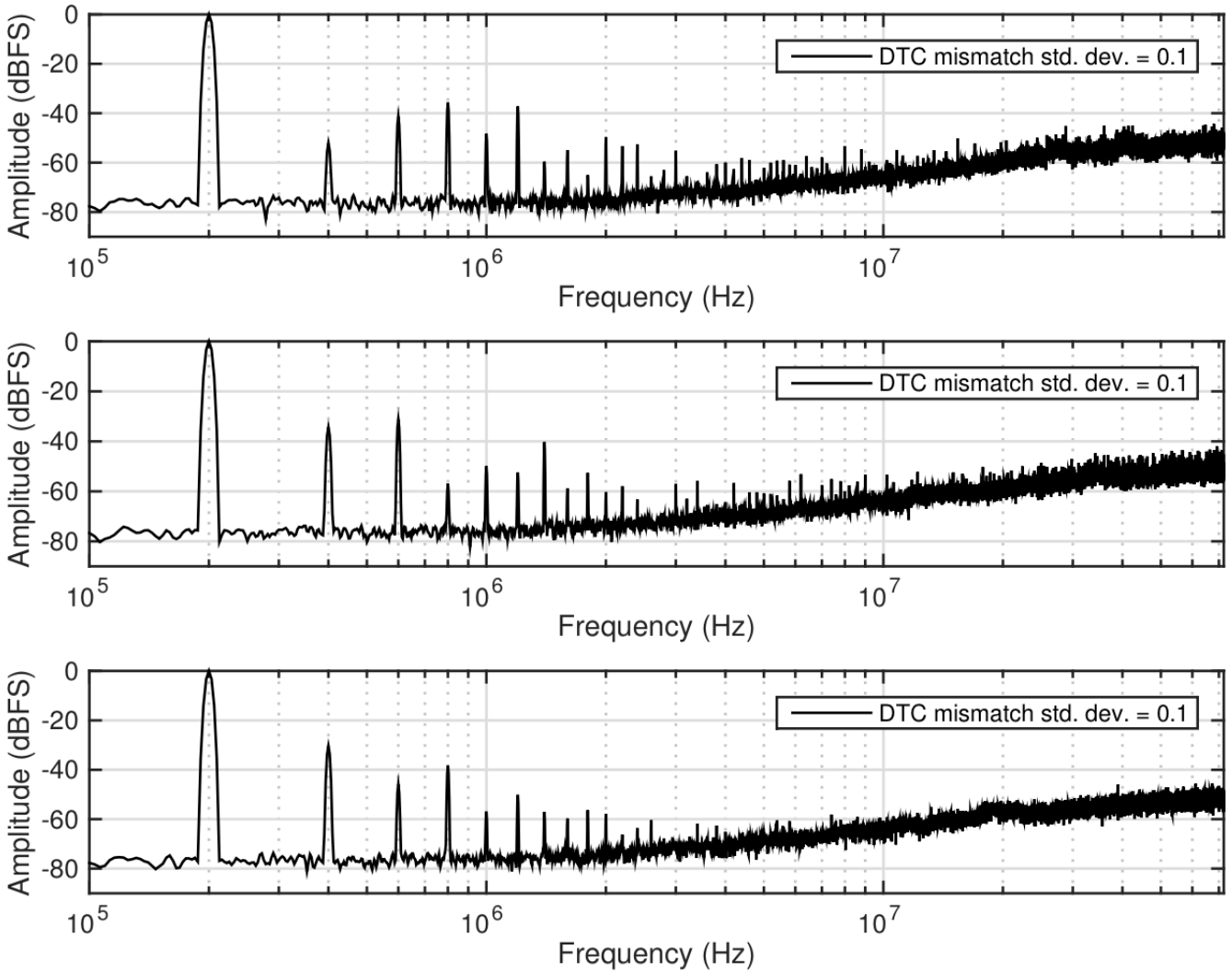
DCU Disabled



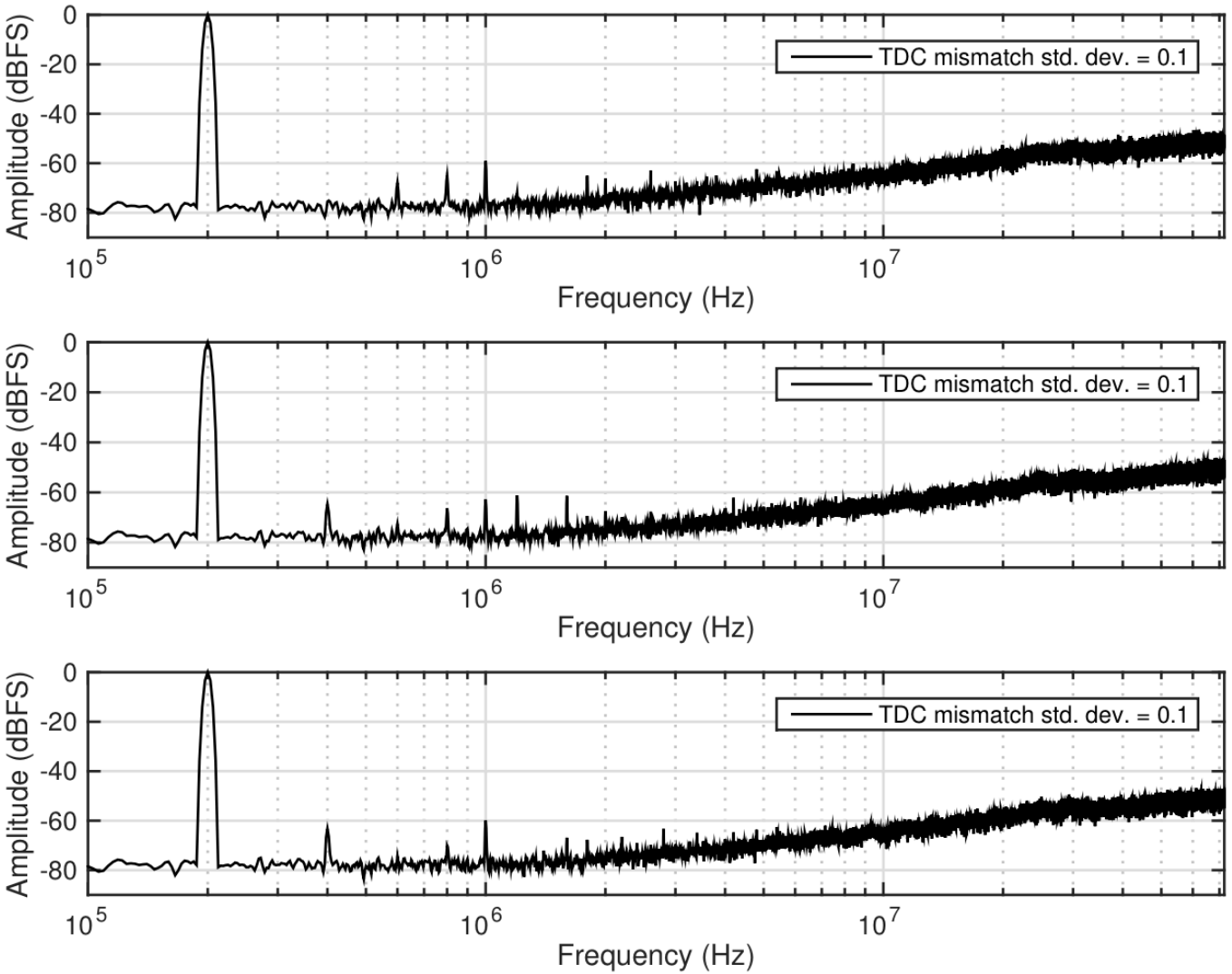
DCU Enabled



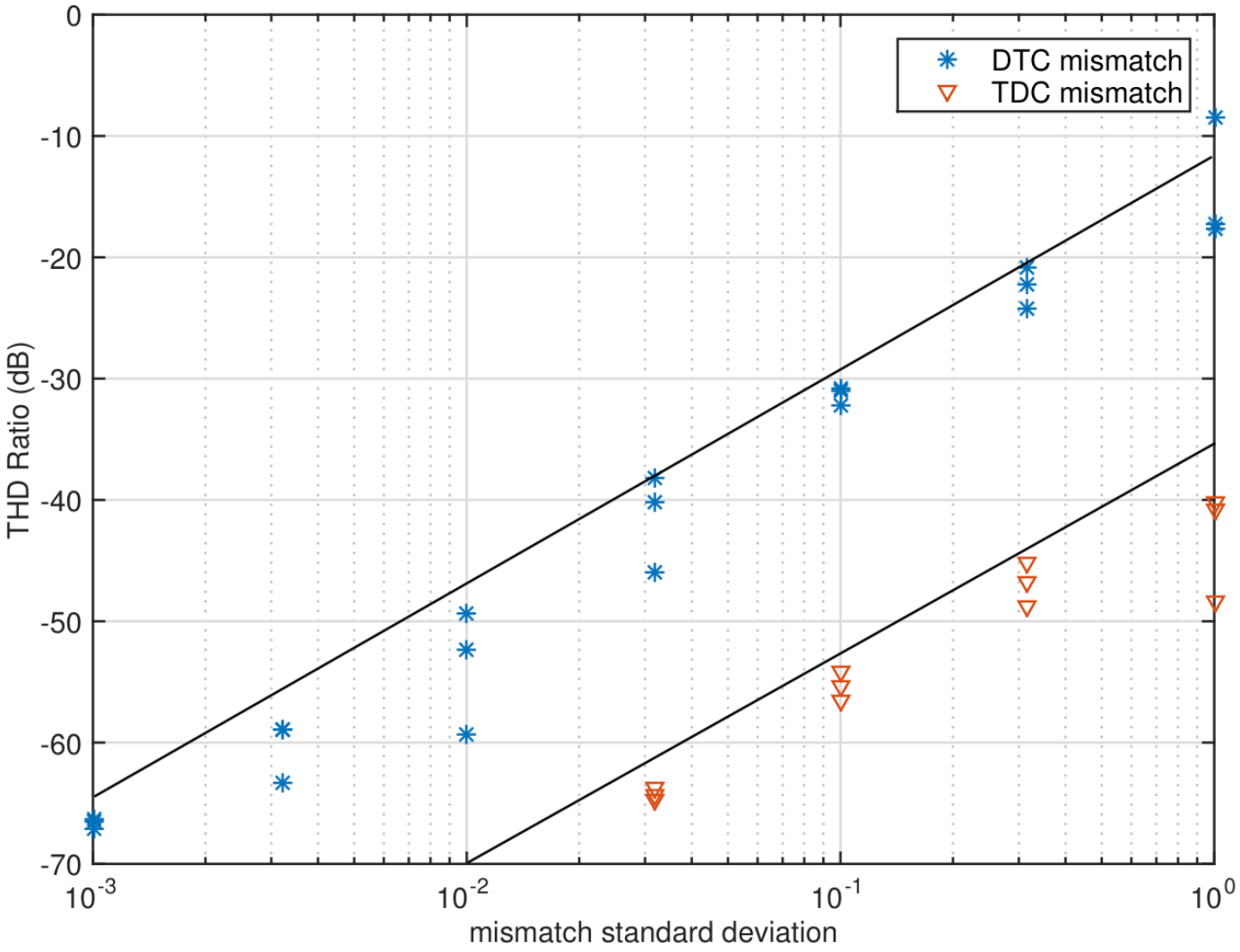
Effect of DTC Element Mismatch

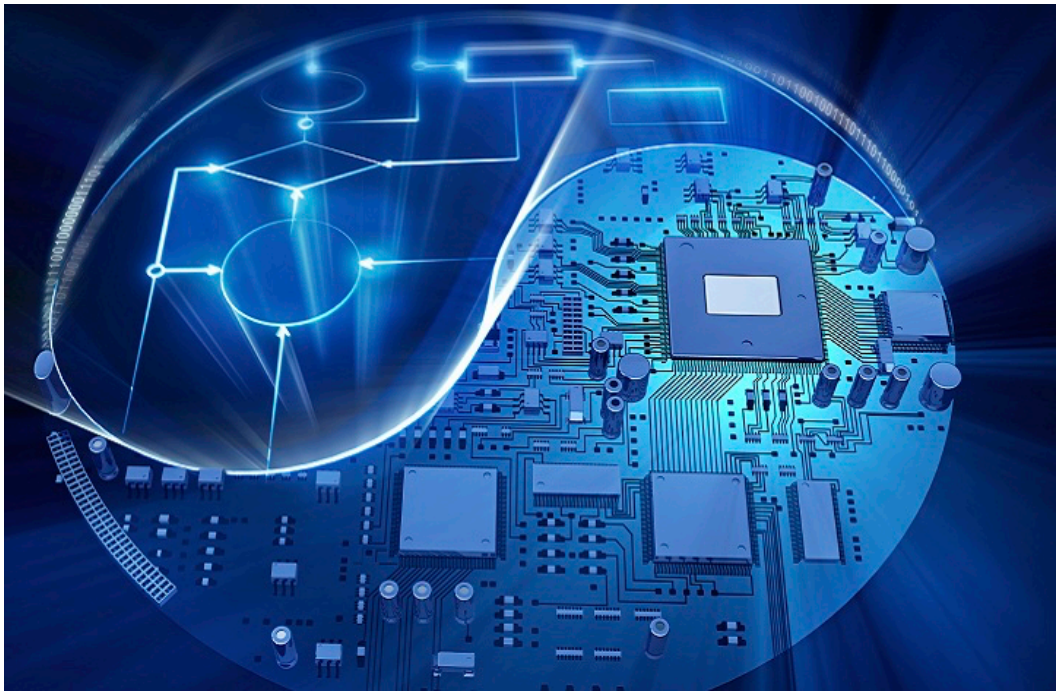


Effect of TDC Element Mismatch



Comparison of DTC/TDC Element Mismatch

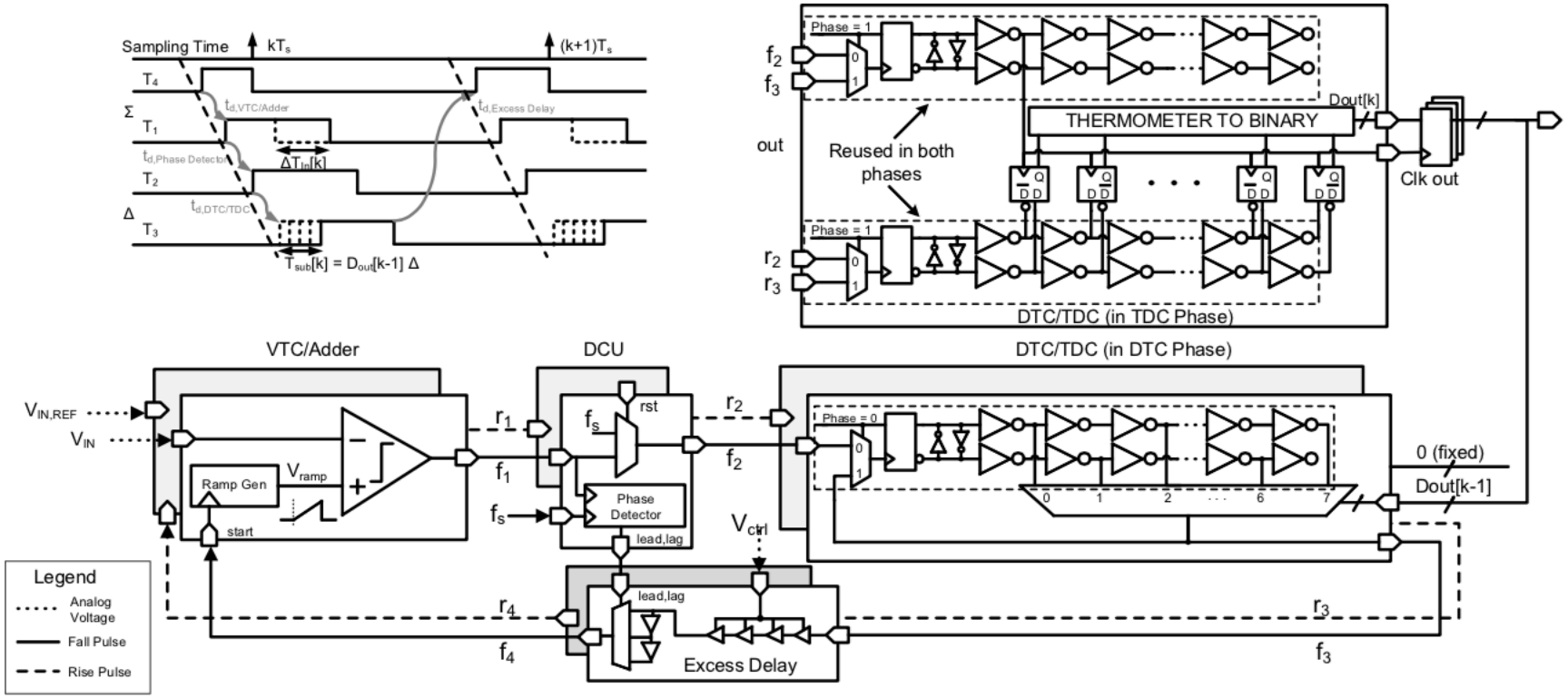




Prototype ADC Chips

Image source: http://www.intel.de/content/www/de/de/cofluent/intel-cofluent-studio.html

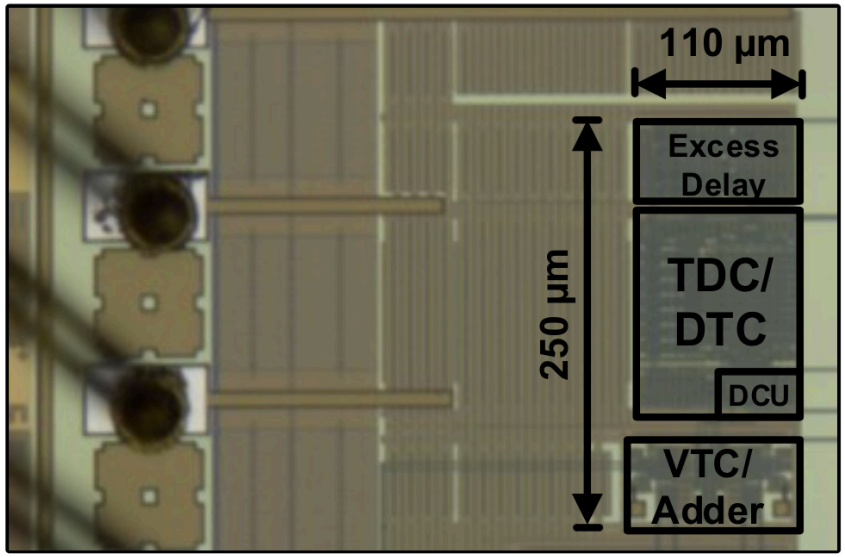
First Generation Chip in TSMC 180nm



TSMC = Taiwan Semiconductor Manufacturing Company

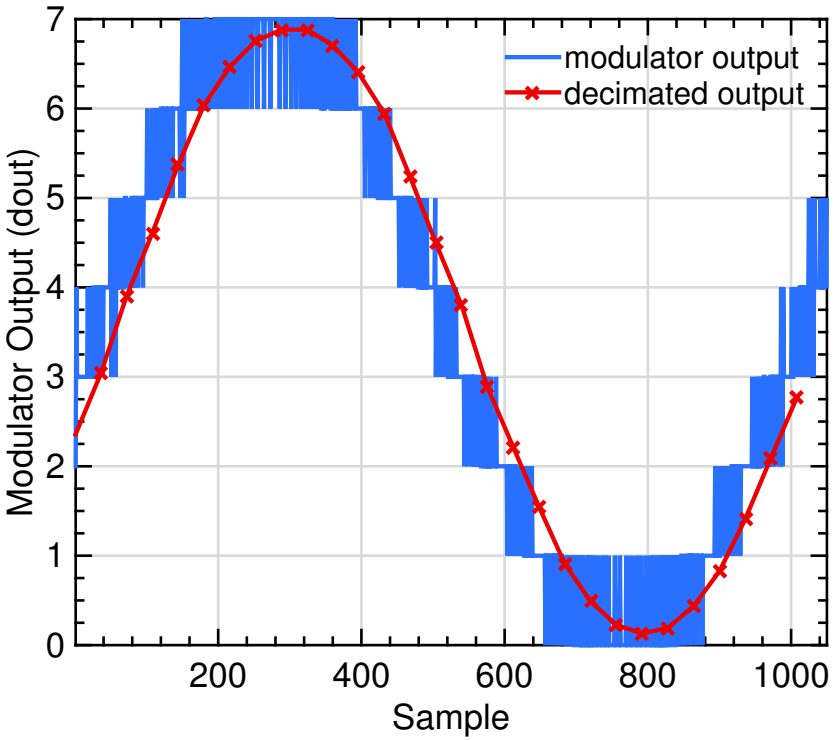
First Generation Chip Details

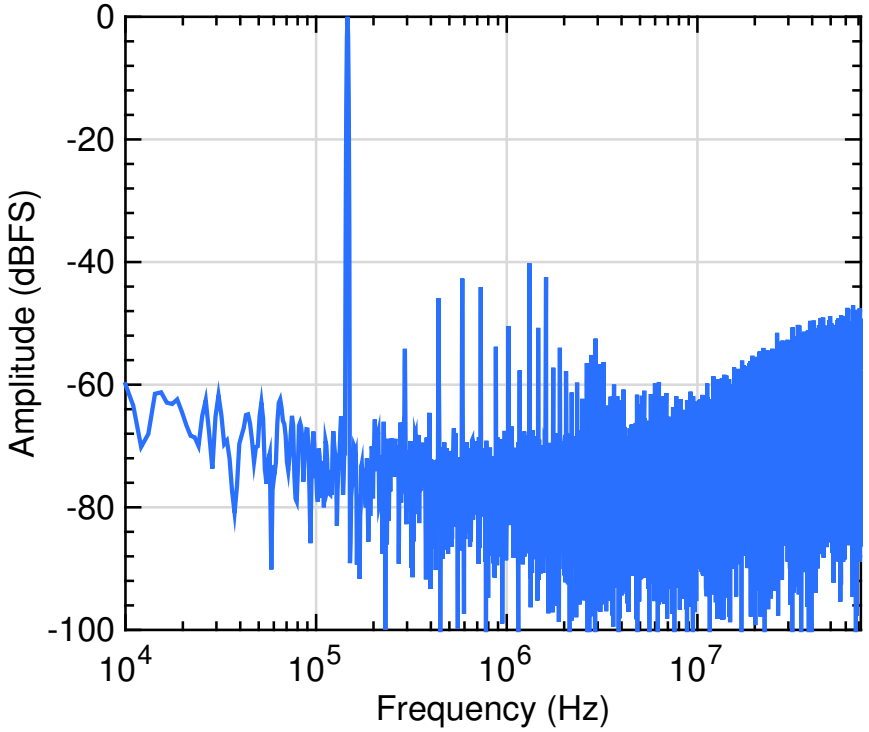
Parameter	Value	Units
Process	TSMC 180nm 6M 1P	-
Supply Voltage (V_{DD})	1.8	V
Oversample Frequency (f_s)	144	MHz
Quantizer (TDC) Number of Bits	3	bits
DAC (DTC) Number of Bits	3	bits
TDC LSB (Δ)	80	ps
$t_{\mathrm{d,VTC/Adder}}$	2.1	ns
$t_{\mathrm{d,PhaseDetector}}$	0.57	ns
$t_{\mathrm{d,DTC}}$	1.24	ns
$t_{\mathrm{d,ExcessDelay}}$ (Average)	2.8	ps
Area	0.0275	mm^2



Quantity	Value	Units
f_s	144	MHz
OSR	36	-
BW	2.0	MHz
f_{in}	146.1	kHz
$V_{in,pk-pk}$	400	mV
SNR	44.6	dB
SNDR	34.6	dB
THD	-35.0	dB
ENoB	5.5	bits
Power	2.7	mW

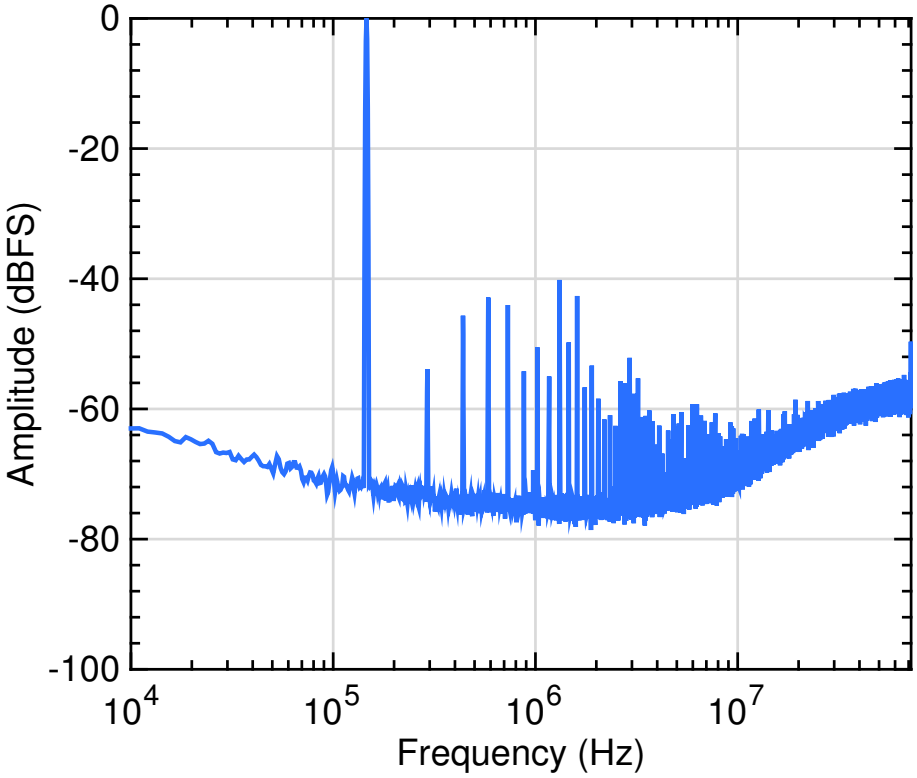
First Generation Chip Waveforms

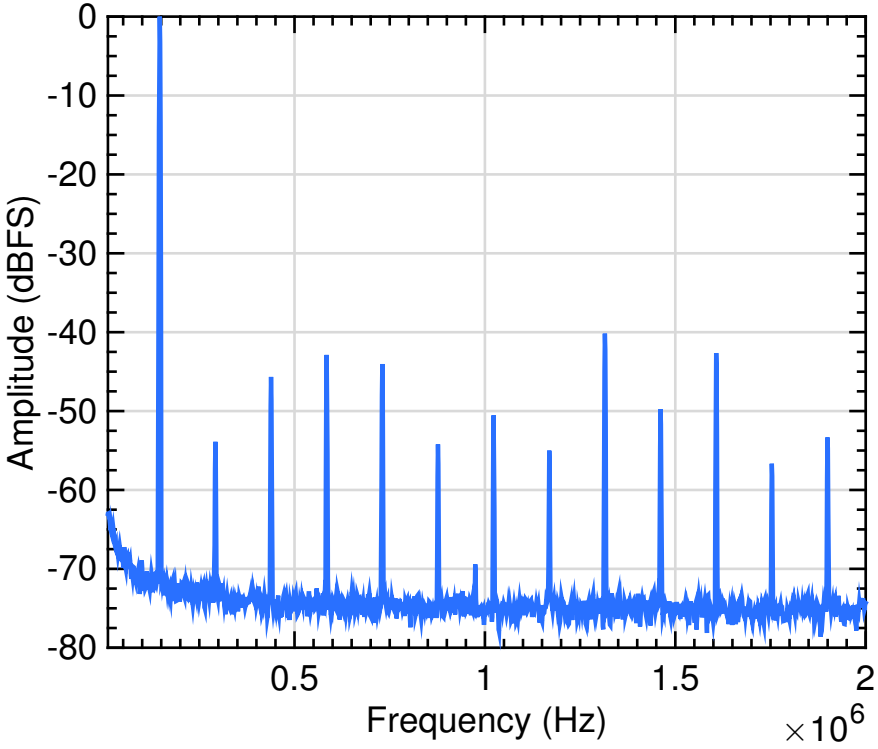




Input is a 146.1 kHz sinusoid

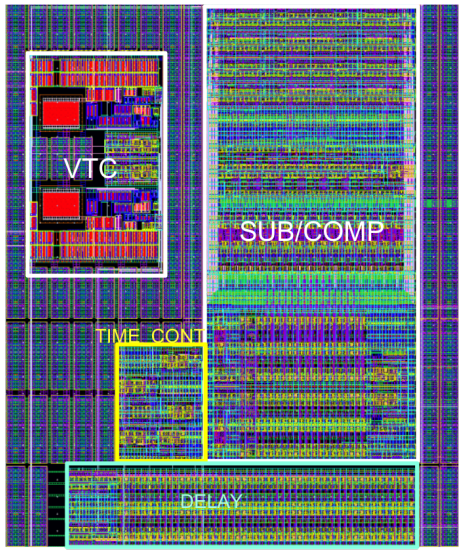
First Generation Chip Waveforms





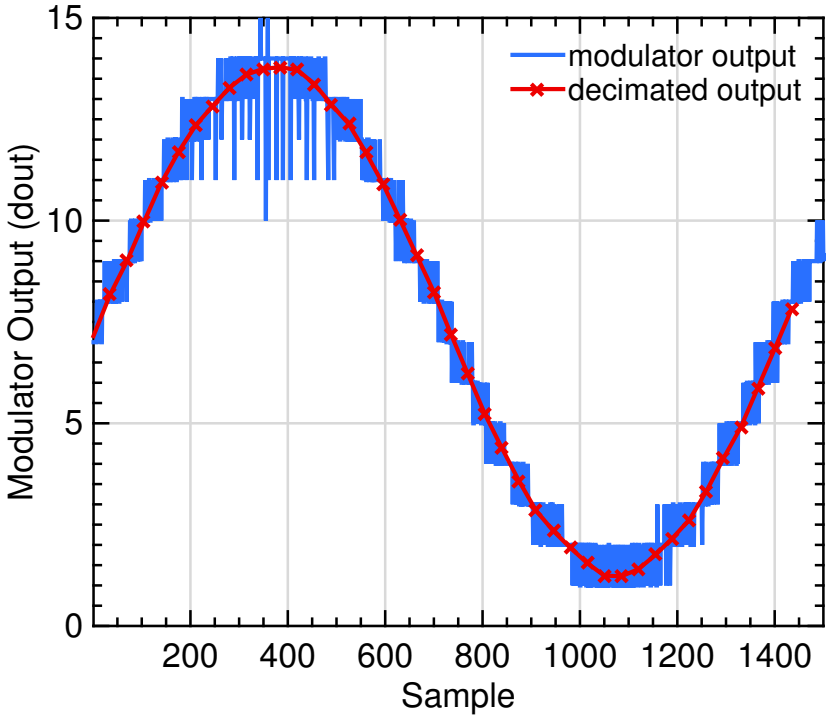
Second Generation Chip in IBM 45nm SOI

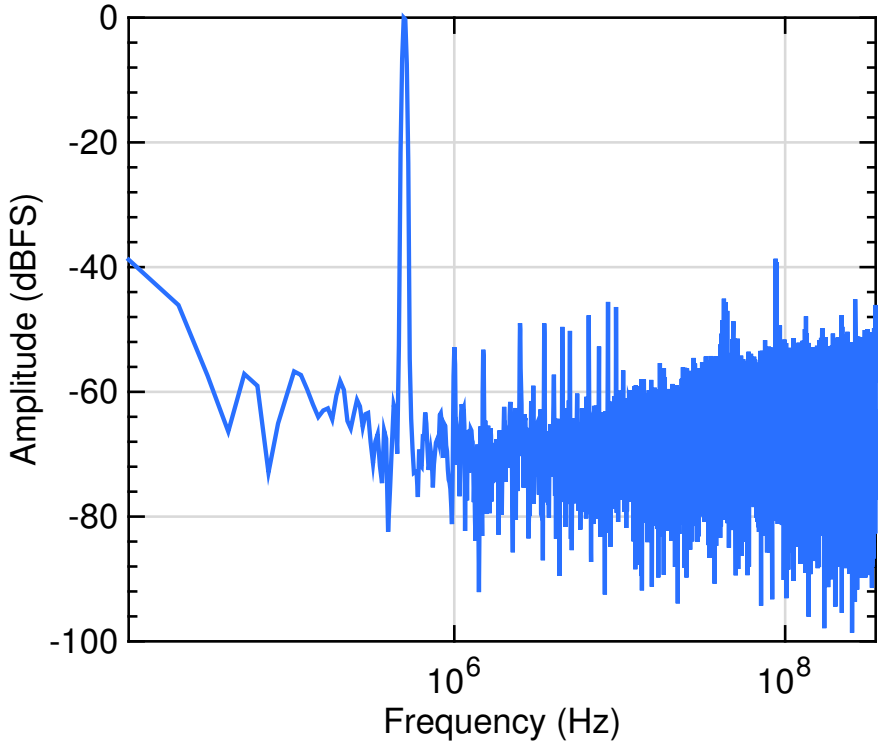
Parameter	Value	Units
Process	IBM 45nm SOI 10M 1P	-
Supply Voltage (V_{DD})	1.8/1.0	V
Oversample Frequency (f_s)	640	MHz
Quantizer (TDC) Number of Bits	4	bits
DAC (DTC) Number of Bits	4	bits
TDC LSB (Δ)	15.8	ps
$t_{\mathrm{d,VTC/Adder}}$	714	ps
$t_{\mathrm{d,PhaseDetector}}$	116	ps
$t_{\mathrm{d,DTC}}$	302	ps
$t_{\mathrm{d,ExcessDelay}}$ (Average)	400	ps
Area	0.0192	mm^2



Quantity	Value	Units
f_s	705	MHz
OSR	36	-
BW	9.8	MHz
f_{in}	500	kHz
$V_{in,pk-pk}$	600	mV
SNR	41.2	dB
SNDR	37.5	dB
ENoB	6	bits
THD	-39.6	dB
Power	8.0	mW

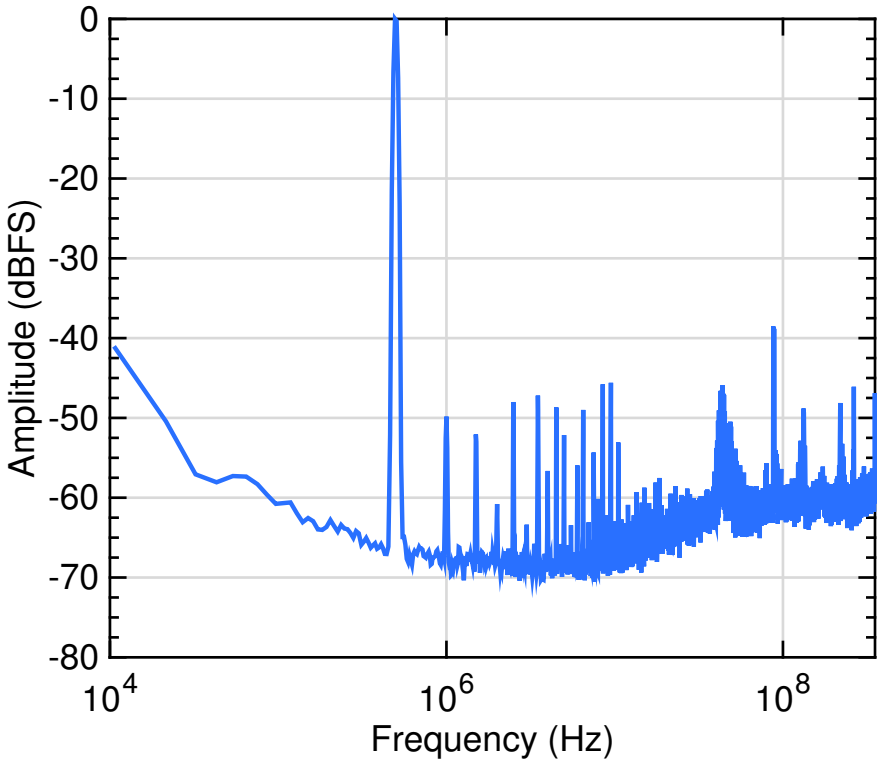
Second Generation Chip in IBM 45nm SOI

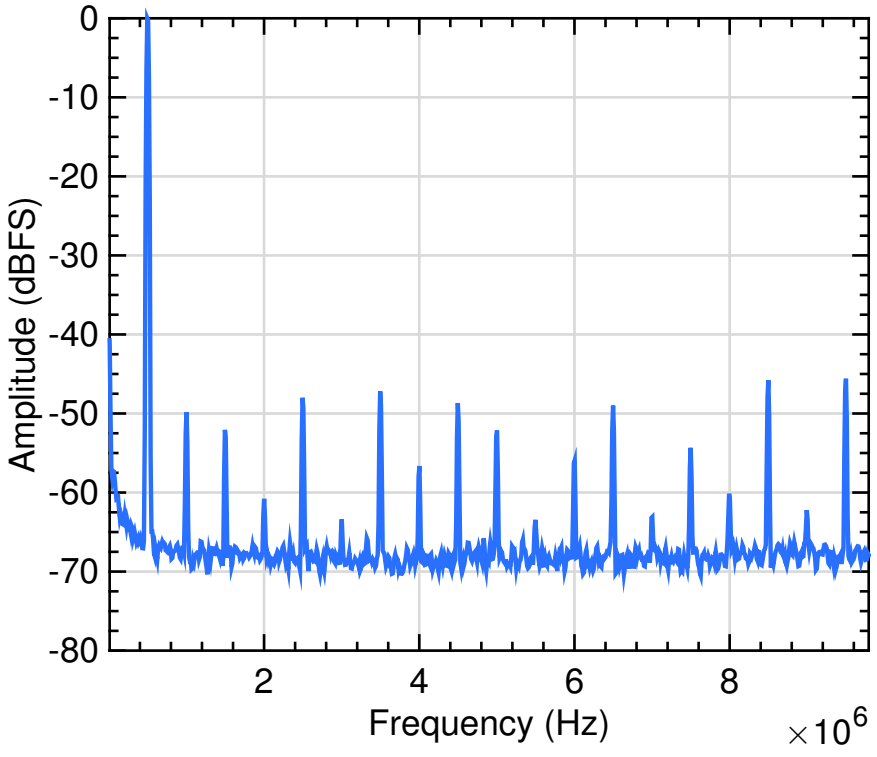




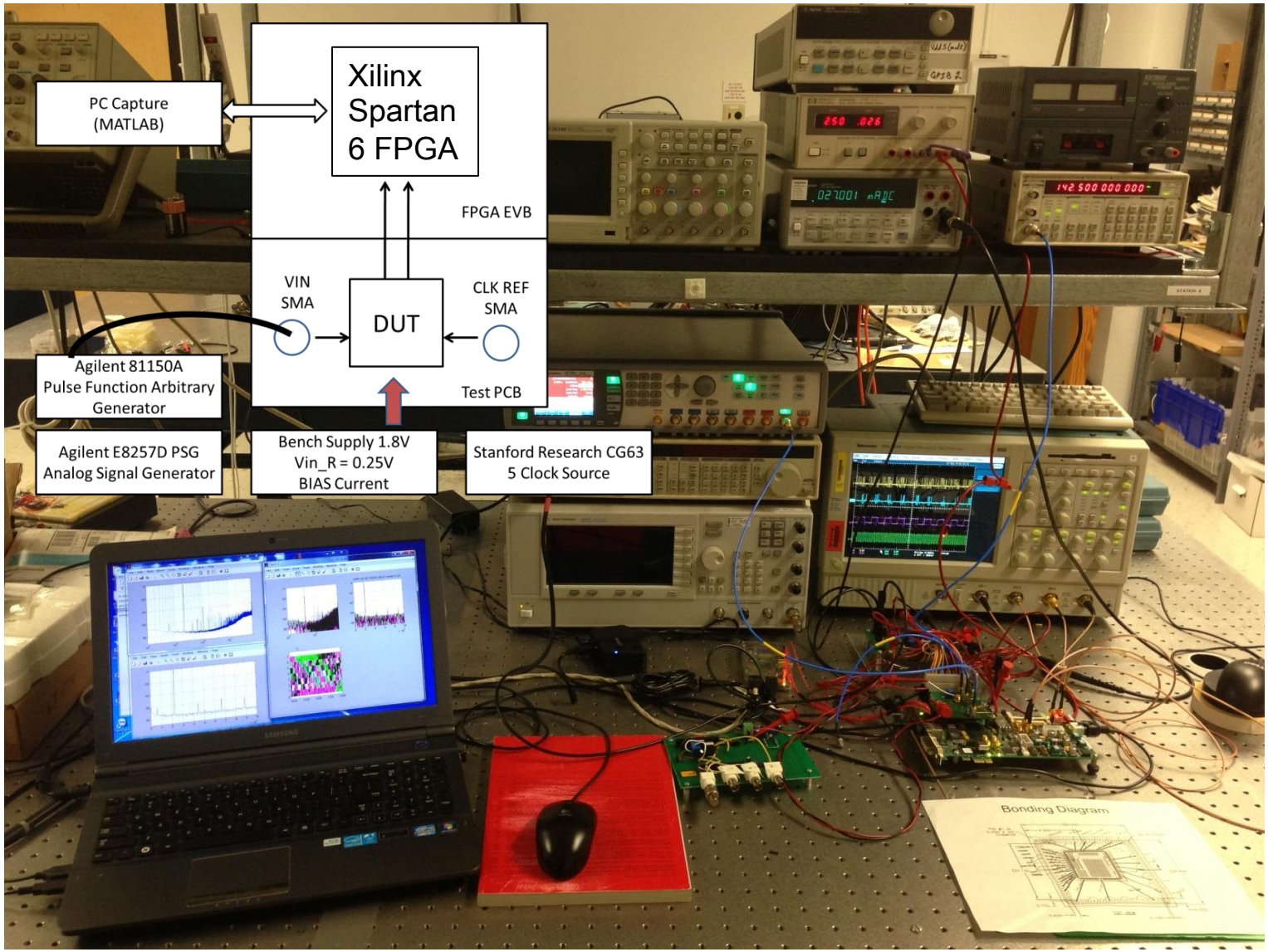
Input is a 500 kHz sinusoid

Second Generation Chip in IBM 45nm SOI





Test Setup


PC Capture
(MATLAB)
Xilinx
Spartan
6 FPGA
FPGA EVB
VIN
SMA
DUT
CLK REF
SMA
Test PCB
Agilent 81150A
Pulse Function Arbitrary
Generator
Agilent E8257D PSG
Analog Signal Generator
Bench Supply 1.8V
Vin_R = 0.25V
BIAS Current
Stanford Research CG63
5 Clock Source
Bonding Diagram

Comparison Table

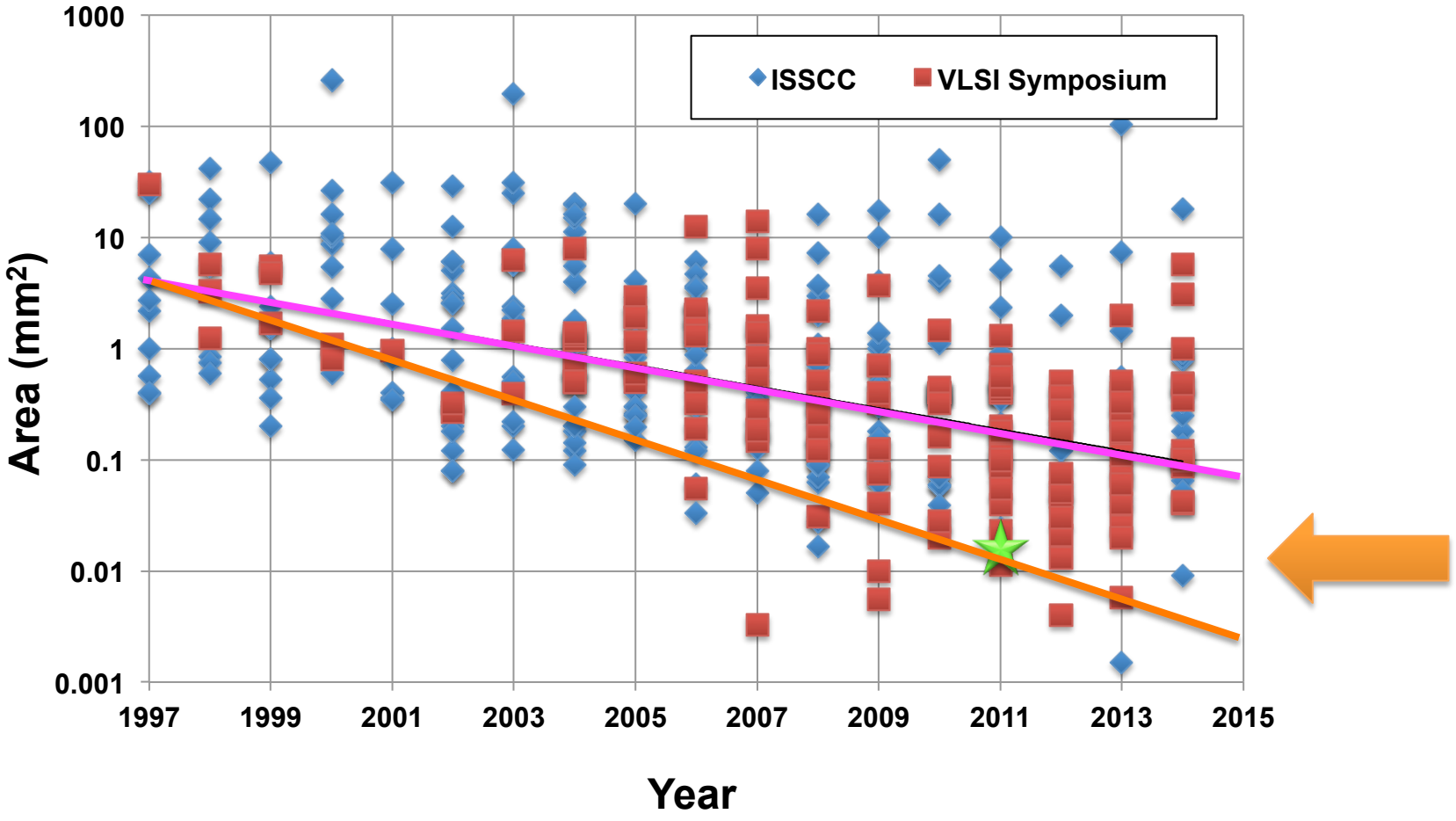
Design Parameters

	Gen1	Gen2	
Parameter	Value	Value	Units
Process	TSMC 180nm 6M 1P	IBM 45nm SOI 10M 1P	-
Supply Voltage (V_{DD})	1.8	1.8/1.0	V
Oversample Frequency (f_s)	144	640	MHz
Quantizer (TDC) Number of Bits	3	4	bits
DAC (DTC) Number of Bits	3	4	bits
TDC LSB (Δ)	80	15.8	ps
$t_{\mathrm{d,VTC/Adder}}$	2.1	714	ps
$t_{\mathrm{d,PhaseDetector}}$	0.57	116	ps
$t_{\mathrm{d,DTC}}$	1.24	302	ps
$t_{\mathrm{d,ExcessDelay}}$ (Average)	2.8	400	ps
Area	0.0275	0.0192	mm^2

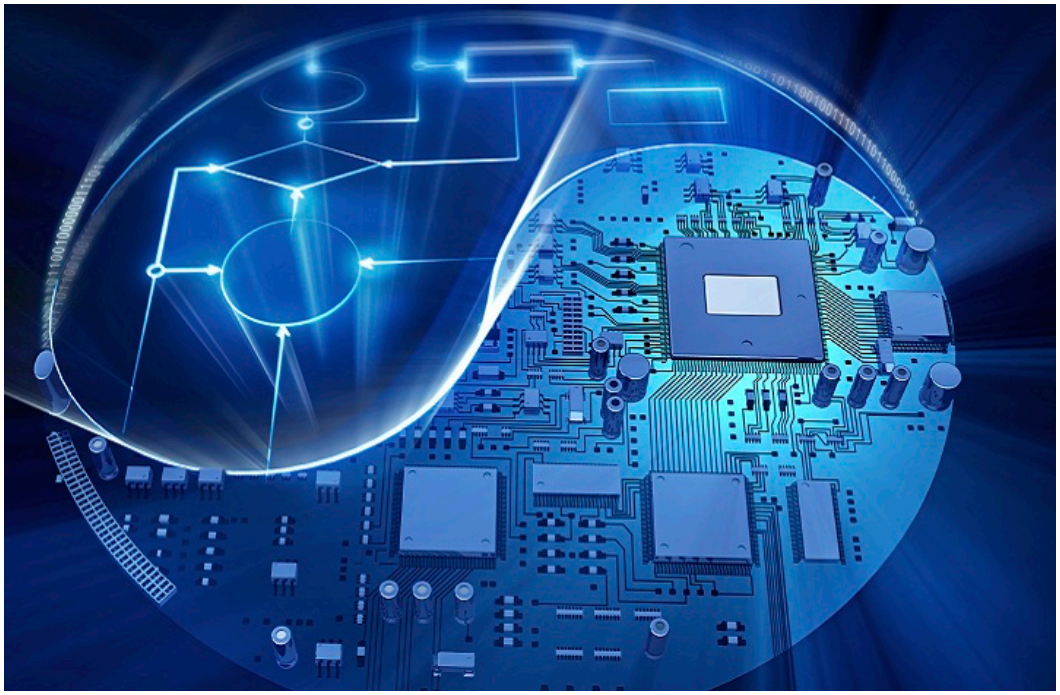
Measured Results

f_s	144	705	MHz
OSR	36	36	-
BW	2.0	9.8	MHz
f_{in}	146.1	500	kHz
$V_{in,pk-pk}$	400	600	mV
SNR	44.6	41.2	dB
SNDR	34.6	37.5	dB
THD	-35.0	6	bits
ENoB	5.5	-39.6	dB
Power	2.7	8.0	mW

Analog-to-Digital Converter Area Comparison



B. Murmann, "ADC Performance Survey 1997-2015," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.



Nonlinearity Calibration

Image source: http://www.intel.de/content/www/de/de/cofluent/intel-cofluent-studio.html

Nonlinearity Due to Element Mismatch

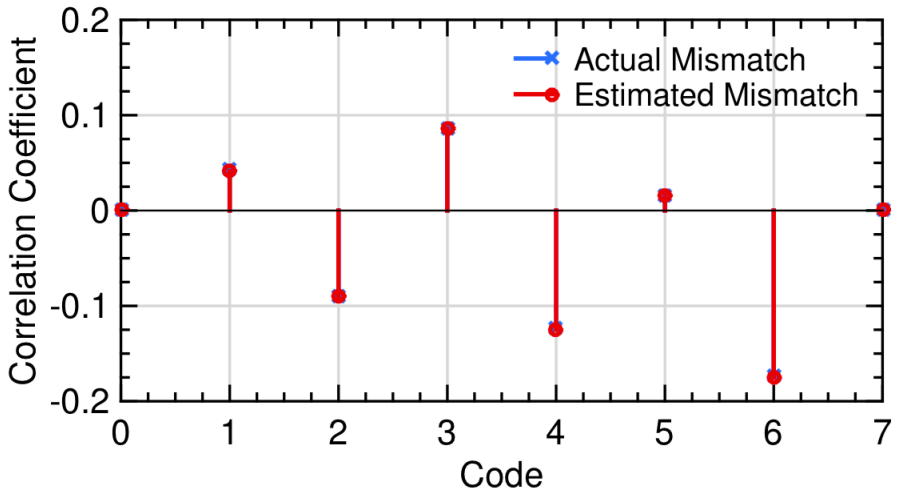
- In the presence of DTC (DAC) element mismatch Multibit DSMs exhibit harmonic distortion.

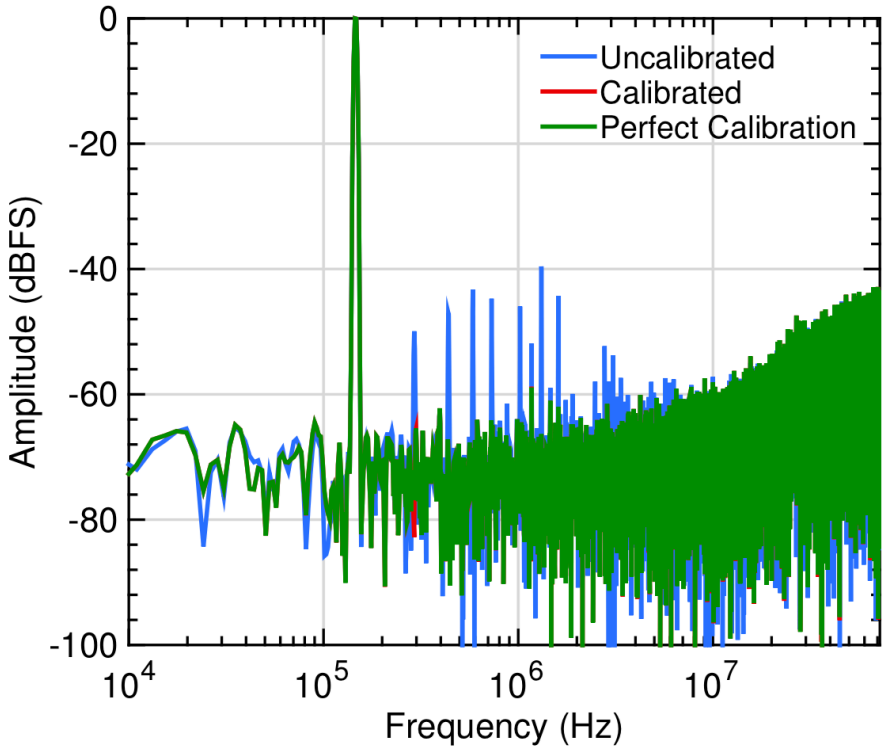
- To lower the distortion, need
  - extremely good matching, and/or
  - dynamic element matching (DEM) schemes.

- Alternatively:
  - Lookup table (LUT) that maps each code out of the modulator to the true value of the DTC can perfectly cancel nonlinearity.

- Problem:
  - How do we estimate the DTC element mismatch?

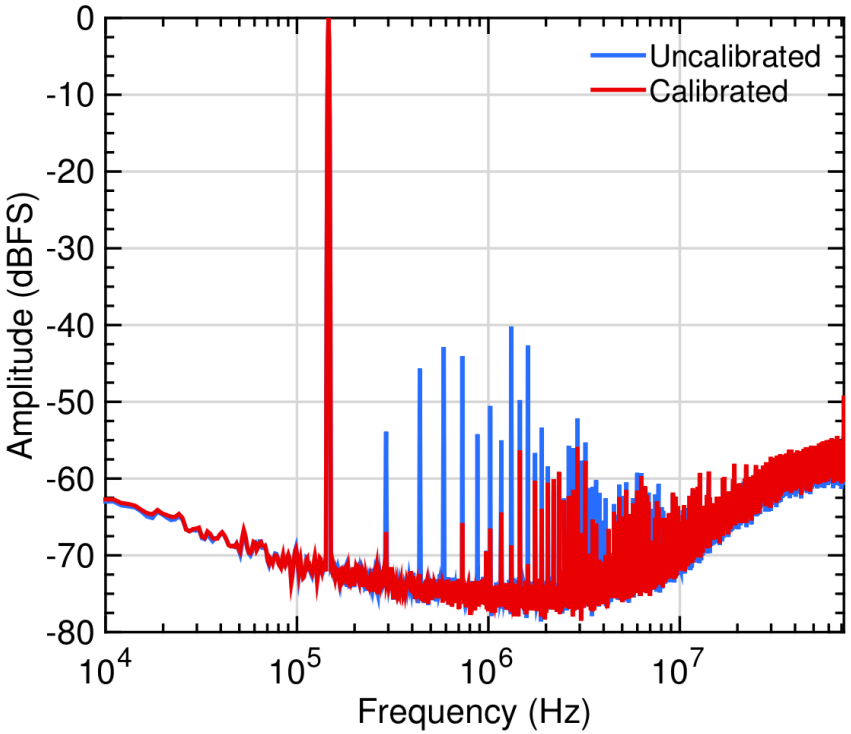
Simulated Estimation/Calibration

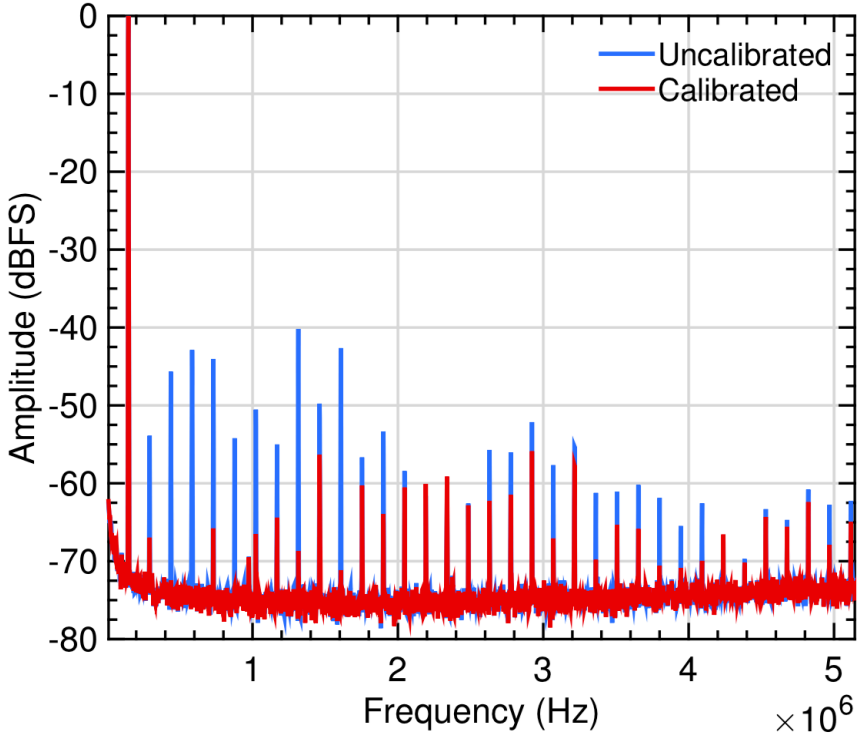




	Uncalibrated	Calibrated	Improvement	Perfect Cal.	Units
SNR	45.5	46.0	0.5	46.0	dB
SNDR	35.1	44.8	9.9	44.8	dB
THD	-35.5	-50.7	15.0	-50.7	dB
ENoB	5.5	7.2	1.7	7.2	bit

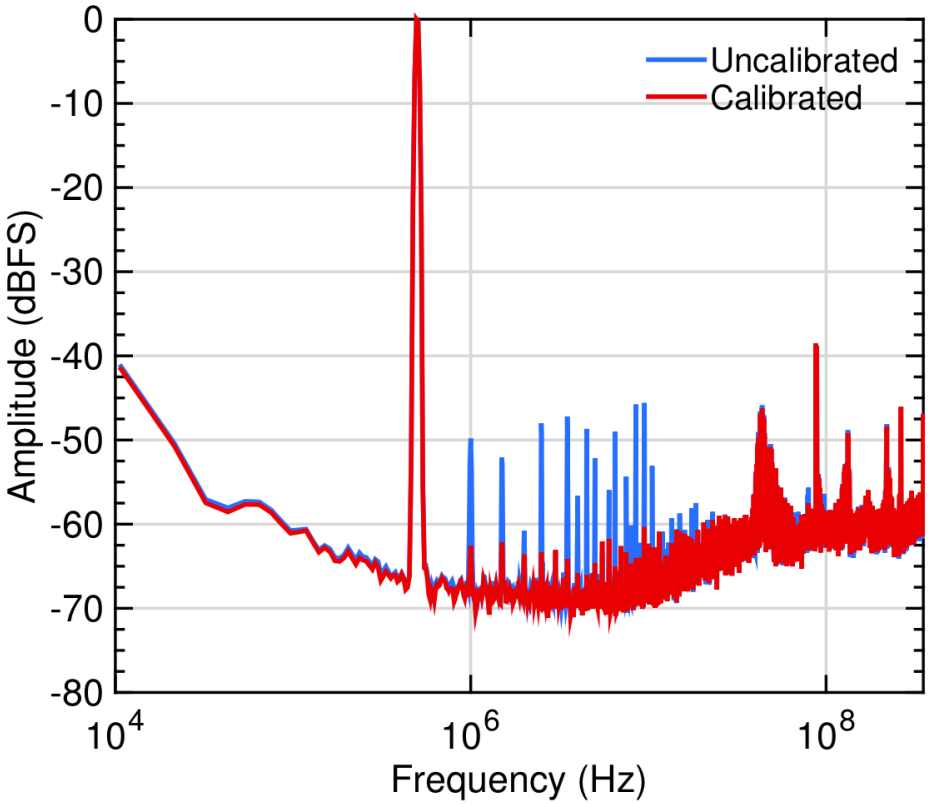
First Generation Chip Calibration

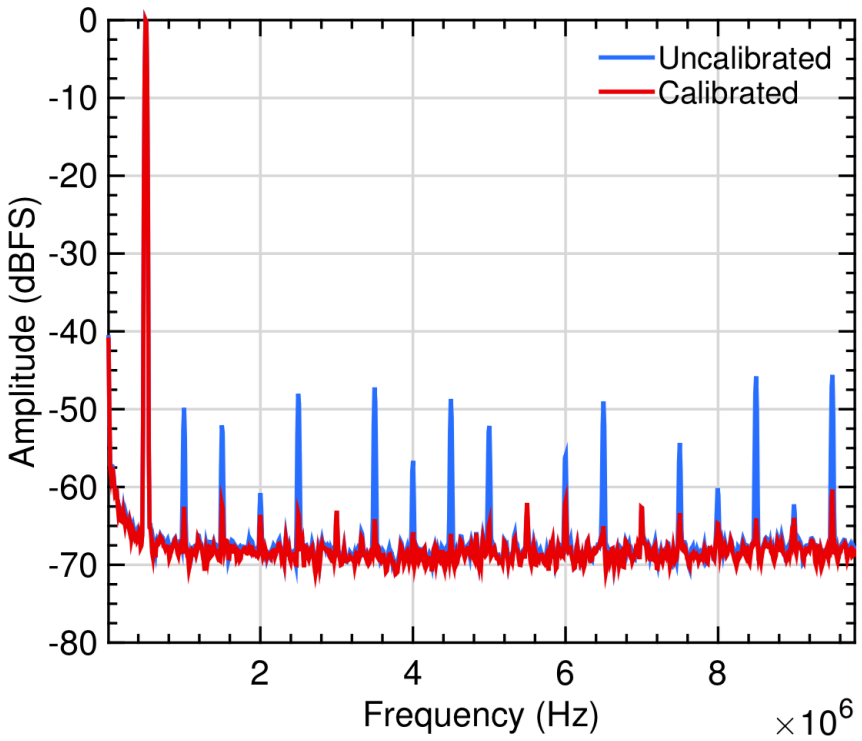




	Uncalibrated	Calibrated	Improvement	Units
SNR	44.6	44.8	0.2	dB
SNDR	34.6	44.0	9.4	dB
THD	-35.0	-51.0	16.0	dB
ENoB	5.5	7.0	1.5	bit

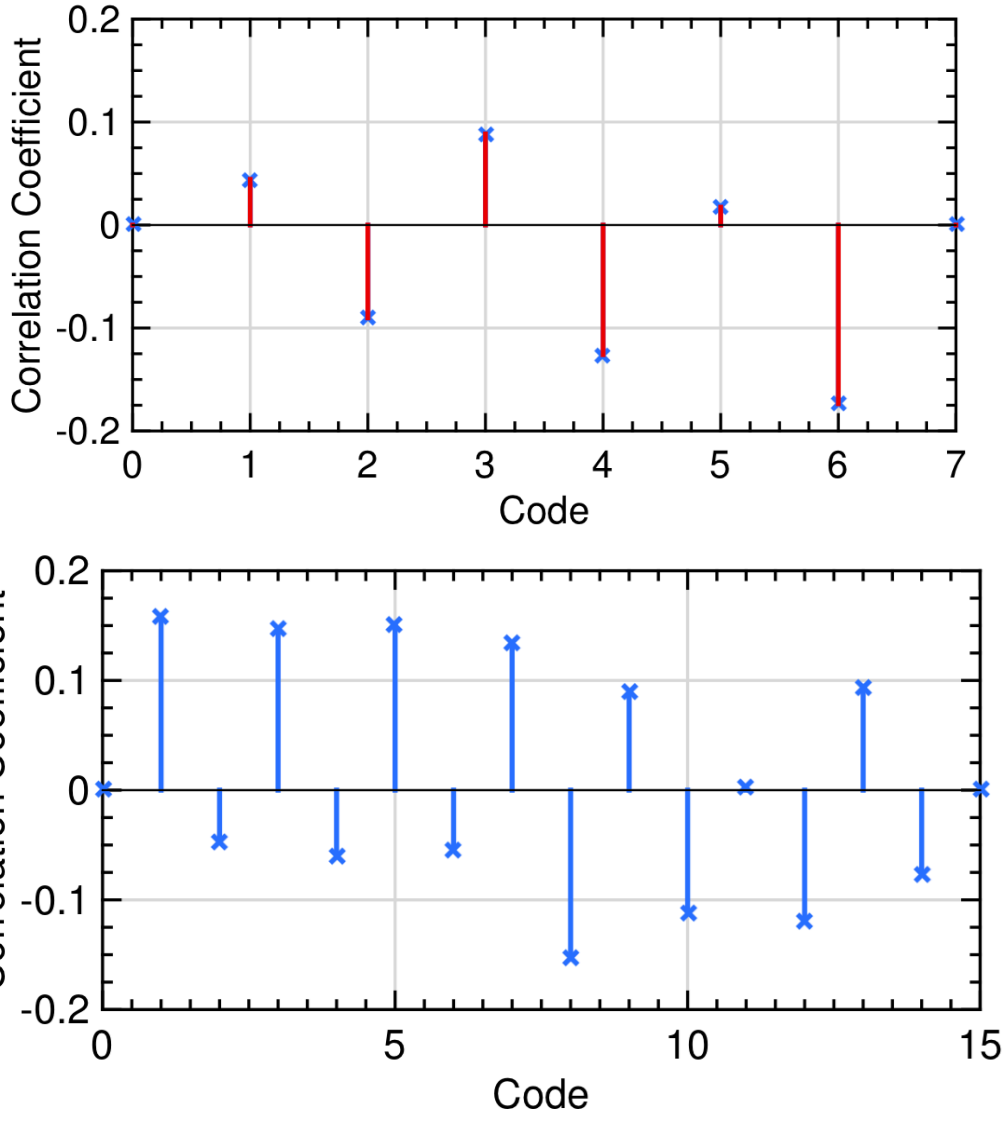
Second Generation Chip Calibration





	Uncalibrated	Calibrated	Improvement	Units
SNR	44.6	44.8	0.2	dB
SNDR	34.6	44.0	9.4	dB
THD	-35.0	-51.0	16.0	dB
EnoB	5.5	7.0	1.5	bit

Mismatch Coefficients



Summary of Contributions

- **Contribution 1:**
  Architect and model novel time-based delta sigma ADC
  - Replace voltage-domain with time-domain processing to enable scaling
  - Calibrate loop delay to reduce non-uniform sampling effects
  - Reuse elements of TDC/DTC to save area

- **Contribution 2:**
  Fabricate and test two prototype two ADC chips
  - TSMC 180nm CMOS
  - IBM 45nm SOI

- **Contribution 3:**
  Analyze and mitigate major nonlinearity
  - Estimate element mismatch coefficients
  - Perform digital post-correction

Future Work

- Reduction in DTC unit delay element mismatch by
  - utilizing (non-inverting) buffers rather than inverters, or
  - using the same structure of DTC/TDC but with feedback that truncates the LSB, or
  - using extra inverter stages and implementing a dynamic element matching scheme.

- Circuit-level improvements
  - Improve thermal/flicker noise in front-end circuits, mainly comparator
  - Reduce power consumption of front-end by removing replica of ramp generator and comparator in the VTC/Adder and replacing it with a calibrated delay cell.

Summary of Relevant Work by Presenter

- Y. Mortazavi, S. M. Mortazavi Zanjani, A. Brennan, D. Allen, M. Ranjbar, A 12.6 μW 70+ dB DR 2nd Order CT ΔΣ Audio ADC in 55nm CMOS, *2015 IEEE Custom Integrated Circuits Conference*, Sep. 28-30, 2015, San Jose, CA USA, to be submitted.
- W. Jung, Y. Mortazavi, B. L. Evans, and A. Hassibi, "An all-digital PWM-based ΔΣ ADC with an inherently matched multi-bit quantizer/DAC," *2014 IEEE Custom Integrated Circuits Conference*, Sep. 15-17, 2014, San Jose, CA USA.
- Y. Mortazavi, W. Jung, B. L. Evans, and A. Hassibi, "A mostly-digital PWM-based ΔΣ ADC with an inherently matched multi-bit quantizer/DAC," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, under review.
- M. Nassar, J. Lin, Y. Mortazavi, A. Dabak, I. H. Kim and B. L. Evans, ``Local Utility Powerline Communications in the 3-500 kHz Band: Channel Impairments, Noise, and Standards", *IEEE Signal Processing Magazine, Special Issue on Signal Processing Techniques for the Smart Grid*, vol. 29, no. 5, pp. 116-127, Sep. 2012.
- M. Nassar, K. Gulati, Y. Mortazavi, and B. L. Evans, ``Statistical Modeling of Asynchronous Impulsive Noise in Powerline Communication Networks", *Proc. IEEE Global Communications Conf.*, Dec. 5-9, 2011, Houston, TX USA.
- A. G. Olson, A. Chopra, Y. Mortazavi, I. C. Wong, and B. L. Evans, ``Real-Time MIMO Discrete Multitone Transceiver Testbed", *Proc. Asilomar Conf. on Signals, Systems, and Computers*, Nov. 4-7, 2007, Pacific Grove, CA USA. [Won Best Student Paper Award for the Architecture and Implementation Track].

References

[Murmann2010] – B. Murmann, "Trends in low-power, digitally assisted A/D conversion," *IEICE Trans. on Electronics,* vol. E93-C, no. 6, pp. 718–729, 2010.

[Rao2011] – S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar, and P. Hanumolu, "A 71dB SFDR open loop VCO-based ADC using 2-level PWM modulation," *2011 Symp. VLSI Circuits*, pp. 270–271, June 2011.

[Taylor2013] – G. Taylor and I. Galton, "A reconfigurable mostly-digital delta-sigma ADC with a worst-case FOM of 160dB," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 983 – 995, Feb. 2013.

[Dhanasekaran2009] – V. Dhanasekaran, M. Gambhir, M. Elsayed, E. Sanchez-Sinencio, J. Silva-Martinez, C. Mishra, L. Chen, and E. Pankratz, "A 20MHz BW 68dB DR CT ΔΣ ADC based on a multi-bit time-domain quantizer and feedback element," *IEEE Solid-State Circuits Conf.*, Feb 2009, pp. 174–175,175a

[Taillefer2009] – C. S. Taillefer and G. W. Roberts, "Delta–sigma A/D conversion via time-mode signal processing," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 9, pp. 1908–1920, 2009.

[Daniels2010] – J. Daniels, W. Dehaene, M. S. J. Steyaert, and A. Wiesbauer, "A/D conversion using asynchronous delta-sigma modulation and time-to-digital conversion," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. PP, no. 99, pp. 1 –1, 2010.

Questions?

Element Mismatch Estimation

1. Calculate $X[k]$, the windowed-FFT of the modulator output ($x[n]$).
2. Repeat the following for $u \in \{1, 2, \ldots, 2^{NoB} - 2\}$
   (a) Calculate $I_u[k]$, the windowed-FFT of the event that the modulator code equals u, i.e., $\mathbf{1}(x[n] = u)$.
   (b) Correlate a predetermined set of bins $(k_1, \ldots, k_j)$ from $X[k]$ with the same bins from $I_u[k]$. Call the result $\epsilon[u]$.
   (c) Where $x(n) = u$, replace $x(n)$ with $T(u) = u + \epsilon[u]$.

Mathematically,

$$\epsilon[u] = \frac{\sum_{k=k_1}^{k_j} \{\Re(X[k]I_u[k]) + \Im(X[k]I_u[k])\}}{\sum_{k=k_1}^{k_j} \{\Re(I_u[k]I_u[k]) + \Im(I_u[k]I_u[k])\}} \tag{7.1}$$

where $\Re(\cdot)$ and $\Im(\cdot)$ denote the real and imaginary parts of the argument, respectively.