High-Speed Digital Subscriber Line Generation 2
(HDSL2) Modem

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Outline

• Need for high bandwidth

• Digital Subscriber Line (DSL) standards

• Top-level block diagram of HDSL2 modem

• Estimate of implementation cost of a soft HDSL2 modem

• Summary
Need for High Bandwidth

- Small Office / Home Office
  - Small business run out of home: 20 million small businesses in the US
- Internet Access
  - Internet users: 28 million, growing by 2x every year
- Internet Service
  - Web sites: 230,000, growing by 2x every 6 months
- Telecommuting
  - Work at home: 5-10 million telecommuters in the US
- Video-conferencing

Communication bandwidth between the computers has not kept up with advances in computing power, system memory size, and storage capacity.

March 9, 1998: Motorola sends samples of CopperGold ADSL solution to customers
Nov. 19, 1997: Texas Instruments purchases Amati for its ADSL and VDSL technology ($395 million)
# Existing and Proposed DSL Standards

<table>
<thead>
<tr>
<th>Standard</th>
<th>Meaning</th>
<th>Data Rate</th>
<th>Mode</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>V.34</td>
<td>Voice Band Modem</td>
<td>33.6 Kbps</td>
<td>Symmetric</td>
<td>Internet Access</td>
</tr>
<tr>
<td>V.PCM</td>
<td>Voice Band Modem</td>
<td>56 Kbps</td>
<td>Down</td>
<td>Internet Access</td>
</tr>
<tr>
<td></td>
<td></td>
<td>33.6 Kbps</td>
<td>Up</td>
<td></td>
</tr>
<tr>
<td>ISDN</td>
<td>Integrated Services Digital Network</td>
<td>144 Kbps</td>
<td>Symmetric</td>
<td>Internet Access, Pair Gain (2 channels)</td>
</tr>
<tr>
<td>T1</td>
<td>T - Carrier One (requires two pairs)</td>
<td>1.544 Mbps</td>
<td>Symmetric</td>
<td>Enterprise, Expansion, Internet Service</td>
</tr>
<tr>
<td>HDSL</td>
<td>High Speed Digital Subscriber Line (requires two pairs)</td>
<td>1.544 Mbps</td>
<td>Symmetric</td>
<td>Pair Gain (12 channels) Internet Access, T1/E1 replacement</td>
</tr>
<tr>
<td>HDSL2</td>
<td>Single Line HDSL</td>
<td>1.544 Mbps</td>
<td>Symmetric</td>
<td>Pair Gain (24 channels)</td>
</tr>
<tr>
<td>ADSL</td>
<td>Asymmetric Digital Subscriber Line</td>
<td>1.5 - 9 Mbps</td>
<td>Down</td>
<td>Internet Access, Digital Video</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16-640 Kbps</td>
<td>Up</td>
<td></td>
</tr>
<tr>
<td>VDSL</td>
<td>Very High Speed DSL</td>
<td>13 - 52 Mbps</td>
<td>Down</td>
<td>Internet Access, Digital Video</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5-2.3 Mbps</td>
<td>Up</td>
<td></td>
</tr>
</tbody>
</table>

(Courtesy of Cicada Semiconductor, Austin, TX)
Top-level Block Diagram of HDSL2 Modem

- **HDSL2 Transmitter**
  - 1.544 Mbps
  - 517 1/3 KHz

- **Transmitter Shaping Filter**

- **Adaptive Echo Canceler**

- **Hybrid**
  - Loop
  - Line Side

- **HDSL2 Receiver**
  - 1.544 Mbps

- **Receiver Front End**

- **Front End**
Block Diagram of HDSL2 Transmitter

HDSL2 Transmitter (as approved by T1E1.4 subcommittee)

December 9, 1997
Block Diagram of HDSL2 Receiver

Symbol to Bit Mapping

Tomlinson Modulo Operator

Trellis Decoder

Adaptive Linear Equalizer

1.552 Mbps

517 1/3 KHz

517 1/3 KHz

517 1/3 KHz

517 1/3 KHz

1.552 Mbps

3 parallel bits

4 parallel bits

1.544 Mbps

T1 out

HDSL2 Framer

Descrambler

HDSL2 Receiver (as approved by T1E1.4 subcommittee)

December 9, 1997
## Estimate of Processing Power and Memory

<table>
<thead>
<tr>
<th>Module</th>
<th>Multiplications (in millions/sec)</th>
<th>Additions (in millions/sec)</th>
<th>Memory (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Framer</td>
<td>none</td>
<td>1.544</td>
<td>FrameSize</td>
</tr>
<tr>
<td>Scrambler</td>
<td>none</td>
<td>3 x 1.552</td>
<td>24 x 16 x 2</td>
</tr>
<tr>
<td>Trellis encoder</td>
<td>none</td>
<td>9 x 1.552</td>
<td>10 x 16</td>
</tr>
<tr>
<td>Bits to Symbol</td>
<td>none</td>
<td>none</td>
<td>2 x 16 x 16</td>
</tr>
<tr>
<td>Tomlinson precoder</td>
<td>100 x 1.552/3 + update</td>
<td>100 x 1.552/3 + update</td>
<td>100 x 16</td>
</tr>
<tr>
<td>Transmit filter</td>
<td>50 x 1.552/3</td>
<td>50 x 1.552/3</td>
<td>50 x 16</td>
</tr>
<tr>
<td>Echo canceler</td>
<td>100 x 1.552/3 + update</td>
<td>100 x 1.552/3 + update</td>
<td>100 x 16</td>
</tr>
<tr>
<td>Receiver filter</td>
<td>50 x 1.552/3</td>
<td>50 x 1.552/3</td>
<td>50 x 16</td>
</tr>
<tr>
<td><strong>Trellis decoder</strong></td>
<td>512 x 2 x 2 x 1.552/3 = 2048 x 1.552/3</td>
<td>512 x 2 x 1.552/3</td>
<td>80 x 1024</td>
</tr>
<tr>
<td>Symbol to bits</td>
<td>none</td>
<td>none</td>
<td>2 x 16 x 16</td>
</tr>
<tr>
<td>Descrambler</td>
<td>none</td>
<td>3 x 1.552</td>
<td>24 x 16 x 16</td>
</tr>
<tr>
<td>Framer</td>
<td>none</td>
<td>1.554</td>
<td>FrameSize</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td>1214.7 + 2 x update</td>
<td>711.34 + 2 x update</td>
<td>89,440</td>
</tr>
</tbody>
</table>
Summary

- HDSL2 requires about 1.2 billion MACs
- Viterbi decoder takes about
  - 87% of processing power
  - 91% of memory
- **Aim**: Implement HDSL2 modem using
  - high-end DSP processors
  - coprocessors
- **Optimization**
  - Design transmit and receive filters to have dyadic coefficients
  - Replace Euclidean distance in Viterbi decoder with absolute differences
- **Current work on HDSL2 modem design**
  - Develop minimum phase transmit and receive filters
  - Embedded implementation of Viterbi decoder on DSP processors
  - Efficient implementation of echo cancelers and other filters
  - Replacing DSP processors with microcontrollers to reduce cost