

# Stephen Bijansky

2000 Cullen Avenue #12  
Austin, TX 78757  
512.467.2547  
bijansky@ece.utexas.edu

- Objective** To obtain a part time teaching position.
- Education**
- University of Texas** December 2008  
Ph.D. program in Electrical and Computer Engineering  
**GPA: 4.0**
- Carnegie Mellon University** December 1998  
Masters of Science in Electrical and Computer Engineering  
**GPA: 3.7**
- University of Delaware** May 1997  
Honors Bachelor of Electrical Engineering  
Minor: Applied Music - Horn  
**GPA: 3.7**
- Experience**
- Qualcomm** December 2007 – Present  
Senior Engineer
- Custom circuit designer of caches for a digital signal processor. Performed logic design, characterization, .lib generation, and power estimation. Developed a power estimation flow for custom circuits using a schematic netlist, Verilog simulation, and extracted node capacitances.
- University of Texas** August 2002 – December 2008  
Research Assistant
- Researched a dual-Vdd design style, and associated CAD algorithms, wherein we assign supply voltages to logic based on post-manufacturing analysis rather than designing with nominal values and guard banding. The goal was to develop an adaptive fabric that can be configured in order to improve performance, reduce power, or both. Ran HSpice Monte Carlo simulations to determine variability performance. Performed Verilog modeling to verify correctness.
- Dynocom Industries** June 2003 – Present  
Embedded Computer Engineer
- Designed embedded hardware and firmware to control and monitor chassis dynamometer using Microchip PIC18 microcontrollers. Designed and debugged PCB hardware. Wrote firmware to control USB, SPI, RS232, A/D conversion, LCD display, PWM signals, air fuel sensor, eddy brake power absorption unit, PID steady state feedback loop, and microcontroller bootloader. Wrote Windows XP C++ program to communicate with microcontroller using USB.
- Pyxis Technology** June 2007 – August 2007  
Computer Engineer
- Performed crosstalk analysis on benchmark circuits using PrimeTime SI. Evaluated crosstalk metrics for total negative slack, worst slack, and slack distribution. Investigated methods to reduce crosstalk by identifying which nets should receive priority during routing.
- Magma Design Automation** May 2006 – August 2006  
Computer Engineer
- Wrote a program to determine and characterize internal flop and latch nodes to get more accurate initial delay values, which enabled a speed up in constraint library characterization. Investigated methods to extrapolate multiple PVT characterizations from a smaller subset of characterizations.

**Dell Computer Corporation**  
Storage Systems Architect

January 1999 – August 2002

Evaluated Network Attached Storage technologies including Windows 2000, Linux 2.4, journaling filesystems, gigabit ethernet, snapshots, TCP offloading, distributed file systems, hardware RAID, software RAID, and SAN integration. Performed benchmarking on a large number of NAS platforms to determine performance and scalability. Prototyped low end NAS hardware.

**Carnegie Mellon University, Parallel Data Lab**  
Research Assistant

August 1997 – December 1998

Investigated the effects of storage based traffic on network performance. Changed tcp code in the Linux kernel to determine why some message sizes received poor bandwidth. Investigated network performance of many servers sending data concurrently to one client.

**University of Delaware**  
Research Assistant

Summer 1997, Summer 1996

Wrote a C encryption benchmark, a Perl web link checker, and interfaced a Perl remote camera program to a Java applet. Installed and maintained multicast video conferencing programs on a variety of Unix machines.

**University of Texas and University of Delaware**

Teaching Assistant, EE360R VLSI	Fall 2007
Teaching Assistant, EE360C Algorithms	Fall 2006, Fall 2005, Fall 2004, Fall 2003
Teaching Assistant, EE382C Hw/Sw Codesign	Spring 2004
Teaching Assistant, EE464 Senior Design Project	Spring 2003
Teaching Assistant, EE302 Intro to Elec and Comp Engr	Fall 2002
Teaching Assistant, Eleg 302 Material Science for EE's	Spring 1996
Teaching Assistant, Eleg 210 Intro to Combinational Logic	Fall 1995

**Related Courses**

Nanometer Scale IC Design	Operating System Design
CAD for Deep Submicron VLSI	Advanced Embedded Systems
Simulation Methods in CAD/VLSI	Memory System Design
VLSI II	Advanced Storage and File Systems
VLSI I	Vivisecting the Internet
Analog IC Design	Security and Cryptography
Hardware/Software Codesign	OOP, Java, and the WWW
Parallel Computer Architecture	Advanced Digital Design Project
Digital Integrated Circuits	Superscalar Processor Design

**Academic Projects**

*Advanced Digital Design Project*  
Designed and implemented a FPGA coprocessor to speed up image compression.

*VLSI Systems*  
Designed and implemented a digital median filter using Magic layout and Spice simulation tools.

*Operating Systems Project*  
Designed and implemented a user level file system.

*Senior Honors Thesis: Long-Range Dependence in Internet Traffic*  
Analyzed Internet traffic using Matlab in order to characterize wide area networks.

**Academic Awards**

University of Texas Engineering Doctoral Fellowship	Undergraduate Research Scholar
Carnegie Mellon Fellowship	Milton G. Young Award
Linton Houston Scholarship	Alumni Award
Peter Warter Scholarship	Advanced Honors Certificate

**Computer Skills**

**Programming Languages:** C++, Java, C, Perl, TCL, Verilog  
**Operating Systems:** Linux, Windows XP, Unix, Solaris  
**Applications:** HSpice, PrimeTime SI, Nanotime, Cadence Virtuoso, Synopsys VCS, Magma Blast Fusion, Cadabra, ESP-CV, Verplex, Magic, Matlab, Netbench, MediaWiki, Apache