

EE382V: VLSI Physical Design Automation

Fall 2008 (Prof. David Pan)

Homework #2: due Oct. 8, 2008

1. Polish Expression: Consider the following slicing floorplan with 8 modules represented with a polish expression: 235V4HV18VH7V6V. The dimensions of the modules 1 through 8 are $\{(2,4), (2, 4), (3,3), (5,3), (1,3), (1,4), (3,6), (4,2)\}$.

- Draw the corresponding slicing tree.
- Find out the area of the smallest rectangle that can accommodate the modules with no overlap. Each module is free to rotate by 90° .
- Draw the optimally-sized slicing floorplan using (x, y) coordinates.

2. Stockmeyer algorithm: Prove why the number of candidate dimensions stored at each internal node is linear in terms of the total number of blocks.

3. Mixed ILP: Consider the following four modules to be floorplanned: $\{m_1 = \text{dimension } 7 \times 4, m_2 = \text{dimension } 4 \times 6, m_3 = \text{area } 30 \text{ with } 1/2 < w/h < 2, m_4 = \text{area } 40 \text{ with } 0.3 < w/h < 2.5\}$.

- How many continuous and integer variables are required if rotation is not allowed?
- Give the complete mixed ILP formulation for the given floorplanning problem with area minimization, **assuming the width W is fixed** (90° rotation is allowed).
- If the half-perimeter of bounding box of net $n_1 = \{m_1, m_3, m_4\}$ needs to be bounded by the length of 10, what are the additional constraints that need to be added?

4. Sequence Pair: Consider the following non-slicing floorplan with 8 modules represented with a sequence pair: (76451328, 12786534). The module dimensions are the same as in Problem 1.

- Draw the corresponding horizontal constraint graph.
- Draw the corresponding vertical constraint graph.
- What is the area of the smallest rectangle that can accommodate the modules with no overlap?
- Draw the corresponding non-slicing floorplan using (x, y) coordinates.