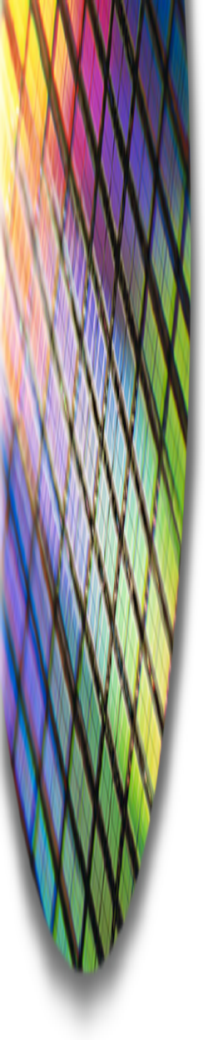


My Take on ASP-DAC on its 20th Anniversary

David Z. Pan

Dept. of Electrical and Computer Engineering

The University of Texas at Austin

http://www.cerc.utexas.edu/utda

Congratulations to ASP-DAC!

Congratulations to ASP-DAC!

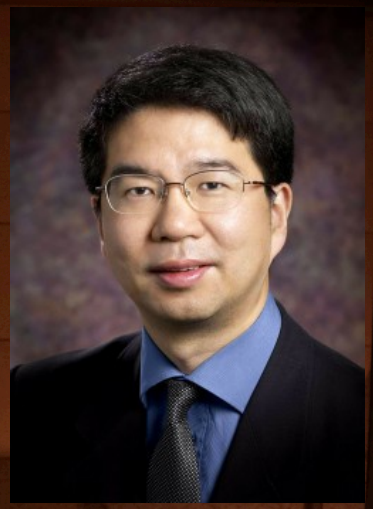
Disclaimer

- I am truly honored and humbled to be asked to give this talk, for the 20th anniversary celebration
- There are many, many key contributors of ASP-DAC who are more qualified than me to give this talk, in particular, on the history of ASP-DAC, etc. (I need to grow more gray hairs for that ☺)
- I will share my personal experience and perspective

So, where was I in 1995?

- The first ASP-DAC was held 08.29-9.1.1995 in Makuhari
- At that time, I was a graduate student in Physical Sciences
- Just took an introductory CS class
- Know nothing about VLSI or CAD
- So, I was really **a new born baby in EDA** ☺

Luckily, I met Prof. Jason Cong who introduced me into the new world of EDA



I received this award last night as Prof. Jason Cong's proxy

My ASP-DAC History

- My first ASP-DAC paper in 1999 (Hong Kong)
- My second ASP-DAC paper in 2001 (Japan)
- ----------
- My first physical attendance at ASP-DAC was actually 2005 – **exactly 10 years ago** in Shanghai ☺
  - G. Xu, L. Huang, D. Z. Pan and M. D.-F. Wong, "Redundant-Via Enhanced Maze Routing for Yield Improvement"
  - 10-year Retrospective Most Influential Paper Award Candidate
- Regularly submit papers to ASP-DAC
  - 30 papers at ASP-DAC (including several invited papers)
- Best Paper Award twice (2010 and 2012)
- Best Paper Award Nomination in 2006, 2008, 2013
- ASP-DAC Frequently Cited Author Award

My first ASP-DAC paper, in 1999

Interconnect Delay Estimation Models for Synthesis and Design Planning

Jason Cong and David Z. Pan

UCLA Computer Science Department
Los Angeles, CA 90095

Sponsored by SRC and Intel

Interconnect Layout Optimization

- E.g., UCLA **TRIO** (Tree, Repeater, Interconnect Optimization) Package
  - Interconnect topology optimization
  - Optimal buffer insertion
  - Wiresizing optimization
  - Global interconnect sizing and spacing
  - Simultaneous driver, buffer & interconnect sizing
  - Simultaneous topology generation with buffer insertion and wiresizing
- Delay can be improved many times

Main Results and Impact

- Develop a set of delay estimation models, under different optimizations such as wire sizing, driver sizing, buffer insertion/sizing, etc.
  - Closed-form formula or simple characteristic equations
  - Constant running time in practice
  - High accuracy (about 90% on average)
  - Great for interconnect planning
- Impacts:
  - Citation: 68 (based on Google Scholar)
  - Widely adopted by industry (IBM, Freescale, Intel, etc.)
  - Jason Cong's SRC Technical Excellence Award in 2000, for "Interconnect Estimation, Planning and Synthesis for Deep Sub-micron Designs"

My second ASP-DAC paper, in 2001

Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization

Jason Cong, Zhigang (David) Pan,
and P.V. Srinivas*

Computer Science Department
University of California, Los Angeles
* Magma Design Automation Inc.

Sponsored by SRC

Main Results and Impact

- Develop a closed-form crosstalk noise model, which has high fidelity cf. detailed spice simulations
- Unified previous crosstalk noise models
- Great to guide crosstalk optimizations during physical synthesis (buffer insertion, driver sizing, spacing, …)

- Impacts:
  - Citation: 146
  - US Patent issued
  - Used by Magma (acquired by Synopsys)

My first physical presence at ASP-DAC, Shanghai, 2005

Redundant Via Enhanced Maze Routing for Yield Improvement

Gang Xu
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Texas Instruments
lida@ti.com

David Z. Pan
ECE Department
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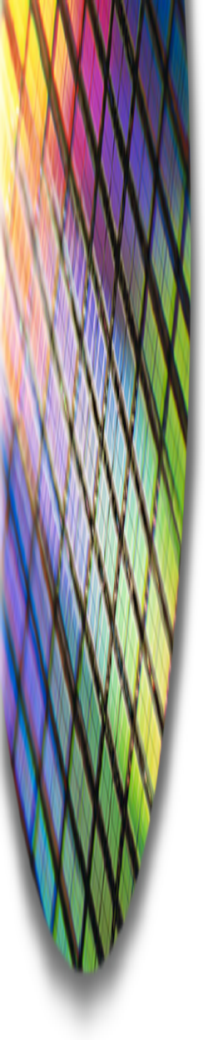
dpan@ece.utexas.edu

Martin D.F. Wong
ECE Department
University of Illinois at Urbana-Champaign
mdfwong@uiuc.edu

Main Results and Impact

- The first paper on redundant via aware routing
- Proposed on-track, off-track redundant vias
- Constrained optimization with Lagrangian Relaxation
- Impacts:
  - Citation: 91
  - 10-year Retrospective Most Influential Paper Award Candidate
  - The first paper on redundant via aware routing
  - All major fabs strongly recommend redundant vias
  - All modern EDA commercial routers have redundant via insertion awareness



MeshWorks: An Efficient Framework for Planning, Synthesis & Optimization of Clock Mesh Networks

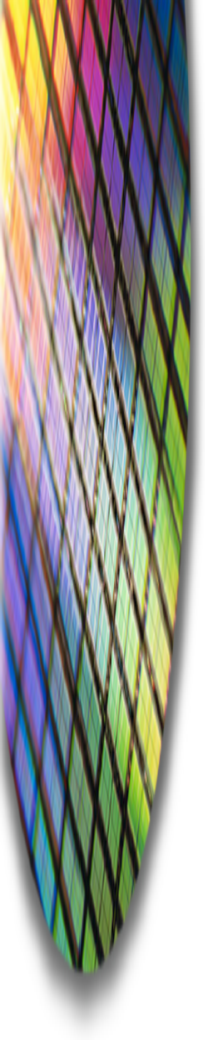
Anand Rajaram[§*] and David Z. Pan[§]

§ ECE Department, University of Texas at Austin.

*** DDSP, Texas Instruments, Dallas.**

Main Results and Impact

- We proposed a systematic methodology for clock mesh planning, synthesis, and optimization
- Impacts:
  - Citation: 42
  - **ASP-DAC'08 Best Paper Candidate**
  - The first paper on fully automatic clock mesh synthesis
  - Clock mesh design was mostly done manually before
  - Now it is available in EDA tools as high-performance ASIC designs may need some mesh-like structures to deal with PVT variations

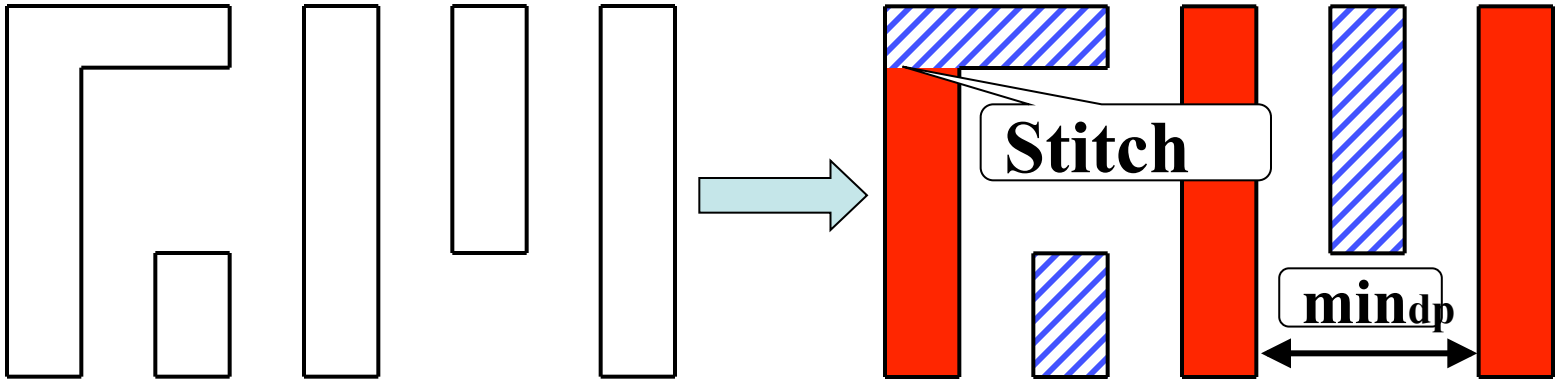


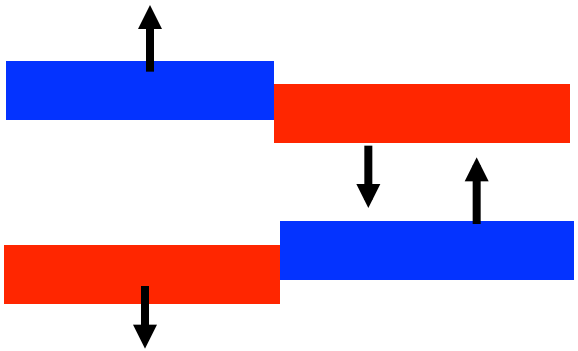
A New Graph-Theoretic, Multi-Objective Layout Decomposition Framework for Double Patterning Lithography

Jae-Seok Yang, Katrina Lu, Minsik Cho, Kun Yuan, and David Z. Pan

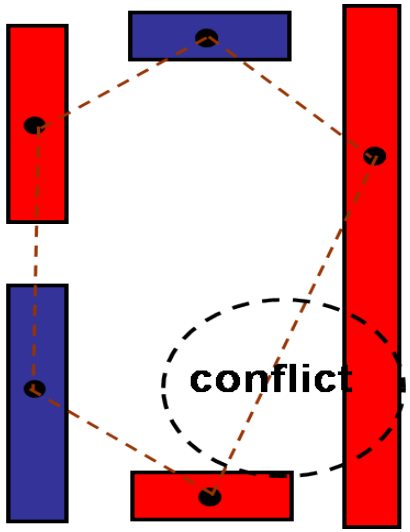
ECE Department, University of Texas at Austin

What is Double Patterning?





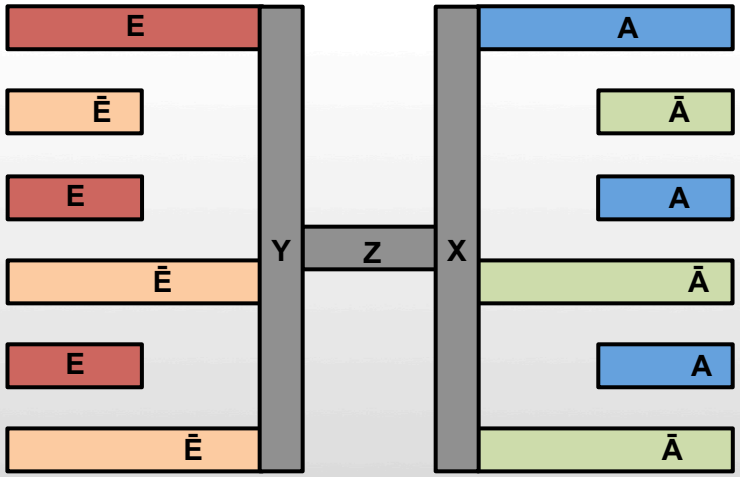
Overlay Error

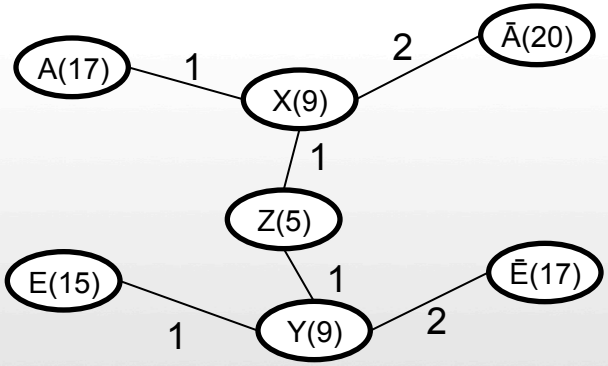


A Graph-Partitioning Based, Multi-Objective Decomposer

Decomposition Graph Construction

[Yang+, ASPDAC10]





Constraint:
(A, Ā) and (E, Ē) are repulsive pairs.

Theorem : Stitch minimization problem is equivalent to the min-cut partitioning of the decomposition graph

Extensions of the framework: to incorporate other constraints and costs into graph partitioning, e.g., balanced density, overlay compensation, and so on

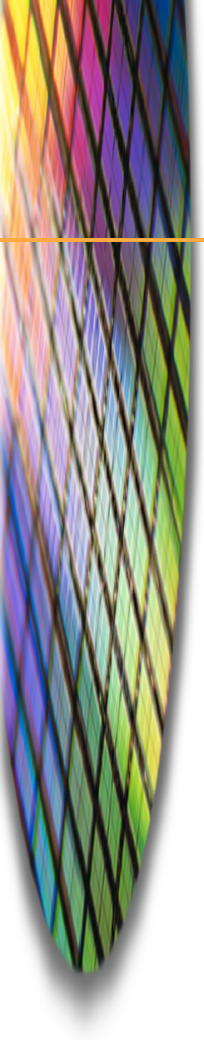
Main Results and Impact

- First holistic framework to consider overlay compensation, stitch minimization, and balanced density together
- Easily adjust weights/multi-objective; very fast
- Impacts:
  - Citation: 51
  - **ASP-DAC 2010 Best Paper Award**
  - **IBM Research 2010 Pat Goldberg Memorial Best Paper Award in CS/EE/Math** (among all papers in very broad areas under CS, EE, and mathematical sciences co-authored by IBM's 4000+ researchers in 2010)
  - Industry usage of double/triple patterning (layout decomposition is a key step for both mask/PD)

Back in 2003

”Daddy, don’t worry. I can show you some **bright** idea!”

“Double patterning!!!”



EPIC: Efficient Prediction of IC Manufacturing Hotspots using a Unified Meta-Classification Method

Duo Ding, Bei Yu, Joydeep Ghosh and David Z. Pan

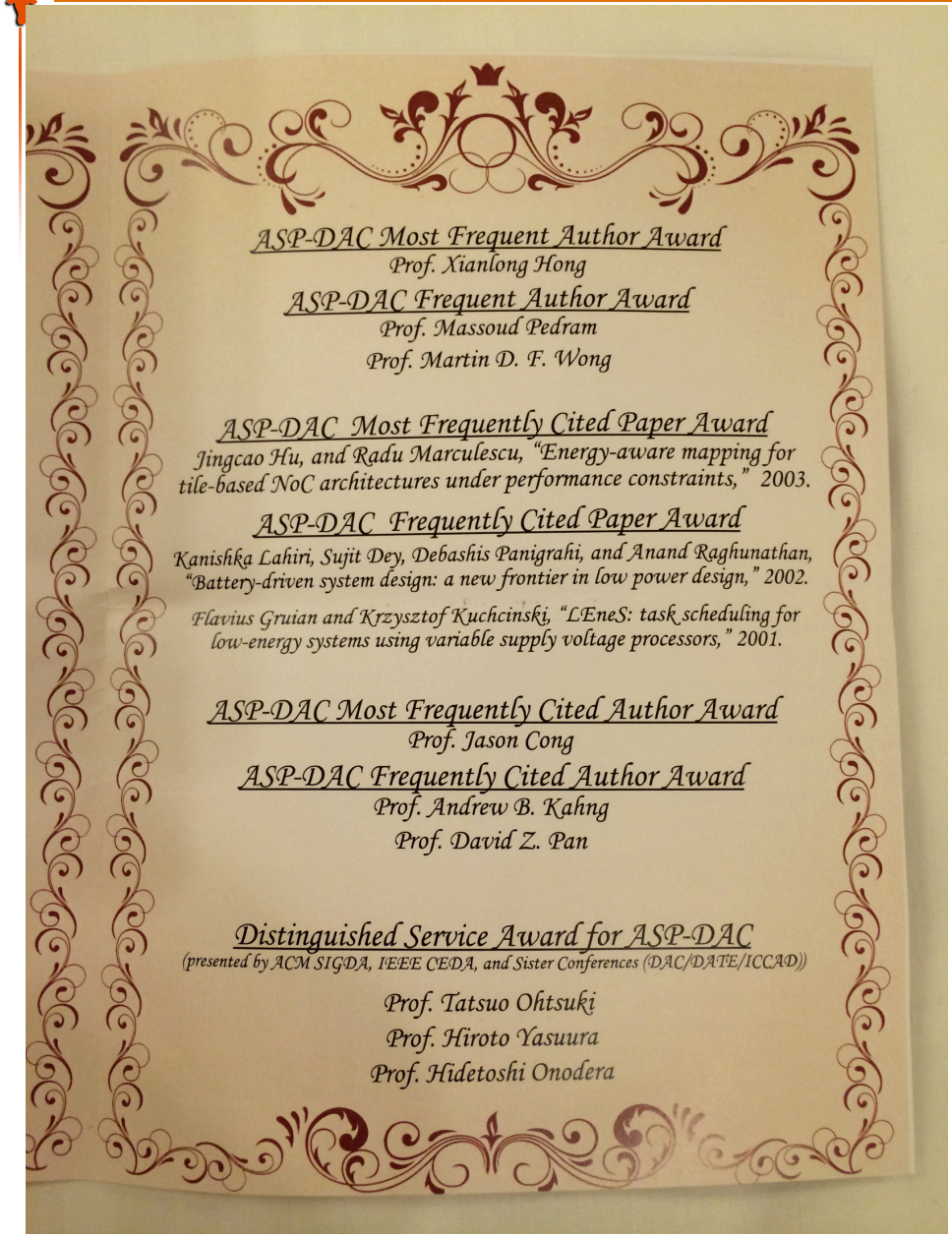
Dept. of Electrical and Computer Engineering
The Univ. of Texas at Austin

http://www.cerc.utexas.edu/utda

Main Results and Impact

- Proposed a novel meta-classification method to unify machine learning and pattern matching methods together
- Impacts:
  - **ASP-DAC 2012 Best Paper Award**
  - ASP-DAC 2011 paper: “High performance lithographic hotspot detection using hierarchically refined machine learning” (citation: 30)
  - Helped spark the **ICCAD 2012 CAD Contest**, organized by Mentor Graphics, on “Lithography Hotspot Detection” (many teams participated)
  - Very well attended ASPDAC’15 Special Session on “Machine Learning in EDA” yesterday

ASP-DAC is Truly International



ASP-DAC Top Authors (based on DBLP, up to 2014)

Xianlong Hong (56)
Massoud Pedram (41)
Martin D. F. Wong (38)
Yici Cai (36)
Chung-Kuan Cheng (34)
Jason Cong (33)
Hidetoshi Onodera (29)
Sheldon X.-D. Tan (28)
David Z. Pan (27)
Yuan Xie (26)
Andrew B. Kahng (25)
Sung Kyu Lim (23)
Hai Zhou (22)
Kwang-Ting Cheng (21)
Masanori Hashimoto (21)
Jing-Yang Jou (20)
Sachin S. Sapatnekar (20)
Kenichi Okada (20)
Kaushik Roy (20)
Nozomu Togawa (19)
Tsutomu Sasao (19)
Lei He (19)
Rolf Drechsler (19)
Yao-Wen Chang (19)

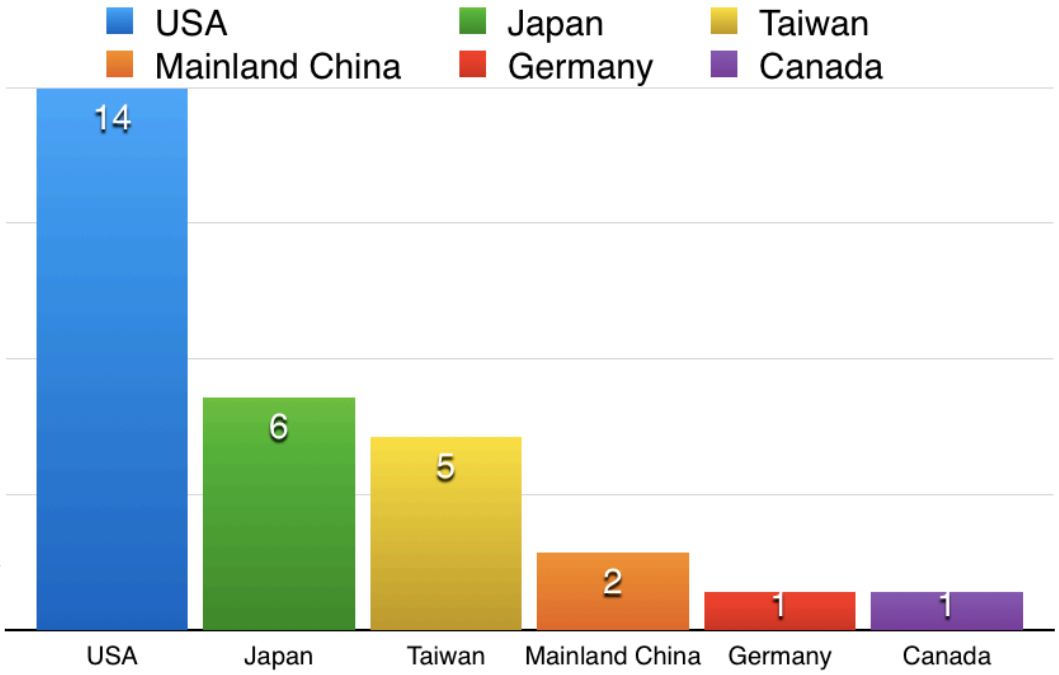
How to Win an ASP-DAC BPA?

- I hope I have a secret sauce

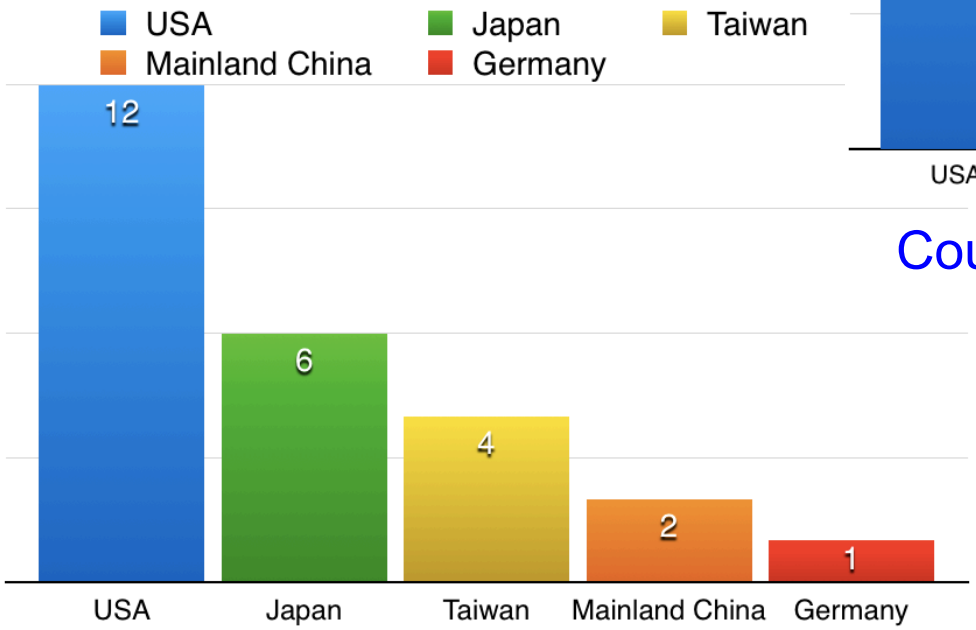
- Seriously, just submit your best work to ASP-DAC
- Then don't worry about it
- Right topic + elegant algorithm + a lot of luck!

ASP-DAC Best Paper Statistics

Based on published data - missing years 2004, 2001, and 1995-1999



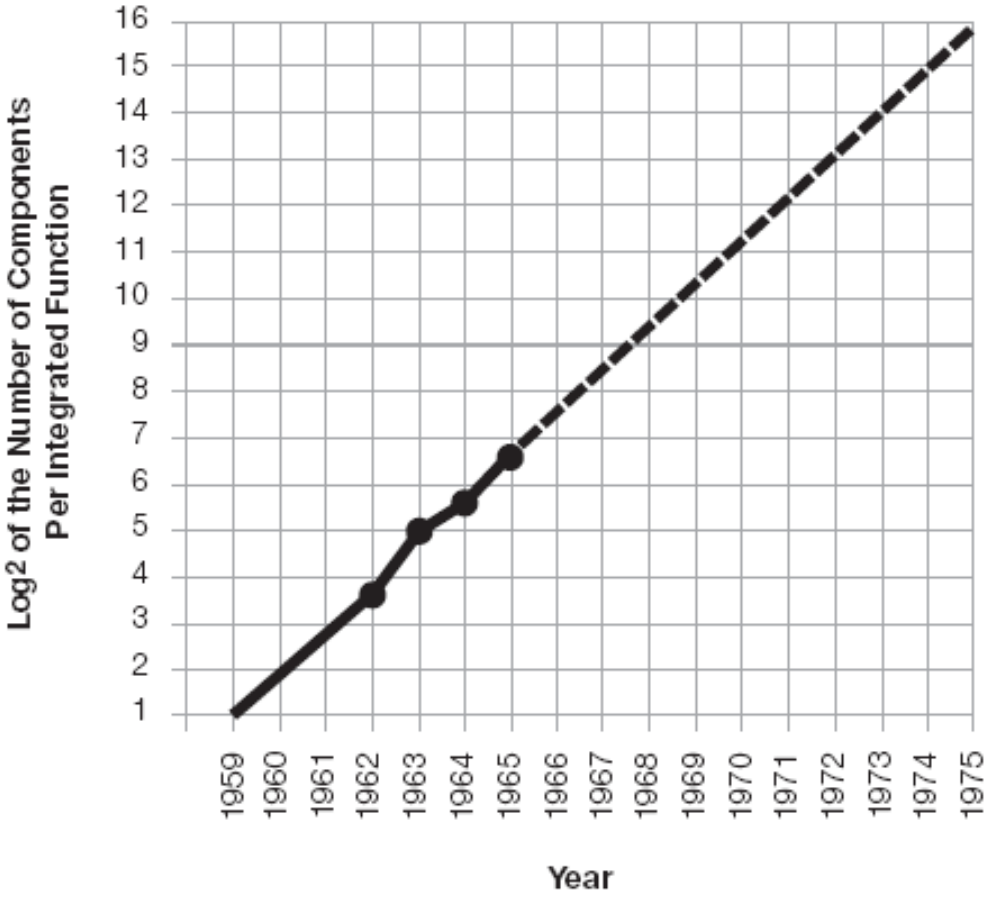
Count other author countries as well



Only count first/contact authors

Moore's Law 50th Anniversary!

- Moore's original paper in 1965



[Moore, 1965]

Moore's Law Amendment

NO EXPONENTIAL IS FOREVER…

BUT

WE CAN DELEY "FOREVER"

[Moore, ISSCC 2003]

Future "EDA" Research

- More Moore: continue pushing the envelope, 14nm, 11nm, 7nm
  - Multiple patterning and emerging lithography
  - Computational scaling (CAD tools still very sub-optimal)
- More than Moore: New CAD issues
  - Vertically – 3D IC integration
  - New device/material: FINFET, III-V, graphene, …
  - New domains: Bio, Photonic, …
  - New applications: energy, big data, security, automotive, …
- **"EDA" – Extreme Difficulty Automation**
  - You can do anything if you can handle "EDA"

I ♥ ASP-DAC

ASPDAC'15 TPC Meeting
Daejeon

ASPDAC'06, Yokohama

Wish ASP-DAC Greater Success!

ASPDAC'12, Sydney