EE382M-26: VLSI CAD & Optimizations
(Fall 2018 - 16935)

Instructor: Prof. David Z. Pan

Lecture hours and location: Tue/Thu 3:30-5:00pm, ECJ 1.316

Instructor: Prof. David Z. Pan
- Office: EER 4.880; Phone: 512-471-1436
- Office hours: Monday and Thursday 1:30-2:30pm, and by appointment.
- Email: dpan@ece.utexas.edu

TA: Keren Zhu
- Office: EER 4th floor 4.852
- Office hours: Friday 2-4pm and by appointment.
- Email: keren.zhu@utexas.edu

The course materials are at UT Canvas https://canvas.utexas.edu/

Course description:
As modern VLSI technology scales into deep sub-micron dimension and the system-on-chip (SoC) complexity reaches billions of transistors, computer aided design (CAD) algorithms, tools, and methodologies are indispensable in obtaining the overall performance, power, and area (PPA) optimizations, under stringent time-to-market requirement. Meanwhile, as technology scaling continues, new challenges in manufacturability, reliability, security, and so on keep emerging and again, intelligent CAD and optimizations play a key role in achieving the overall design and manufacturing closure. This course will introduce a number of key VLSI CAD techniques with underlying modeling issues to deal with these nanometer IC design challenges. Guest lecturer(s) from industry will be invited to provide supplementary views and practical challenges and practices.

TOPICS OUTLINE (tentative)

1. Introduction and IC technology trends
2. Modeling and optimization in VLSI/CAD overview
3. Transistor/gate sizing, wire sizing/spacing/planning
4. Buffer insertion, optimization, and planning
5. Congestion and crosstalk noise optimization
6. Clock network synthesis
7. Modern VLSI placement techniques
8. Low power design and optimizations
9. Design for manufacturability
10. Design for reliability
11. Hardware security

12. Machine learning in EDA
13. CAD for FPGA and emerging technologies (3D-IC, nanophotonics, etc.)

Prerequisite:
Introduction to VLSI (460R or equivalent) and Algorithms (360C or equivalent), or consent of the instructor.

Grading Policy (tentative):
10% class participation/presentation, 20% homework, 30% midterm, 40% project.

Textbook and Reader:
No textbook is required. A collection of reference books and papers will be posted on the class web site as a course reader.

REFERENCES

- **Mainly based on technical papers from journals and conference proceedings, such as TCAD, TVLSI, DAC, ICCAD, ASPDAC, ISPD, ISLPED, etc.**
- Bei Yu and David Z. Pan, *Design for Manufacturability with Advanced Lithography*, Springer, 2016
- David Z. Pan, Minsik Cho, Yuan Kun, *Manufacturability Aware Routing in Nanometer VLSI (Foundations and Trends in Electronic Design Automation),* Now Publishers, 2010
- Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, *Handbook of Algorithms for Physical Design Automation*, CRC Press, 2009
- Luciano Lavagno, Grant Martin, and Louis Scheffer, *Electronic Design Automation for Integrated Circuits Handbook* - 2 Volume Set, April 2006
- Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, *VLSI Physical Design: From Graph Partitioning to Timing Closure*, Springer 2011
- Jan Rabaey, *Low Power Design Essentials*, Springer 2009
- Yuan Xie, Jingsheng Jason Cong, Sachin Sapatnekar, *Three-Dimensional Integrated Circuit Design: EDA, Design and Microarchitectures*, Springer, 2010
- Sung Kyu Lim, *Design for High Performance, Low Power, and Reliable 3D Integrated Circuits*, Springer 2012

College of Engineering Drop/Add Policy:
The Dean must approve adding or dropping courses after the fourth class day of the semester.

Students with Disabilities:
The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4641 TTY or the College of Engineering Director of Students with Disabilities at 471-4382.