EE382V: VLSI Physical Design Automation

Spring 2015 (Prof. David Pan)

Homework #2: due Feb. 23, 2015

1. Polish Expression: Consider the following slicing floorplan with 8 modules represented with a polish expression: 235V4HV18VH7V6V. The dimensions of the modules 1 through 8 are {(2,4), (2, 4), (3,3), (5,3), (1,3), (1,4), (3,6), (4,2) }.

   a) Draw the corresponding slicing tree.
   b) Find out the area of the smallest rectangle that can accommodate the modules with no overlap. Each module is free to rotate by 90°.
   c) Draw the optimally-sized slicing floorplan using (x, y) coordinates.

2. Stockmeyer algorithm: Prove why the number of candidate dimensions stored at each internal node is linear in terms of the total number of blocks.

3. Mixed ILP: Consider the following four modules to be floorplanned: {m1 = dimension 7×4, m2 = dimension 4×6, m3 = area 30 with $1/2 < w/h < 2$, m4 = area 40 with $0.3 < w/h < 2.5$}.

   a) How many continuous and integer variables are required if rotation is not allowed?
   b) Give the complete mixed ILP formulation for the given floorplanning problem with area minimization, assuming the width W is fixed (90° rotation is allowed).
   c) If the half-perimeter of bounding box of net n1= {m1,m3,m4} needs to be bounded by the length of 10, what are the additional constraints that need to be added?

4. Sequence Pair: Consider the following non-slicing floorplan with 8 modules represented with a sequence pair: (76451328, 12786534). The module dimensions are the same as in Problem 1.

   a) Draw the corresponding horizontal constraint graph.
   b) Draw the corresponding vertical constraint graph.
   c) What is the area of the smallest rectangle that can accommodate the modules with no overlap?
   d) Draw the corresponding non-slicing floorplan using (x, y) coordinates.