THE UNIVERSITY OF TEXAS AT AUSTIN
Cockrell School of Engineering
Standard Resume

FULL NAME: David Z. Pan

TITLE: Professor, Engineering Foundation Endowed Professorship #1

DEPARTMENT: Electrical and Computer Engineering, The University of Texas at Austin

EDUCATION:

University of California, Los Angeles	Computer Science	Ph.D.	Fall 2000
University of California, Los Angeles	Computer Science	M.S.	Fall 1998
University of California, Los Angeles	Atmospheric Sciences	M.S.	Fall 1994
Peking University, China	Physics	B.S.	Spring 1992

CURRENT AND PREVIOUS ACADEMIC POSITIONS:

The University of Texas at Austin	Professor, Engineering Foundation Endowed Professorship #1	09/2014 –
The University of Texas at Austin	Professor, Brasfield Endowed Faculty Fellow	09/2013 – 08/2014
The University of Texas at Austin	Associate Professor	09/2008 – 08/2013
The University of Texas at Austin	Assistant Professor	09/2003 – 08/2008
Technical Univ. of Munich, Germany	Visiting Professor / IAS Visiting Fellow	05/2015 – 07/2015
Fudan University, China	Distinguished Guest Professor	2013 -
Zhejiang University, China	Y.C. Tang Chair Guest Professor	2008 - 2011
Technical Univ. of Dresden, Germany	Visiting Professor	June to July, 2008
Shanghai Jiaotong University, China	Guest Professor	2004 - 2005

OTHER PROFESSIONAL EXPERIENCES:

IBM T. J. Watson Research Center	Research Staff Member	October 2000 - August 2003

CONSULTING:

LATHAM & WATKINS LLP	Consultant	2016
Cooley LLP	Consultant	2013-2014
Tabula, Inc.	Advisor and Consultant	2012-2015
Pyxis Technology Inc. (Acquired by Mentor Graphics in 2011)	Member of Technical Advisory Board	2005 - 2011
Cadence Design Systems	Consultant	2008
Fish & Richardson, P.C.	Consultant	2006 - 2007

HONORS AND AWARDS (SELECTED):

- 2017 **Best Paper Award**, IEEE International Symposium on Hardware Oriented Security and Trust (HOST)
- 2017 ACM International Symposium on Physical Design (ISPD) **Contest: 1st Place**
- 2017 **SPIE Fellow,** for achievements in IC design for manufacturing with advanced lithography
- 2016 Honor for PhD Student Xiaoqing Xu: **ACM/SIGDA Student Research Competition Gold Medal** (Graduate Category) at ICCAD 2016
- 2016 ACM International Symposium on Physical Design (ISPD) **Contest: 1st Place**

- 2016 SPIE Advanced Lithography **Franco Cerrina Memorial Best Student Paper Award**
- 2015 **Best in Session Award**, SRC Techcon Conference
- 2015 Honor for PhD Student Bei Yu: **European Design and Automation Association** (**EDAA) Outstanding Dissertation Award**
- 2015 Asian and South Pacific Design Automation Conference (ASP-DAC) **Frequently Cited Author Award** (given to the top 3 cited authors in ASP-DAC's 20-year history)
- 2015 ASP-DAC 10-Year Retrospective Most Influential Paper Award Candidate
- 2014- **Engineering Foundation Endowed Professorship #1**, The University of Texas at Austin
- 2014 **RAISE Faculty Excellence Award** -- Recognizing Asian & Asian American Faculty & Staff Instilling Strength and Excellence, The University of Texas at Austin
- 2014 **Best Paper Award**, ACM International Symposium on Physical Design (ISPD)
- 2014 **IEEE Fellow**, for contributions to design for manufacturability in integrated circuits
- 2014 Communications of the ACM (CACM) **Research Highlights**, for "Full-Chip Mechanical Reliability Analysis and Optimization for 3D ICs"
- 2013 **ICCAD CAD Contest Award** (the 2nd Place) in "Mask Optimization"
- 2013 Honor for PhD Student Bei Yu: **ACM/SIGDA Student Research Competition Silver Medal** (Graduate Track) at ICCAD 2013
- 2013 IEEE/ACM **William J. MacCalla ICCAD Best Paper Award**
- 2013 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), **Keynote Paper** for "Design for Manufacturing with Emerging Nanolithography"
- 2013 **SRC Technical Excellence Award**, for "Nanometer IC Design for Manufacturability" with the citation "In recognition of your key contributions to technology that have significantly enhanced the productivity of the semiconductor industry"
- 2013 **Earl N. & Margaret Brasfield Endowed Faculty Fellowship** in Engineering, UT Austin
- 2013 **DAC Top 10 Author in Fifth Decade**, for being one of the top 10 most prolific authors for DAC's fifth decade
- 2013 **DAC Prolific Author Award** - DAC 25 Club, for having published 25 or more papers at the Design Automation Conference
- 2013 Keynote Speaker, the 22nd ACM/IEEE International Workshop on Logic & Synthesis (IWLS)
- 2013 Honor for PhD Student Duo Ding: **ACM Outstanding PhD Dissertation Award in EDA**
- 2012 Fall UT-ECE Senior Design Open House, the 1st Place Winning Team, Faculty Mentor
- 2012 **ICCAD CAD Contest Award** in "Fuzzy Pattern Matching for Physical Verification", the 2nd Place
- 2012 **Best Paper in Session Award**, SRC Techcon Conference
- 2012 **Best Paper Award**, ACM/IEEE Asian and South Pacific Design Automation Conference
- 2011 **Overseas and Hong Kong/Macau Scholars Collaborative Research Award** (a.k.a. Overseas Distinguished Young Scholar) by National Natural Science Foundation of China (NSFC)
- 2011 **IBM Research Pat Goldberg Memorial Best Paper Award** for 2010 in Computer Science, Electrical Engineering and Math
- 2011 Keynote Speaker, the 18th IEEE/ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)
- 2011 **Best Paper Award**, ACM International Symposium on Physical Design (ISPD)
- 2010 **IBM Faculty Award**
- 2010 **Best Paper Award**, ACM/IEEE Asian and South Pacific Design Automation Conference (ASPDAC)
- 2009 UCLA School of Engineering and Applied Science, **Distinguished Young Alumnus Award**
- 2009 **Best Student Paper Award**, IEEE International Conference on IC Design and Technology (ICICDT)
- 2009 Grand Prize ($25,000), eASIC Placement Worldwide Contest
- 2009 **Best Paper (IP) Award**, IEEE/ACM Design Automation & Test in Europe (DATE)
- 2008-2009 IEEE Circuits & Systems (CAS) Society Distinguished Lecturer
- 2008 Semiconductor Research Corporation (SRC) **Inventor Recognition Award**
- 2008 Association for Computing Machinery (ACM) Recognition of Service Award

- 2008 Keynote Speaker, Freescale Physical Design and Design for Manufacturing (DFM) Conference
- 2007 **Best Paper in Session Award**, SRC Techcon Conference
- 2007 **National Science Foundation (NSF), Faculty Early Career Development (CAREER) Award**
- 2007 Cadence Distinguished Speaker
- 2007 Association for Computing Machinery (ACM) Recognition of Service Award
- 2007 IEEE CEDA Award for the Open Source BoxRouter 2.0
- 2007 ACM International Symposium on Physical Design (ISPD) **Routing Contest Awards**: the 2nd place in 3D and the 3rd place in 2D
- 2006 **IBM Faculty Award**
- 2005 **IBM Faculty Award**
- 2005 **ACM/SIGDA Outstanding New Faculty Award**
- 2004 **IBM Faculty Award**
- 2003 IBM Research Bravo Award
- 2001 Outstanding Ph.D. Award, UCLA Computer Science Department
- 2000 SRC Inventor Recognition Award
- 2000 Dimitris Chorafas Foundation Award
- 1999-2000 IBM Research Fellowship
- 1998 Best Paper in Session Award, SRC Techcon Conference
- **11 additional Best Paper Award Finalists/Nominations**: DAC'14, ASPDAC'13, DAC'12, ISPD'12, ICCAD'11, DAC'11, ISPD'10, ICCAD'08, ASPDAC'08, DAC'06, ASPDAC'06

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:

Fellow, IEEE (Institute of Electrical and Electronics Engineers), class of 2014
Fellow, SPIE (International Society for Optical Engineering), class of 2017
Member, ACM (Association for Computing Machinery) and ACM/SIGDA

UNIVERSITY COMMITTEE ASSIGNMENTS:

Departmental-	Member, ECE Faculty Search Committee	2012-present
	Member, ECE Faculty Peer Review Committee	2013-present
	Member, ECE Faculty Awards Committee	2014-present
	Member, ECE Department Colloquium Committee	2011-present
	Member, ECE Benchmarking/Directions Committee	2014-present
	Coordinator, ECE Department, Integrated Circuits & Systems Area Graduate Admissions Committee	2009-present
	Member, ECE Department, Integrated Circuits & Systems Area Graduate Admissions Committee	2005-present
	Member, Integrated Circuits & Systems Curriculum Committee	2005-present
	Member, Computer Science Department, Graduate Studies Committee	2004-present
	Co-founder/Co-organizer, VLSI Seminar Series (renamed to Integrated Circuits & Systems Seminar Series in Spring 2010)	2003-present
	Member, ECE Department, Computer Engineering Graduate Admissions Committee	2003-present
	Member, Computer Engineering Curriculum Committee	2003-present
	Member, ECE Department, Graduate Studies Committee	2003-present
	Member, Undergraduate Student Appeals Committee	2003-present
	Member, ECE Department Faculty Review Committee	2010
University-	Faculty Co-Chair, Asian/Asian American Faculty and Staff Association (AAAFSA), UT Austin	2012-2014

	AAAFSA RAISE Award Committee	2015
	Heman Sweatt Nominations Committee	2013, 2014
	Faculty Mentor Program	2005-present
	AAAFSA Undergraduate Scholarship Committee	2013, 2014
	Graduate School Outstanding Dissertation Selection Committee	2011

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES:

Editorship

- Associate Editor, IEEE Design & Test, 2016-
- Senior Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2014 -
- Associate Editor, IET Computers & Digital Techniques, 2014-present
- Associate Editor, Science China Information Sciences, 2013-present
- Subject Area Editor (in VLSI Design), Journal of Computer Science and Technology (JCST), 2010-present
- Associate Editor, IEEE Circuits and Systems Society (CASS) Newsletters, 2007-present
- Associate Editor, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2007-2014
- Associate Editor, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), 2006-2011
- Associate Editor, IEEE Transactions on Circuits and Systems, I: Regular Papers (TCAS-I), 2008-2009
- Guest Editor, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Special Section of International Symposium on Physical Design, 2007 and 2008
- Associate Editor, IEEE Transactions on Circuits and Systems, II: Express Briefs (TCAS-II), 2006-2007

Service to Professional Society and Government/Agencies

- IEEE Council on Electronic Design Automation (CEDA), Distinguished Lecturer Program Committee, 2016-present
- ACM/SIGDA Outstanding New Faculty Award Committee, 2017
- ACM/TODAES Best Paper Award Committee, 2016, 2017
- ACM/SIGDA Outstanding PhD Dissertation Award Committee, 2014
- Advisor Board, Chinese American Semiconductor Professional Association (华美半导体协会), Austin Chapter, 2013 -
- IEEE Council on Electronic Design Automation (CEDA), Publicity Committee, 2012-present
- IEEE Admission & Advancement Committee Senior Member Review Panel, Feb. 2013
- ACM/SIGDA Technical Committee on Physical Design, Chair, 2009-present
- Semiconductor Industry Association, International Technology Roadmap for Semiconductors (ITRS), Design Technology Working Group, 2004-present
- ACM/SIGDA Outstanding PhD Dissertation Award Committee, 2012
- IEEE Computer-Aided Network Design (CANDE) Committee: Past Chair, 2010; Chair, 2009; Secretary, 2008
- IEEE Council on EDA (CEDA) Working Group for Educational Certification Program in China, 2007
- IEEE Guillemin-Cauer and Darlington Best Paper Awards Nomination Committee, 2007
- IEEE TCAS-II EDICS Committee, 2006
- NYSTAR (New York State) Microelectronics Design Center (MDC) Industrial Liaison, 2002-2003

- Semiconductor Research Corporation (SRC) Industrial Liaison, 2001-2003

Services to Professional Conferences

Various Chair/Leadership/Advisory Positions

- General Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019
- Program Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2018
- Vice Program Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2017
- Technical Program Chair, ACM/IEEE Asia and South Pacific Design Automation Conference (ASPDAC), 2017
- Executive Committee Member and Special Session/Tutorial Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016
- International Advisory Committee Co-Chair, IEEE International Conference on Ubiquitous Wireless Broadband (ICUWB), Oct. 16-19, 2016
- Subcommittee Chair for "Physical Verification, Lithography and DFM", Design Automation Conference (DAC), 2016
- Steering Committee Member, ACM International Symposium on Physical Design (ISPD), 2016
- Technical Program Committee Vice Chair, ACM/IEEE Asia and South Pacific Design Automation Conference (ASPDAC), 2016
- Executive Committee Member and Workshop Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2015
- Executive Committee Member and Tutorial Chair, ACM/IEEE Design Automation Conference (DAC), 2014
- Organizing Committee Chair, IEEE Texas Workshop on Integrated Systems Exploration (TexasWISE), 2014
- Co-Chair, IEEE/ACM Workshop on Variability Modeling and Characterization (VMC), 2013, 2014 (co-located with ICCAD)
- Co-Chair, NSF/SRC/DFG Cross Domain Resilience Workshop, Austin, July 11-12, 2013
- Technical Program Co-Chair, the 1st IEEE International High Speed Interconnect Symposium (From Silicon to Systems), Dallas, April 30, 2013
- Organizing Committee, the 1st IEEE Texas Workshop on Integrated Systems Exploration (TexasWISE), 2013
- Conference Co-Chair, the 13th International CAD/Graphics Conference, 2013
- EDA Track Co-Chair, 31st IEEE International Conference on Computer Design (ICCD), 2013
- ASPDAC 10-Year Retrospective Most Influential Paper Award Committee Member, 2013
- Technical Advisory Board Member, International System-on-Chip (SoC) Conference & Exhibit, 2007-present
- Design for Manufacturability Track Chair, International Conference on Computer Aided Design (ICCAD), 2012
- CAD and Design Tools Track Chair, International Symposium on Low Power Electronics & Design (ISLPED), 2012, 2013, 2014
- Design for Manufacturability Subcommittee Chair, Design Automation Conference (DAC), 2012
- DFM and Statistical Design, Subcommittee Chair, Asian and South Pacific Design Automation Conference (ASPDAC), 2012, 2013
- EDA Subcommittee Chair, International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2010, 2011, 2012, 2013, 2014
- EDA Subcommittee Co-Chair, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2012, 2013, 2014

- Award Chair, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2009-2012
- Biological, Nanoscale and Post-CMOS Systems, Subcommittee Chair, International Conference on Computer-Aided Design (ICCAD), 2011
- Physical Design & Manufacturability Subcommittee Chair, Design Automation Conference (DAC), 2011
- Physical Design Track Chair, Asian and South Pacific Design Automation Conference (ASPDAC), 2011
- Exhibits Chair, International Symposium on Low Power Electronics & Design (ISLPED), 2010
- Best Paper Award Committee Member, IEEE/ACM International Symposium on Networks-on-Chip (NOCS), 2009
- Steering Committee Chair, ACM International Symposium on Physical Design (ISPD), 2009
- DFM Track Chair, Asian and South Pacific Design Automation Conference (ASPDAC), 2009
- General Co-Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2009
- Chair for Electronic Design Automation (EDA) track, First Asian Symposium on Quality Electronic Design (ASQED), 2009
- General Chair, ACM International Symposium on Physical Design (ISPD), 2008
- Program Co-Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2008
- Publication Chair, SLIP Workshop, 2008
- Co-Chair for Design of Reliable Circuits and Systems (DFR) track, International Symposium on Quality Electronic Design (ISQED), 2007 and 2008
- Local Arrangement Chair/Steering Committee Member, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2007
- Program Chair, ACM International Symposium on Physical Design (ISPD), 2007
- IEEE CANDE Workshop Chair, 2007
- CAD track Co-Chair, International Symposium on Circuits and Systems (ISCAS), 2006, 2007
- Invited Speakers/Panel Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2006, 2007
- Publication Chair, ACM International Symposium on Physical Design (ISPD), 2006
- Publicity Chair, ACM International Symposium on Physical Design (ISPD), 2005
- Publicity Co-Chair, SLIP Workshop, 2003
- Local Arrangement Chair, Great Lakes Symposium on VLSI (GLSVLSI), 2002
- Session Chair for DAC, ICCAD, ISPD, ASPDAC, ISQED, SLIP, ICICDT, ICSICT, etc.

Program Committee Member

- SPIE Advanced Lithography Symposium – DFM Conference Committee, 2012-present
- SPIE Photonics West – Optoelectronic Interconnect XII Conference Committee, 2012
- ACM International Symposium on Low Power Electronics & Design (ISLPED), 2011-present
- IEEE International Conference on Computer Design (ICCD), 2011-present
- ACM/SIGDA Student Research Competition at ICCAD 2013, 2014
- ACM/IEEE Design Automation Conference (DAC), 2009-2012
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2003-2005, 2009-2012
- ACM/IEEE Asian and South Pacific Design Automation Conference (ASPDAC), 2003-2005, 2007, 2009-2013, 2015
- IEEE International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2008-present
- IEEE International Workshop on Design for Manufacturability & Yield (DFM&Y), 2007-present
- IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2005-present
- ACM International Workshop on System Level Interconnect Prediction (SLIP), 2003-2011
- SASIMI Workshop, 2009-2010
- IEEE International Symposium on Quality Electronic Design (ISQED), 2006-2009
- Austin Conference on Integrated Systems and Circuits (ACISC), 2006-2008

- International Semiconductor Technology Conference, 2008
- IEEE/ACM International Conference on VLSI Design (VLSID), 2008
- IEEE/ACM Design, Automation and Test in Europe (DATE), 2006, 2007
- International Symposium on Circuits and Systems (ISCAS), 2004-2007
- ACM International Symposium on Physical Design (ISPD), 2004-2007
- ACM Great Lakes Symposium on VLSI (GLSVLSI), 2002-2006

Proposal Review Panels

- National Science Foundation (NSF) Panelist
- External reviewer for California MICRO Program
- External reviewer for Louisiana Board of Regents
- External reviewer for University of Missouri Research Board
- External reviewer for Austrian Science Fund (FWF)
- External reviewer for Research Grants Council, Hong Kong
- External reviewer for Qatar National Research Fund

PUBLICATIONS:

Google citation page http://scholar.google.com/citations?user=3aLIroEAAAAJ
Citations 6447, h-index 45, i-10 index 145, as of May 4, 2017

A. Refereed Journal Articles

[J1] Taehee Lee, David Z. Pan, and Joon-Sung Yang, "Clock Network Optimization with Multi-bit Flip-flop Generation Considering Multi-corner Multi-mode Timing Constraint," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J2] Derong Liu, Bei Yu, Salim Chowdhury, and David Z. Pan, "Incremental Layer Assignment for Timing Optimization," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2017 (accepted)

[J3] Yibo Lin, Bei Yu, Yi Zou, Zhuo Li, Charles J. Alpert, and David Z. Pan**, "**Stitch Aware Detailed Placement for Multiple E-Beam Lithography," *Integration, the VLSI Journal*, 2017 (accepted)

[J4] Derong Liu, Bei Yu, Salim Chowdhury, and David Z. Pan, "TILA-S: Timing-Driven Incremental Layer Assignment Avoiding Slew Violations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J5] Xiaoqing Xu, Yibo Lin, Meng Li, Jiaojiao Ou, Brian Cline, and David Z. Pan, "Redundant Local-Loop Insertion for Unidirectional Routing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J6] Yibo Lin, Bei Yu, Biying Xu, and David Z. Pan, "Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J7] Yibo Lin, Bei Yu, and David Z. Pan, "High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J8] Vinicius Livramento, Derong Liu, Salim Chowdhury, Bei Yu, Xiaoqing Xu, David Z. Pan, Jos´e Lu´ıs G¨untzel, and Luiz C. V. dos Santos, "Incremental Layer Assignment Driven by an External Signoff Timing Engine," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J9] Xiaoqing Xu and David Z. Pan, "Toward Unidirectional Routing Closure in Advanced Technology Nodes," *IPSJ Transactions on System LSI Design Methodology*, Vol.10, pp. 1–12, Apr. 2017 **(Invited Paper)**

[J10] Tetsuaki Matsunawa, Bei Yu, and David Z Pan, "Laplacian Eigenmaps and Bayesian Clustering Based Layout Pattern Sampling and Its Applications to Hotspot Detection and OPC," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, 2017

[J11] Jun Zhang, Yu-Feng Guo, David Z. Pan, and Ke-Meng Yang, "A Novel 3-D Analytical Method for Curvature Effect-Induced Electric Field Crowding in SOI Lateral Power Device," *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 4359 - 4365, Nov. 2016

[J12] Subhendu Roy, Derong Liu, Jagmohan Singh, Junhyung Um, and David. Z. Pan, "OSFA: A New Paradigm of Aging Aware Gate-Sizing for Power/Performance Optimizations under Multiple Operating Conditions," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 10, pp. 1618-1629, Oct. 2016. Available at http://dx.doi.org/10.1109/TCAD.2016.2523439

[J13] Yunfeng Yang, Wai-Shing Luk, David Z. Pan, Hai Zhou, Changhao Yan, Dian Zhou, and Xuan Zeng, "Layout Decomposition Co-optimization for Hybrid E-Beam and Multiple Patterning Lithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 9., September 2016. Available at http://dx.doi.org/10.1109/TCAD.2015.2512903

[J14] Xiaoqing Xu, Bei Yu, Jhih-Rong Gao, Che-Lun Hsu and David Z. Pan, "PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 21, no. 3, July 2016, Available at http://dx.doi.org/10.1145/2842612

[J15] Bei Yu, Xiaoqing Xu, Subhendu Roy, Yibo Lin, Jiaojiao Ou, and David Z. Pan, "Design for Manufacturability and Reliability in Extreme-Scaling VLSI," *Science China Information Sciences (SCIS),* vol.59, June, 061406:2, 2016. (**Invited Paper**)

[J16] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu and David Z. Pan, "A Systematic Framework for Evaluating Standard Cell Middle-Of-Line (MOL) Robustness for Multiple Patterning Lithography," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, vol. 15, no. 2, 021202, 2016. Available at http://dx.doi.org/10.1117/1.JMM.15.2.021202

[J17] Tetsuaki Matsunawa, Bei Yu, and David Z Pan, "Optical Proximity Correction with Hierarchical Bayes Model," *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, vol. 15, no. 2, 021009, 2016. Available at http://dx.doi.org/10.1117/1.JMM.15.2.021009

[J18] Subhendu Roy, Mihir Choudhury, Ruchir Puri, and David Z. Pan, "Polynomial Time Algorithm for Area and Power Efficient Adder Synthesis in High-Performance Designs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 5, pp. 820-831, May 2016. Available at http://dx.doi.org/10.1109/TCAD.2015.2481794

[J19] Ye Zhang, Wai-Shing Luk, Yunfeng Yang, Hai Zhou, Changhao Yan, David Z. Pan, and Xuan Zeng, "Layout Decomposition with Pairwise Coloring and Adaptive Multi-Start for Triple Patterning Lithography," *ACM Transactions on Design Automation of Electronic Systems*, vol. 21, no. 1, Nov. 2015, Available at http://dx.doi.org/10.1145/2764904

[J20] Jiaojiao Ou, Bei Yu, Jhih-Rong Gao, Moshe Preil, Azat Latypov, and David Z Pan, "Directed Self-Assembly (DSA) Cut Mask Assignment for Unidirectional Design," *The Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 14, no. 3, 031211, Aug., 2015, Available at http://dx.doi.org/10.1117/1.JMM.14.3.031211

[J21] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Yibo Lin, Zhuo Li, Charles Alpert, and David Z. Pan, "Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 5, pp. 726 – 739, May 2015. Available at http://dx.doi.org/10.1109/TCAD.2015.2401571

[J22] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu, and David Z. Pan, "Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 5, pp. 699-712 May 2015. Available at http://dx.doi.org/10.1109/TCAD.2015.2399439

[J23] Subhendu Roy, Pavlos M. Mattheakis, Laurent Masse-Navette, and David Z. Pan, "Clock Tree Resynthesis for Multi-corner Multi-mode Timing Closure," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 4, pp. 589-602, April 2015. Available at http://dx.doi.org/10.1109/TCAD.2015.2394310

[J24] Bei Yu, Kun Yuan, Duo Ding, and David Z. Pan, "Layout Decomposition for Triple Patterning Lithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 3, pp. 433 – 446, March 2015. Available at http://dx.doi.org/10.1109/TCAD.2014.2387840

[J25] Yongchan Ban and David Z. Pan, "Self-Aligned Double Patterning Layout Decomposition for 2D Random Metals for Sub-10nm Node Design," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 14, no. 1, pp. 011004, Jan-Mar 2015. Available at http://dx.doi.org/10.1117/1.JMM.14.1.011004

[J26] Bei Yu, Jhih-Rong Gao, Duo Ding, Xuan Zeng, and David Z. Pan, "Accurate Lithography Hotspot Detection based on Principal Component Analysis-Support Vector Machine Classifier with Hierarchical Data Clustering," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 14, no. 1, pp. 011003, Jan-Mar 2015. Available at http://dx.doi.org/10.1117/1.JMM.14.1.011003

[J27] Bei Yu, Subhendu Roy, Jhih-Rong Gao, and David Z. Pan, "Triple Patterning Lithography Layout Decomposition Using End-cutting," *SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3)*, vol. 14, no. 1, pp. 011002, Jan-Mar 2015. Available at http://dx.doi.org/10.1117/1.JMM.14.1.011002

[J28] Jiwoo Pak, Sung Kyu Lim, and David Z. Pan, "Electromigration Study for Multi-scale Power/Ground Vias in TSV-based 3D ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no. 12, Dec. 2014. Available at http://dx.doi.org/10.1109/TCAD.2014.2360456

[J29] Subhendu Roy, Mihir Choudhury, Ruchir Puri, and David Z. Pan, "Toward Optimal Performance-Area Trade-Off in Adders by Synthesis of Parallel Prefix Structures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 33, no. 10, pp. 1517—1530, Oct. 2014. Available at http://dx.doi.org/10.1109/TCAD.2014.2341926

[J30] Moongon Jung, Joydeep Mitra, David Z. Pan, and Sung Kyu Lim, "Full-Chip Mechanical Reliability Analysis and Optimization for 3D ICs," *Communications of the ACM* (**Research Highlights**), Vol. 57, No. 1, pp. 107-115, Jan. 2014. Available at http://dx.doi.org/10.1145/2494536

[J31] Runsheng Wang, Xiaobo Jiang, Tao Yu, Jiewen Fan, Jiang Chen, David Z. Pan, and Ru Huang, "Investigations on Line-Edge Roughness (LER) and Line-Width Roughness (LWR) in Nanoscale CMOS Technology: Part II – Experimental Results and Impacts on Device Variability," *IEEE Transactions on Electron Devices*, vol. 60, no. 11, pp. 3676-3682, Nov. 2013. Available at http://dx.doi.org/10.1109/TED.2013.2283517

[J32] Moongon Jung, David Z. Pan, and Sung Kyu Lim, "Chip/Package Mechanical Stress Impact on 3D IC Reliability and Mobility Variations," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 11, Nov. 2013. Available at http://dx.doi.org/10.1109/TCAD.2013.2265372

[J33] David Z. Pan, Bei Yu, and Jhih-Rong Gao, "Design for Manufacturing with Emerging Nanolithography," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 32, no. 10, pp. 1453 – 1472, Oct. 2013. (**Keynote Paper**) Available at: http://dx.doi.org/10.1109/TCAD.2013.2276751

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[C3] Xiaoqing Xu, Yibo Lin, Vinicius Livramento, and David Z. Pan, "Concurrent Pin Access Optimization for Unidirectional Routing," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, Jun. 18-22, 2017.

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[C5] Travis Meade, Zheng Zhao, Shaojie Zhang, David Z. Pan, and Yier Jin**, "**Revisit Sequential Logic Obfuscation: Attacks and Defenses," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, USA, May 28-31, 2017 **(Invited Paper)**

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[C26] Yibo Lin, Xiaoqing Xu, Bei Yu, Ross Baldick, and David Z. Pan, "Triple/Quadruple Patterning Layout Decomposition via Novel Linear Programming and Iterative Rounding," *Proc. SPIE 9781, Design-Process-Technology Co-optimization for Manufacturability X*, San Jose, CA, Feb. 21-25, 2016 (**Franco Cerrina Memorial Best Student Paper Award)**

[C27] Xiaoqing Xu, Brian Cline, Greg Yeric, and David Z. Pan, "Standard Cell Pin Access and Physical Design in Advanced Lithography," *SPIE Advanced Lithography Conference*, San Jose, CA, Feb. 21-25, 2016 **(Invited Paper)**

[C28] Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, and David Z. Pan, "Hybrid Hotspot Detection using Regression Model and SOCS Kernels," *Proc. SPIE 9781, Design-Process-Technology Co-optimization for Manufacturability X*, San Jose, CA, Feb. 21-25, 2016

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[C32] Andrew B. Kahng, Mulong Luo, Gi-Joon Nam, Siddhartha Nath, David Z. Pan, and Gabriel Robins, "Toward Metrics of Design Automation Research Impact," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015. (**Invited Paper**)

[C33] Bei Yu, Derong Liu, Salim Chowdhury, and David Z. Pan, "TILA: Timing-Driven Incremental Layer Assignment," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015.

[C34] Yibo Lin, Bei Yu, Biying Xu, and David Z. Pan, "Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015.

[C35] Chen-Hsuan Lin, Subhendu Roy, Chun-Yao Wang, David Z. Pan, and Deming Chen, "CSL: Coordinated and Scalable Logic Synthesis Techniques for Effective NBTI Reduction," *IEEE International Conference on Computer Design (ICCD)*, Oct. 18-21, 2015

[C36] David Z. Pan, Lars Liebmann, Bei Yu, Xiaoqing Xu, Yibo Lin, "Pushing Multiple Patterning in Sub-10nm: Are We Ready?" *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015 (**Invited Paper**)

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[C39] Subhendu Roy, Derong Liu, Junhyung Um, and David Z. Pan, "OSFA: A New Paradigm of Gate Sizing for Power/Performance Optimizations under Multiple Operating Conditions," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015

[C40] Keith Campbell, Pranay Vissa, David Z. Pan, and Deming Chen, "High-Level Synthesis of Error Detecting Cores through Low-Cost Modulo-3 Shadow Datapaths," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015

[C41] Wei Ye, Bei Yu, Yong-Chan Ban, Lars Liebmann, and David Z. Pan, "Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line," *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Pittsburgh, PA, May 20-22, 2015

[C42] Jiaojiao Ou, Bei Yu, Jhih-Rong Gao, Moshe Preil, Azat Latypov, and David Z Pan, "Directed Self-Assembly Based Cut Mask Optimization for Unidirectional Design," *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Pittsburgh, PA, May 20-22, 2015

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C. Other Refereed Conference/Workshop Papers/Posters (without proceeding) (Partial List)

[W1] Xiaoqing Xu, Bei Yu, Jhih-Rong Gao, Che-Lun Hsu, and David Z. Pan, "PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning," *SRC Techcon Conference*, Austin, TX, September 2015. **(Best Paper in Session Award)**

[W2] Tetsuaki Matsunawa, Jhih-Rong Gao, Bei Yu, and David Z. Pan, "Machine Learning Based High-Accurate Hotspot Detection with Boosting Algorithm," *ACM/IEEE Design Automation Conference (DAC)* Designer Track, 2014 (**Best Designer Track Finalist**)

[W3] Jiwoo Pak, Mohit Pathak, Sung Kyu Lim, David Z. Pan, "Modeling and Prediction of Chip-Level Electromigration for TSV-Based 3D ICs," *SRC Techcon Conference*, Austin, TX, September 2012. **(Best Paper in Session Award)**

[W4] Yen-Hung Lin, Bei Yu, David Z. Pan, and Yih-Lang Li, "TRIAD: Triple Patterning Lithography Aware Detailed Router," *the 6th IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y)*, June 4, 2012

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[W6] T. Luo, D. Newmark, and David Z. Pan, "Effective Power Optimization combining Placement, Sizing and Multi-Vt techniques," *SRC Techcon Conference*, Austin, TX, September 2007. **(Best Paper in Session Award)**

[W7] P. Yu and David Z. Pan, "TIP-OPC: A New Topological Invariant Paradigm for Pixel Based Optical Proximity Correction," *Proceedings SRC Techcon Conference*, Austin, TX, September 2007.

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[W10] C.-C. Chang, J. Cong, David Z. Pan, and X. Yuan, "Interconnect-Driven Floorplanning with Fast Global Wiring Planning and Optimization," *Proceedings SRC Techcon Conference*, Phoenix, AZ, September 2000.

[W11] J. Cong, David Z. Pan, and P.V. Srinivas, "Improved Crosstalk Modeling with Applications to Noise Constrained Interconnect Optimization," *Proceedings SRC Techcon Conference*, Phoenix, AZ, September 2000.

[W12] J. Cong and David Z. Pan, "Interconnect Delay and Area Estimation for Multiple-Pin Nets," *Proceedings ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Monterey, CA, March 1999.

[W13] J. Cong and David Z. Pan, "Interconnect Delay Estimation Models for Logic and High Level Synthesis," *SRC Techcon Conference*, Las Vegas, NV, September 1998. **(Best Paper in Session Award)**

[W14] J. Cong and David Z. Pan, "Interconnect Performance Estimation Models for Synthesis and Design Planning," *ACM/IEEE International Workshop on Logic Synthesis*, Lake Tahoe, CA, June 1998.

D. Books/Book Chapters and Dissertation

[B1] Bei Yu and David Z. Pan, *Design for Manufacturability with Advanced Lithography*, Springer, 2016

[B2] Bei Yu and David Z. Pan, "Layout Decomposition for Triple Patterning," in Encyclopedia of Algorithms, M.-Y. Kao eds., Springer, 2015

[B3] Minsik Cho and David Z. Pan, "Global Routing," in Encyclopedia of Algorithms, M.-Y. Kao eds., Springer, 2015

[B4] M. Cho, J. Mitra, and David Z. Pan, "Manufacturability Aware Routing" in *The Handbook of Algorithms for VLSI Physical Design Automation* (edited by Charles J. Alpert, Dinesh P. Mehta, and Sachin S. Sapatnekar), CRC Press, 2009. (Invited book chapter)

[B5] David Z. Pan, B. Halpin, and H. Ren, "Timing-Driven Placement" in *The Handbook of Algorithms for VLSI Physical Design Automation* (edited by Charles J. Alpert, Dinesh P. Mehta, and Sachin S. Sapatnekar), CRC Press, 2009. (Invited book chapter)

[B6] T. Luo and David Z. Pan, "DPlace: Anchor Cell based Quadratic Placement with Linear Objective" in *Modern Circuit Placement: Best Practices and Results* (edited by Jason Cong and Gi-Joon Nam), Springer, 2007. (Invited book chapter)

[B7] David Z. Pan and M. Stan, "Physical Design and Interaction with Technology" in *CAD Algorithms, Methods and Tools for Low-Power Circuits and Systems* (edited by Enrico Macii), IEEE Technology Survey, 2006

[B8] Zhigang Pan, *Interconnect Synthesis and Planning for High-Performance IC Designs*, PhD Dissertation, University of California at Los Angeles, 2000

PATENTS:

[P1] David Zhigang Pan and Peng Yu, "Method and System for Performing Optical Proximity Correction with Process Variations Considerations." US Patent, No. 7,711,504, Granted May 4, 2010.

[P2] Minsik Cho and David Zhigang Pan, "Method and System for Performing Global Routing on an Integrated Circuit Design." US Patent, No. 7,661,085, Granted on February 9, 2010.

[P3] Anthony Correale, Jr., David S. Kung, Douglas T. Lamb, David Zhigang Pan, Ruchir Puri, and David Wallach, "Multiple Voltage Integrated Circuit and Design Method Therefore." US Patent, No. 7,480,883, Granted on January 20, 2009.

[P4] Anthony Correale, Jr., Rajeev Joshi, David S. Kung, David Zhigang Pan, and Ruchir Puri, "Single Supply Level Converter." US Patent, No. 7,119,578, Granted on October 10, 2006.

[P5] Anthony Correale, Jr., David S. Kung, Douglas T. Lamb, David Zhigang Pan, Ruchir Puri, and David Wallach, "Multiple Voltage Integrated Circuit and Design Method Therefor." US Patent, No. 7,111,266, Granted on September 19, 2006.

[P6] Anthony Correale, Jr., David S. Kung, David Zhigang Pan, and Ruchir Puri, "Method and Program Product of Level Converter Optimization." U.S. Patent, No. 7,089,510, Granted on August 8, 2006.

[P7] Jingsheng Cong, David Zhigang Pan, and P.V. Srinivas, "Method and Apparatus for Calculation of Crosstalk Noise in Integrated Circuits." U.S. Patent, No. 7,013,253, Granted March 2006.

[P8] Jingsheng Cong and David Zhigang Pan, "Wire Width Planning and Performance Optimization for VLSI Interconnects." U.S. Patent No. 6,408,427, Granted June 2002.

ORAL PRESENTATIONS:

Invited Tutorials/Talks, Special Sessions, Panels at Conferences/Workshops

[O1] "Bridging Design and Technology Gap for Manufacturability, Reliability, and Security," The First ShanghaiTech Workshop on Emerging Devices, Circuits and Systems (SWEDCS), June 30, 2016

[O2] **Panelist, "**TSVs ARE SO 2010 - THE REALITY OF 3D-IC," ACM/IEEE Design Automation Conference, Austin, TX, June 6-9, 2016

[O3] **Visionary Talk,** "DFX: on Deep Nanoscale Design for Manufacturability, Reliability, and Security," *IEEE International Workshop on Design Automation for Cyber-Physical System*s (co-located with DAC), Austin, TX, June 5, 2016 http://www.ieee-cps.org/CPSDA-2016/program.html

[O4] **Keynote**, "Nanolithography and Design Technology Co-optimization in Extreme Scaling," China S*emiconductor Technology International Conference (CSTIC) - Symposium II and Symposium XI-DTCO Joint session*, Shanghai, March 13-14, 2016

[O5] Invited talk, "Standard Cell Pin Access and Physical Design in Advanced Lithography," *SPIE Advanced Lithography Conference*, San Jose, CA, Feb. 21-25, 2016

[O6] Panelist -- "From EDA to DA: Can we evolve beyond our E-roots?" ICCAD, Austin, Nov. 2-6, 2015

[O7] "Toward Cross-Layer Technology, EDA and System Power/Performance/Reliability Optimizations," Samsung Low Power Forum, Austin, TX, Oct. 8, 2015
[O8] "Cross-Layer Reliability in Extreme Scaling & Beyond," Reliability and Design (ZuE) Workshop, Siegen, Germany, September 21-23, 2015
[O9] "Pushing Multiple Patterning in Sub-10nm: Are We Ready?" *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, June 11, 2015. (**Special Session)**
[O10] "Technology, EDA and System Power/Performance/Reliability Optimization with a Cross-Layer Case Study," DAC 2015 SEAK Workshop, June 7, 2015
[O11] "Design for Manufacturing in Extreme Scaling and Beyond," edaWorkshop, Dresden, May 21, 2015
[O12] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," CSTIC, March 16, 2015
[O13] "Machine Learning and Pattern Matching in Physical Design," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Japan, Jan. 19-22, 2015 (**Special Session**)
[O14] IEEE CEDA All Japan Joint Chapter, "My Take on ASP-DAC on its 20th Anniversary," ASP-DAC 2015
[O15] **Keynote**, "CAD Tool and Methodology for Reliable 3D-IC Integration," TwinLab 3DSC Workshop, 11/11/2014
[O16] Invited talk, "Evolving Challenges and Techniques for Nanometer SoC Clock Network Synthesis," IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Oct. 28-31, 2014, Guilin, China
[O17] Invited talk, "Manufacturable and Reliable Interconnect in Extreme Scaling," IEEE SLIP Workshop, June 1, 2014
[O18] Invited talk, "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," *China Semiconductor Technology International Conference (CSTIC)*, Shanghai, March 16, 2014
[O19] **Opening Plenary**, "Mathematical Methods in Nanometer Design for Manufacturability," *International Workshop on Mathematical Methods in Chip Design Automation*, Fuzhou, March 14-16, 2014
[O20] Invited talk, "Bridging the Gap from Mask to Physical Design for Multiple Patterning Lithography," *SPIE International Symposium on Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability VIII*, San Jose, CA, Feb. 23-27, 2014
[O21] 2013 BIMS 北京微电子国际研讨会特邀讲员，"未来集成电路的智能设计与制造," Beijing, China, Oct. 31, 2013
[O22] Invited talk, "Lithography Hotspot Detection and Mitigation in Nanometer VLSI," 2013 *IEEE ASICON*, Shenzhen, China, Oct. 29, 2013
[O23] SRC e-Workshop, "CAD Tool and Methodology for Reliable 3D-IC Integration" (jointly presented with Prof. Sung Kyu Lim at Georgia Tech), July 18, 2013
[O24] Invited talk, "VLSI Design and Nanolithography in 14nm and Beyond", 2013 *CMOS Emerging Technologies Research Symposium*, Whistler, Canada, July 17, 2013
[O25] Invited talk, "Cross-Layer Robustness in Extreme Scaling", The first NSF/SRC/DFG International Workshop on Cross-Layer Resilience, Austin, July 11 and 12, 2013
[O26] **Keynote**, "Cross-Layer Resilient Design for Extreme Scaling and Beyond", ACM/IEEE International Workshop on Logic and Synthesis (IWLS), Austin, TX, June 7, 2013
[O27] Roundtable Panelist in "Who Will Pay for Low Power – Chip Manufacturers, Tool Providers or Consumers?" hosted by Ed Sperling of Low Power Engineering, held during DAC, June 5, Austin, TX, 2013
[O28] Invited talk, "Design for Manufacturability and Reliability in TSV-based 3D-IC", ACM/IEEE DFM&Y Workshop, Austin, TX, June 3, 2013
[O29] "CAD in Extreme Scaling and Emerging Technologies", NSF/CCC/SIGDA Workshop, Austin, TX, June 2, 2013
[O30] "Modeling and Layout Optimization for Robust 3D-IC Integration with TSVs", the 1st IEEE International High Speed Interconnect Symposium (From Silicon to Systems), Dallas, April 30, 2013
[O31] "Dealing with IC Manufacturability in Extreme Scaling", ICCAD Embedded Tutorial, Nov. 2012
[O32] "Lithography Aware Physical Design," 2012 Lithography Workshop, Williamsburg, VA, June 2012

[O33] "Reliability Modeling and Design Issues for TSV-based 3D Integration," *4th Design for 3D Silicon Integration Workshop (D43D)*, Lausanne, Switzerland, June 25, 2012
[O34] Panelist on "Future Interconnect Technologies," SLIP 2012, co-located with DAC'12 in San Francisco, CA, June 2012
[O35] Special Session talk on "VLSI CAD for Emerging Nanolithography," VLSI-DAT, Hsinchu, Taiwan, April 2012
[O36] "Design for Manufacturability with Emerging Nanolithography," ASPDAC 2012 Tutorial, Sydney, Australia, January 2012
[O37] Special Session talk on "Physical CAD for Robust Designs," ASPDAC 2012, Sydney, Australia, January 2012
[O38] Special Session talk on "Design for Manufacturability & Reliability for TSV-based 3D-ICs," ASPDAC 2012, Sydney, Australia, January 2012
[O39] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and 3D-IC," Global COE Workshop on "Ambient SoC Education and Research for New Leaders," co-located with ASP-DAC 2012, Sydney, Australia, January 30, 2012 (Invited talk)
[O40] "Robust and Energy Efficient Design-Process Integration in Sub-22nm CMOS and 3D-IC," Pacific Rim Outlook Forum for IC Technology (PROFIT) Workshop, Inner Mongolia, China, August 2011
[O41] "'More Moore' and 'More than Moore', beyond 22nm: Challenges and Opportunities," The 11th Emerging Information & Technology Conference, Chicago, IL, July 28-29, 2011
[O42] "Reliability and Variability in TSV-based 3D-IC Designs," The 3rd Design for 3D Silicon Integration Workshop (D43D), Grenoble, France, June 2011
[O43] **Keynote Speaker,** "Nanolithography and Design-Technology Co-optimization Beyond 22nm," TAU Workshop, Santa Barbara, CA, March 2011
[O44] "Double Patterning Lithography Layout Decomposition and Routing," IEEE Lithography Workshop, Kauai, HI, November 2010
[O45] Invited Tutorial on "Design for Resilience in Beyond-22nm CMOS & 3D-IC," IEEE Dallas CAS Workshop, Dallas, TX, October 18, 2010
[O46] "Design for Manufacturability and Reliability in TSV-based 3D-IC," ASPDAC TPC Workshop, Seoul, Korea, September 11, 2010
[O47] "Voltage and Frequency Island Optimizations for Many-Core/ Networks-on-Chip Designs," the first International Conference on Green Circuits & Systems (ICGCS), Shanghai, China, June, 2010
[O48] "CAD for Double Patterning Lithography," IEEE ICICDT, Grenoble, France, June 3, 2010
[O49] "Layout Optimizations for Double Patterning Lithograph," IEEE ASICON, Changsha, China, October 23, 2009
[O50] "Nanometer & Emerging Design Automation Research at UTDA," ASPDAC TPC Workshop, Tokyo, Japan, September 7, 2009
[O51] "More Moore's Law through Computational Scaling - and EDA's Role," invited talk at the **NSF Workshop on the Future of Electronic Design Automation**, Washington DC, July 8, 2009
[O52] Organizer/Presenter, "Nanolithography and CAD Challenges for 32nm/22nm (and Beyond?)," half-day tutorial at ICCAD, San Jose, CA, November 12, 2008
[O53] Invited Talk, "EDA Education and Research at UT Austin," the first EDA Education & Research Workshop, held at ICCAD 2008, San Jose, CA, November 9, 2008
[O54] Invited Talk, "Lithography Friendly Routing: From Construct-by-Correction to Correct-by-Construction," ICSICT, Beijing, China, October 21, 2008
[O55] Invited Tutorial, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," SBCCI, Gramado, Brazil, September 1, 2008
[O56] Invited Talk, "Lithography Friendly Routing: From Construct-by-Correction to Correct-by-Construction," SBCCI, Gramado, Brazil, September 2, 2008
[O57] **Keynote Speaker**, "Design for Manufacturability – Practices and Perspectives for 45/32nm and Beyond," 2008 Freescale Physical Design and Design for Manufacturing (DFM) Conference, Austin, TX, May 13-16, 2008
[O58] Special Session Organizer/Presenter, "Tackling Manufacturability/Variability for 32nm and Below," *ASPDAC*, Seoul, Korea, January 2008
[O59] Tutorial Organizer/Presenter, "DFM Routing and Clock Distribution," *ICCAD*, San Jose, CA, November 2007

[O60] "Design and CAD for Manufacturability." *ACM/SIGDA Design Automation Summer School*, San Diego, CA, June 2-3, 2007 (held with IEEE/ACM Design Automation Conference)
[O61] "Nanometer Physical Design for Manufacturability and Variability," 3-hour Tutorial at the *VLSI-DAT* Conference, Taiwan, April 27, 2007
[O62] "DFM: Impact of Manufacturing Reality on Design," Half-day Tutorial at *ICCAD*, San Jose, CA, November 9, 2006
[O63] Panelist – "What Will Make or Break DFM&Y," *The First IEEE Design for Manufacturability & Yield Workshop (DFM&Y)*, San Jose, CA, October 26, 2006
[O64] Tutorial on "Lithography and Design for Variability," *Austin Conference on Integrated Systems and Circuits* (with Dr. Chris Mack), Austin, TX, May 18, 2006
[O65] Panelist – "Design for Manufacturability (DFM)," *SPIE Microlithography, Design and Process Integration Conference*, San Jose, CA, March 4, 2005
[O66] "Lithography and CMP Aware Routing," *IEEE Design for Manufacturability & Yield Workshop (DFM&Y)*, San Jose, CA, October 26, 2006
[O67] "Design for Manufacturability with Deep Sub-wavelength Lithography," *International Center on Design for Nanotechnology (IC-DFN) Workshop*, Hangzhou, China, August 16, 2006
[O68] "Manufacturability Aware Physical Layout Optimizations," *International Conference on IC Design and Technology (ICICDT)*, Austin, TX, May 2005
[O69] "Lithography Aware Physical Design," *IEEE International Conference on ASIC (ASICON)*, Shanghai, China, October 27, 2005
[O70] "Nanometer Physical Design Research at UT Austin," *International Center for System-on-Chip (IC-SOC) Workshop*, Changsha, China, August 6, 2004
[O71] "Diffusion-Based Placement Migration," *IEEE Electronic Design Process Symposium (EDPS)*, Monterey, CA, April 7, 2005
[O72] "Optimizing Power in Performance Constraints," *IEEE International Conference on Integrated Circuit Design and Technology (ICICDT)*, Austin, TX, May 19, 2004

Invited Talks at Various Institutions and Companies

[O73] **Distinguished Lecture,** "Bridging IC Design and Technology Gaps for Manufacturability, Reliability, and Security," Michigan Technological University, Oct. 7, 2016
[O74] **Distinguished Lecture,** "Bridging IC Design and Technology Gaps for Manufacturability, Reliability, and Security," Old Dominion University, Sept. 19, 2016
[O75] "Robust Standard Cell Design and Layout Regularity Study with Nanolithography," SRC eWorkshop, August 10, 2016
[O76] "Bridging Design and Technology Gaps for Manufacturability, Reliability, and Security," Univ. of Utah, June 16, 2016
[O77] "Design & Process Technology Co-optimizations in Extreme Scaling," NVIDIA, Austin, June 13, 2016
[O78] "Challenges and Opportunities of IC Design & Manufacturing in Extreme Scaling and Beyond," Anhui University, Hefei, China, May 17, 2016
[O79] "Challenges and Opportunities IC Design and Manufacturing in Deep Nano-Scaling and Beyond," Univ. of Science and Technology of China (USTC), Hefei, China, May 16, 2016
[O80] "Challenges and Opportunities of IC Design & Manufacturing in Extreme Scaling and Beyond," Hefei Univ. of Technology, May 16, 2016
[O81] "Challenges and Opportunities IC Design and Manufacturing in Extreme Scaling and Beyond," Jiangnan University, Wuxi, China, May 10, 2016
[O82] "Challenges and Opportunities of IC Design & Manufacturing in Extreme Scaling and Beyond," Tsinghua University (Institute of Microelectronics), May 5, 2016
[O83] "IC Design and Technology Co-Optimization and Exploration in Extreme Scaling and Beyond," Institute of Microelectronics, Chinese Academy of Science, May 3, 2016
[O84] "Machine Learning and Pattern Matching in VLSI-CAD Applications," Intel Strategic CAD Lab Online Seminar, April 19, 2016
[O85] "Standard Cell Pin Access and Physical Design in Advanced Lithography," Intel Corporation, Hillsboro, Oregon, April 8, 2016

[O86] "Lithography Hotspot Detection and Mask Synthesis in Extreme Scaling," Intel Corporation, Hillsboro, Oregon, April 8, 2016
[O87] "Machine Learning and Pattern Matching in VLSI CAD," Chongqing University, China, March 21, 2016
[O88] "Toward Cross-Layer Power/Performance/Reliability Optimizations," School of Microelectronics, Southeast University, Nanjing, China, March 17, 2016
[O89] "Machine Learning and Pattern Matching in VLSI CAD," School of Computer Science, Southeast University, Nanjing, China, March 17, 2016
[O90] "Toward Cross-Layer Power/Performance/Reliability Optimizations," School of Microelectronics, Fudan University, Shanghai, China, March 15, 2016
[O91] "纳米集成电路设计与制造的挑战、机遇与展望 Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," University of Macao, Jan. 28, 2016
[O92] "纳米集成电路设计与制造的挑战、机遇与展望 Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," SYSU-CMU Joint Institute of Engineering, Guangzhou, China, Jan. 22, 2016
[O93] "纳米集成电路设计与制造的挑战、机遇与展望 Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," PKU-Shenzhen, China, Jan. 21, 2016
[O94] "Machine Learning and Pattern Matching in VLSI CAD," City University of Hong Kong, Hong Kong, China, Jan. 18, 2016
[O95] "Machine Learning and Pattern Matching in VLSI CAD," Chinese University of Hong Kong, Hong Kong, China, Jan. 18, 2016
[O96] "Pushing Multiple Patterning and Hybrid Lithography in Extreme Scaling," IMEC, Leuven, Belgium, Oct. 5, 2015
[O97] "Nanometer IC Design and Manufacturing Closure in Extreme Scaling and Beyond," TU Eindhoven, Netherlands, Oct. 2, 2015
[O98] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," KIT, Karlsruhe, Germany, September 28, 2015
[O99] "Multiple Patterning & Physical Design in Extreme Scaling," Univ. of Bonn, Germany, September 24, 2015
[O100] "Design for Manufacturability and Reliability in Nanometer IC and Beyond," SMIC, Shanghai, September 2, 2015
[O101] "Pushing Multiple Patterning and Hybrid Lithography in Extreme Scaling," TSMC, Hsinchu, September 1, 2015
[O102] "Pushing Multiple Patterning and Hybrid Lithography in Sub-10nm: What's the Limit?" National Tsinghua University, Taiwan, September 1, 2015
[O103] "Technology, EDA and System Power/Performance/Reliability Optimization with a Cross-Layer Case Study," Cirrus Logic, Austin, TX, August 4, 2015
[O104] "Design for Reliability in Nanometer IC and Beyond," Infineon, Munich, Germany, July 17, 2015
[O105] "Design for Manufacturability/Reliability Research at UTDA," TU Vienna, Austria, June 23, 2015
[O106] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," TUM, Munich, Germany, June 2, 2015
[O107] "Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," Huazhong University of Science and Technology, March 24, 2015
[O108] "CAD Tool and Methodology for Reliable 3D-IC and Optical Integration," Wuhan University, March 23, 2015
[O109] "Nanometer IC Design, Manufacturing and Applications: Challenges, Opportunities, and Outlooks," Nanjing University of Science and Technology, March 18, 2015
[O110] "Standard Cell Pin Access and Cell Layout Co-Optimizations," Fudan University, March 16, 2015
[O111] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," CMU ECE Colloquium, Feb. 5, 2015
[O112] "Design for Reliability in Nanometer VLSI," Hisilicon, Jan. 16, 2016
[O113] "Cross-Layer Optimizations for Nanometer VLSI in Extreme Scaling and Beyond," Peking University, Jan. 15, 2015
[O114] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Tsinghua University, EE Dept., Jan. 14, 2015

[O115] "Machine Learning and Pattern Matching in VLSI Design and Verification," HK PolyU, Jan. 8, 2015
[O116] "Cross-Layer Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Chinese University of Hong Kong, Jan. 8, 2015
[O117] "Mask Synthesis and Physical Design for Nanolithography," GlobalFoundries, Dec. 12, 2014
[O118] "Mask Synthesis and Physical Design for Nanolithography," ASML, Nov. 6, 2014
[O119] "Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," Nanjing University of Posts & Telecommunications, Oct. 27, 2014
[O120] 'Design Techniques for Monolithic 3D Integration," IBM, Webinar, Oct. 3, 2014
[O121] "Mask and Physical Design Optimizations for Multiple Patterning Lithography," Samsung Electronics Future Technology Seminar, Seoul, S. Korea, Aug. 22, 2014
[O122] "Nanometer IC Design Challenges & Opportunities in Extreme Scaling and Beyond," LG Electronics, Seoul, S. Korea, Aug. 22, 2014
[O123] "Nanometer IC Design and Manufacturing in Extreme Scaling and Beyond," Shanghai Jiaotong University, Shanghai, China, July 23, 2014
[O124] "Nanometer IC Design and Technology Co-Optimization in Extreme Scaling and Beyond," University of Electronic Science and Technology in China (UESTC), Chengdu, China, July 15, 2014
[O125] "Nanometer IC Design and Manufacturing in Extreme Scaling and Beyond," Northwestern Polytechnic University, Xi'an, China, July 11, 2014
[O126] "Physical Design and Manufacturing Closure for 22nm/14nm IC and Beyond," Nanjing University of Posts & Telecommunications, July 10, 2014
[O127] Design for Manufacturability & Reliability in Extreme Scaling and Beyond, Southeast University, Nanjing, China, July 8, 2014
[O128] "Physical Design and Manufacturing Closure for 22nm/14nm IC and Beyond," Nanjing University of Science and Technology, July 8, 2014
[O129] "Reclaiming Over-the-IP-Block Routing Resources for Routability and Timing," IBM EDA Seminar, Austin, TX, June 10, 2014
[O130] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Harvard University, May 5, 2014
[O131] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," MIT, May 2, 2014
[O132] "Physical Design and Manufacturing Closure for Nanometer VLSI," Cirrus Logic, Austin, TX, April 17, 2014
[O133] "New Trends in Physical Design for Nanoscale, 3D, and Optical Integration," Fudan University, China, Jan. 10, 2014
[O134] "Intelligent Design and Manufacturing of Future Integrated Circuits," Nanjing University of Science and Technology, China, Jan. 7, 2014
[O135] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Zhejiang University, China, Jan. 6, 2014
[O136] "Design and Manufacturing Closure for Nanometer VLSI," Broadcom, Sunnyvale, Dec. 12, 2013
[O137] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," IEEE CEDA Central Texas Chapter, Nov. 12, 2013
[O138] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, Oct. 31, 2013
[O139] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and Beyond," IEEE CAS Victoria Chapter, Univ. of Victoria, July 22, 2013
[O140] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and Beyond," IEEE CAS Vancouver Chapter, UBC, July 15, 2013
[O141] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Qualcomm, San Diego, CA, July 8, 2013
[O142] "CAD for Nanolithography," School of Microelectronics, Fudan University, China, June 24, 2013
[O143] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, June 20, 2013
[O144] "Physical Design and Manufacturability/Reliability in Extreme Scaling and Beyond," Huada Empyrean Software Co., Beijing, China, June 20, 2013

[O145] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Peking University, Beijing, China, June 18, 2013
[O146] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Fudan University, Shanghai, China, June 13, 2013
[O147] "Design Technologies for Extreme Scaling and Beyond," Texas Instruments, Dallas, Texas, April 29, 2013
[O148] "Design and Manufacturing Closure for Next-Generation Microprocessors," Oracle Labs Tea Talk, Redwood City, CA, April 24, 2013
[O149] "Design for Robustness in Extreme Scaling and 3D-IC," Princeton University – EE Department, March 13, 2013
[O150] "Design for Robustness in Extreme Scaling and 3D-IC," Columbia University - EE, New York, March 12, 2013
[O151] "Dealing with IC Manufacturability and Design Enablement in Extreme Scaling and Beyond," IBM Research Design Automation PIC Seminar, Yorktown Heights, March 11, 2013
[O152] "Dealing with IC Manufacturability in Extreme Scaling," Toshiba, Japan, Jan. 21, 2013
[O153] "Next Generation VLSI CAD for "More Moore" and "More than Moore," Globalfoundries, San Jose, CA, Nov. 8, 2012
[O154] "Design Technologies for "More Moore" and "More than Moore"," Oracle, Santa Clara, CA, Nov. 7, 2012
[O155] "Next Generation VLSI CAD for "More Moore" and "More than Moore," Mentor Graphics, San Jose, CA, Nov. 6, 2012
[O156] "The 'Moore', The Merrier!" Peking University, China, August 21, 2012
[O157] "The 'Moore', The Merrier!" National Taiwan University, Taipei, Taiwan, July 27, 2012
[O158] "Synergistic Design & Technology Co-Optimization for 'More Moore' and 'More than Moore'," National Tsing Hua University, Hsinchu, Taiwan, July 26, 2012
[O159] "Nanolithography and CAD Challenges beyond 14nm," Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, July 25, 2012
[O160] "Nanolithography and CAD Challenges beyond 14nm," Yuan Ze University, Taoyuan, Taiwan, July 25, 2012
[O161] "Nanolithography and CAD Challenges beyond 14nm", EPFL EE Summer Research Institute, Lausanne, Switzerland, June 22, 2012
[O162] "Physical Design in Extreme Scaling/3D Integration and Datapath-Aware Placement," Tabula, Santa Clara, CA, June 7, 2012
[O163] "Challenges and Opportunities for Physical Design in 14nm and Beyond," Samsung Austin Research Center (SARC), Austin, TX, May 29, 2012
[O164] "Design for Manufacturability/Reliability in beyond-14nm/3D-IC Integration and Datapath-aware Placement," IBM Austin Research Lab, Austin, TX, May 11, 2012
[O165] "Nanolithography and CAD Challenges beyond 14nm," National Cheng Kung University, Tainan City, Taiwan, April 26, 2012
[O166] "Design for Manufacturability & Reliability in TSV-based 3D-IC," National Cheng Kung University, Tainan City, Taiwan, April 26, 2012
[O167] "High-Performance VLSI Placement with Automatic Datapath Extraction and Evaluation," National Tsing Hua University and National Chiao Tung University, Hsinchu, Taiwan, April 23, 2012
[O168] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and 3D-IC Integration," Department of Electrical Engineering, University of Southern California, Los Angeles, CA, April 13, 2012
[O169] "Resilient Design in Extremely-Scaled CMOS and 3D-IC Integration," ARM Inc., Austin, TX, April 11, 2012
[O170] "Design for Manufacturability and Reliability in Beyond-14nm Lithography and 3D-IC Integration," Fudan University, Shanghai, China, Jan. 10 2012
[O171] "'More Moore' and 'More than Moore' in Sub-20nm CMOS and 3D-IC," Xidian University, Xi'an, Shaanxi, China, January 3, 2012
[O172] "'More Moore' and 'More than Moore' in Sub-20nm CMOS and 3D-IC," Peking University, Beijing, China, December 30, 2011
[O173] "'More Moore' and 'More than Moore' in Sub-20nm CMOS and 3D-IC," Tsinghua University, Beijing, China, December 29, 2011

[O174] "Resilient Design in Nanoscale CMOS and 3D-IC," Globalfoundries, Sunnyvale, CA, November 11, 2011
[O175] "Resilient Design Closure in Nanoscale CMOS and 3D-IC," Oracle, Sunnyvale, CA, November 9, 2011
[O176] "Resilient Design Closure in Nanoscale CMOS and 3D-IC," ARM, San Jose, CA, November 8, 2011
[O177] "Resilient Design Closure in Nanometer CMOS and 3D-IC," Freescale, Austin, TX, October 19, 2011
[O178] "'More Moore' and 'More than Moore' in Nanometer CMOS and 3D-IC," Shangdong University, Shangdong, China, July 19, 2011
[O179] "'More Moore' and 'More than Moore' in sub-22nm CMOS and 3D-IC," Zhejiang University, Zhejiang, China, July 12, 2011
[O180] "Physical Design and DFM in Sub-22nm and 3D," Politecnico di Torino, Torino, Italy, July 1, 2011
[O181] "Design and Technology Integration in beyond-22nm CMOS and 3D-IC," IMEC, Leuven, Belgium, June 27, 2011
[O182] "'More Moore' and 'More than Moore' beyond 22nm: Challenges and Opportunities," Katholieke Universiteit Leuven, Leuven, Belgium, June 27, 2011
[O183] "Recent Results in Nanometer Physical CAD," AMD, Austin, TX, May 19, 2011
[O184] "Nanometer Physical Design and Technology Co-optimization: A Synergistic Perspective," Samsung Austin Research Center, Austin, TX, May 5, 2011
[O185] "Design and Technology Co-optimization in beyond-22nm CMOS and 3D-IC Integration," Qualcomm, San Diego, CA, April 1, 2011
[O186] "Design and Technology Integration in beyond-22nm CMOS and 3D-IC," Globalfoundries, Sunnyvale, CA, February 4, 2011
[O187] "Design for Manufacturability and Reliability in beyond-22nm CMOS and 3D-IC Integration," Fujitsu Labs, Kawasaki, Japan, January 26, 2011
[O188] "Design for Resilience in Beyond-22nm CMOS and 3D-IC," UIUC ECE Colloquium, Urbana Champaign, IL, September 30, 2010
[O189] "Design for Resilience in Nanometer CMOS and 3D-IC," Samsung, Korea, September 9, 2010
[O190] "Design for Resilience in Nanometer CMOS and 3D-IC," Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, September 8, 2010
[O191] "Design for Resilience in Nanometer CMOS and 3D-IC," Design Automation PIC Seminar Series, IBM T. J. Watson Research Center, Yorktown Heights, NY, July 22, 2010
[O192] "Challenges and Opportunities in Nanometer VLSI and 3D-IC," Fuzhou University, Fuzhou, China, July 4, 2010
[O193] "Design for Manufacturability and Resilience in Nanometer CMOS and 3D-IC," TSMC, Hsinchu, Taiwan, April 28, 2010
[O194] "Design for Resilience in Nanometer CMOS and 3D-IC," at Springsoft, National Chiao Tung University, April 29; at Fudan University and Shanghai Jiaotong University, June 25; at Peking University and Tsinghua University, June 29; at Institute of Computing Technology, Chinese Academy of Sciences, June 30, 2010
[O195] "Design for Manufacturability and Robustness in Nanometer CMOS, 3D-IC, and Emerging Technologies," ITRI, Hsinchu, Taiwan, April 28, 2010
[O196] "Recent Results in Design for Manufacturing and Robustness," Freescale, Austin, TX, April 9, 2010
[O197] "Low Power Design and Challenges in Nanometer Multicore Era," IEEE CAS Melbourne and Victoria University, Melbourne, Australia, August 20, 2009
[O198] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Melbourne, Melbourne, Australia, August 20, 2009
[O199] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Sydney, Sydney, Australia, August 14, 2009
[O200] "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," Institute of Microelectronics, Singapore, July 14, 2009
[O201] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Singapore Chapter, Singapore, July 13, 2009

[O202] "Unified Analysis, Characterization and Optimization of Systematic and Random Variations with Variational Litho-Modeling," SRC e-Workshop, Austin, TX, April 22, 2009
[O203] "On Clock Mesh Design," Sun Microsystems, Austin, TX, March 9, 2009
[O204] "On Graduate Research and Education in US," Zhejiang University, Hangzhou, China, January 12, 2009
[O205] "Synergistic Modeling and Optimization for Nanometer IC Design & Manufacturing Closure," Tsinghua University, Beijing, China, October 24, 2008
[O206] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Taiwan, Kaohsiung, Taiwan, September 10 and 11, 2008
[O207] "Nanometer Physical Design and DFM," SpringSoft, Hsinchu, Taiwan, September 9, 2008
[O208] "On Nanometer VLSI Physical Design and Manufacturing Closure: What, Why, and How?," UFRGS, Porto Alegre, Brazil, August 13, 2008
[O209] "Physical Design Issues in Microfluidic Biochips," Technical University of Dresden, Germany, July 4, 2008
[O210] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE Los Angeles Council, Los Angeles, CA, June 9, 2008
[O211] "New Faculty Seminar on NSF CAREER," FIC, Cockrell School of Engineering, UT Austin, Austin, TX, May 21, 2008
[O212] "Modeling and Optimization for Nanometer IC Design and Manufacturing Integration," AMD, Austin, TX, March 28, 2008
[O213] "Synergistic Modeling and Optimization for Nanometer Design for Manufacturing," Texas Instruments, Dallas, TX, February 15, 2008
[O214] "Synergistic Modeling and Optimization for Physical and Electrical DFM," UT Dallas, Dallas, TX, February 14, 2008
[O215] "Synergistic Modeling and Optimization for Physical and Electrical DFM," UC Santa Barbara, CA, February 8, 2008
[O216] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Seoul National University LSI Workshop, Seoul, Korea, January 25, 2008
[O217] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Samsung Electronics, Seoul, Korea, January 21, 2008
[O218] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Stanford University, Stanford, CA, November 30, 2007
[O219] "Synergistic Modeling and Optimization for Physical and Electrical DFM," University of California at Berkeley, CA, November 30, 2007
[O220] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Mentor Graphics, San Jose, CA, November 29, 2007
[O221] "Challenges and Opportunities for Nanometer VLSI Design and Manufacturability," Tongji University, Shanghai, China, August 23, 2007
[O222] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Tsinghua University and Peking University, Beijing, China, August 22, 2007
[O223] "Challenges and Opportunities for Nanometer IC Design and Manufacturability," Shangdong University, Jinan, China, August 20, 2007
[O224] "Challenges and Opportunities for Nanometer IC Design and Manufacturability," Southeast University, Nanjing, China, August 10, 2007
[O225] "Recent Results and Physical and Electrical DFM," Qualcomm, San Diego, CA, July 11, 2007
[O226] "Synergistic Modeling and Optimization for Physical and Electrical DFM," **Cadence Distinguished Seminar Series**, San Jose, CA, July 11, 2007
[O227] "Recent Research Highlights at UTDA," Cadence Berkeley Lab, Berkeley, CA, July 11, 2007
[O228] "DFM and Physical CAD Research at UTDA," Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, April 25, 2007
[O229] "Modeling & Optimization for Physical and Electrical DFM," National Tsing-hua University, Hsinchu, Taiwan, April 24, 2007
[O230] "Modeling & Optimization for Physical and Electrical DFM," National Taiwan University, Taipei, Taiwan, April 23, 2007

[O231] "Tackling Design for Manufacturability/Variability from Root Causes," Intel Corporation, Santa Clara, CA, February 28, 2007
[O232] "Recent Research on Physical CAD and DFM at UT Design Automation (UTDA) Lab," System LSI Design Workshop, Fukuoka, Japan, September 9, 2006
[O233] "Modeling and Optimization for Nanometer Physical Design and Manufacturability," Fudan University, Shanghai, China, August 24, 2006
[O234] "Physical Design and Manufacturability Closure for Nanometer VLSI/SOC," 6th Emerging Information Technology Conference (EITC), Dallas, TX, August 10, 2006
[O235] "Modeling and Optimization for Nanometer Physical Design and Manufacturability," IBM T. J. Watson Research Center, Yorktown Heights, NY, July 21, 2006
[O236] "The Real DFM - Physical Design for Manufacturability/Variability," Freescale Seminar, Austin, TX, July 13, 2006
[O237] "The True DFM - Physical Design For Manufacturability" (part two), IBM EDA Seminar Series, Fishkill, NY, May 2, 2006 (given through conference call & online)
[O238] "The True DFM - Physical Design For Manufacturability" (part one), IBM EDA Seminar Series, Fishkill, NY, April 25, 2006 (given through conference call & online)
[O239] "New Ideas in Nanometer Physical CAD & DFM," Intel, Santa Clara, CA, February 24, 2006
[O240] "A New LP Based Incremental Timing Driven Placement for High Performance Designs," IBM Austin CAS Conference, Austin, TX, February 17, 2006
[O241] "Nanometer Physical Design for Manufacturability," STARC, Kawasaki, Japan, January 25, 2006
[O242] "Physical Design for Manufacturability," Fujitsu Corporation, Kawasaki, Japan, January 23, 2006
[O243] "New Ideas in Nanometer Physical CAD & Manufacturability," Tsinghua University, Beijing, China, October 28, 2005
[O244] "Challenges and Opportunities in Nanometer VLSI Physical Design & Manufacturing Closure," Peking University, Beijing, China, October 28, 2005
[O245] "Physical Design for Manufacturability," Zhejiang University, Hanzhou, China, October 24, 2005
[O246] "New Ideas in Nanometer Physical Synthesis & DFM," IBM T. J. Watson Research Center, Yorktown Heights, NY, August 8, 2005
[O247] "Litho-Aware Routing & Diffusion-Based Placement," Cadence, San Jose, CA, July 28, 2005
[O248] "New Ideas in Nanometer Physical CAD," Sun Microsystems, Austin, TX, July 21, 2005
[O249] "New Ideas in Placement & Variation-Tolerant Clock Designs," Intel Strategic CAD Lab, Hillsboro, OR, July 8, 2005
[O250] "New Ideas in Placement & DFM," Synopsys Advanced Technology Group, Hillsboro, OR, July 7, 2005
[O251] "True Manufacturability Aware Physical Design," Freescale, Austin, TX, May 27, 2005
[O252] "Physical CAD Research on Nanometer Design and Manufacturing Closure," Texas Instruments, Dallas, TX, March 18, 2005
[O253] "Diffusion-Based Placement Migration," IBM Austin CAS Conference, Austin, TX, February 25, 2005
[O254] "Nanometer Physical Synthesis for Multi-Objective Design Closure and Manufacturability," Magma Design Automation, Santa Clara, CA, November 5, 2004
[O255] "Nanometer Physical Synthesis for Multi-Objective Design Closure and Manufacturability," Cadence Berkeley Lab, Berkeley, CA, November 5, 2004
[O256] "Nanometer Physical Synthesis for VLSI Design Closure," University of Maryland at College Park, MD, October 22, 2004
[O257] "Recent Results of Physical Synthesis with Nanometer Effects," IBM Austin Research Lab Seminar, Austin, TX, October 8, 2004
[O258] "Holistic Approaches for Multi-Objective Design Closure with Nanometer Effects," AMD, Austin, TX, October 5, 2004
[O259] "Nanometer Physical Synthesis for Timing, Signal Integrity, and Low Power Optimizations," Synopsys Advanced Technology Group, Hillsboro, OR, October 1, 2004
[O260] "Nanometer Physical Synthesis for Timing, Signal Integrity, and Low Power Optimizations," Intel Strategic CAD Lab, Hillsboro, OR, September 30, 2004
[O261] "Integrated Placement with Nanometer Timing and Signal Integrity Closure," Electrical Engineering Department, Texas A&M University, College Station, TX, September 28, 2004

[O262] "Recent Results of Physical Synthesis with Nanometer Effects," Intel, Austin, TX, September 9, 2004
[O263] "Nanometer VLSI Designs: Challenges, Opportunities and Optimizations," Shanghai Jiaotong University, Shanghai, China, August 17, 2004
[O264] "Holistic Approaches of Next-Generation Physical Design to Cope with Nanometer Effects," Fudan University, Shanghai, China, August 17, 2004
[O265] "Physical Synthesis in Nanometer VLSI Designs," Tsinghua University, China, August 12, 2004
[O266] "Physical Design with Integrity." Agere Systems, Allentown, PA, July 27, 2004
[O267] "Recent Results of Physical Synthesis with Nanometer Effects," IBM T. J. Watson Research Center, Design Automation PIC Seminar, Yorktown Heights, NY, July 26, 2004
[O268] "Nanometer Physical Synthesis for Performance, Power and Predictability," AMD, Austin, TX, March 4, 2004
[O269] "Physical Synthesis for Nanometer Designs," IEEE CAS/SSC Joint Chapter Meeting, Austin, TX, February 26, 2004
[O270] "Physical Synthesis for Nanometer Designs," Motorola SPS (Freescale), Austin, TX, February 19, 2004
[O271] "Interconnect-Centric Design Closure for High Performance and Low Power VLSI," ECE Department, Yale University, New Haven, CT, May 12, 2003
[O272] "Interconnect-Centric Design Closure for High Performance and Low Power VLSI," ECE Department, University of Wisconsin at Madison, Madison, WI, May 1, 2003
[O273] "Physical Design Closure for High Performance and Low Power VLSI," ECE Seminar, Purdue University, West Lafayette, IN, April 17, 2003
[O274] "Physical Design Closure for High Performance and Low Power VLSI," EE-Systems, University of Southern California, Los Angeles, CA, April 14, 2003
[O275] "Physical Design Closure for High Performance and Low Power VLSI," Department of Electrical and Computer Engineering, UT Austin, Austin, TX, April 7, 2003
[O276] "Physical Design Closure for High Performance and Low Power VLSI," Division of Engineering, Brown University, Providence, RI, April 2, 2003
[O277] "Challenges and Opportunities for Nanometer Design Closure," VLSI Seminar Series, University of Michigan, Ann Arbor, MI, October 28, 2002
[O278] "Interconnect Prediction and Planning for Design Closure," EE Seminar, Fudan University, Shanghai, China, November 26, 2001

MEDIA COVERAGE:

- Semiconductor Engineering, September 7, 2016, "Joint R&D Has Its Ups And Downs," http://semiengineering.com/joint-rd-has-its-ups-and-downs/
- EE Times, April 8, 2016, "Machine Learning Routes Chips," http://www.eetimes.com/document.asp?doc_id=1329391 (covered my students and I as the ISPD'16 FPGA Placement Contest 1st Place Winners)
- EE Times, April 9, 2014,"ISPD-14 Focuses on FinFETs, Security, Supply Chain," http://www.eetimes.com/document.asp?doc_id=1321843 (covered our ISPD'14 Best Paper)
- SRC Press Release, "2013 Technical Excellence Award Presented to David Pan from UT/Austin" http://www.src.org/award/tech-excellence/2013/
- Stanford and UT Austin Professors to Be Honored for Advancing Chip Research at Annual SRC TECHCON Event
    - http://www.src.org/newsroom/press-release/2013/499/
    - Business Wire Article: http://www.businesswire.com/news/home/20130905005318/en/Stanford-UT-Austin-Professors-Honored-Advancing-Chip
    - + other media coverage (Yahoo Finance, Market Watch, etc.)
- June 2013, DAC Roundtable "Experts at the Table: Who Pays for Low Power?" hosted by System-Level Design Editor-in-Chief Ed Sperling http://lp-hp.com/blog/2013/07/11/experts-at-the-table-who-pays-for-low-power/

- Synopsys Conversation Central, "CAD Research and Education in Extreme Scaling and Beyond," hosted by Karen Bartleson, June 2013 (Synopsys web site, YouTube, Podcast)
  - Show Notes page: http://bit.ly/13jZHFb
  - YouTube Video: http://youtu.be/06mz2HLkWpk
  - iTunes Page: http://bit.ly/QPtlHr
- EE Times, April 13, 2011: "ISPD spots 3-D, maskless-lithography trends," http://www.eetimes.com/electronics-news/4215124/ISPD-reveals-3-D--maskless-lithography-trends-
- March 20, 2010: Interview by Prof. Patrick Madden, ACM/SIGDA Chair, on the ASPDAC 2010 Best Paper on *"A Multi-Objective Min-Cut Based Layout Decomposition Framework for Double Patterning Lithography,"* http://www.youtube.com/watch?v=N76t3YNQoPc
- May 19, 2009: "The IEEE CANDE Committee Elects Officers", Reuters, Yahoo Finance, etc. http://www.reuters.com/article/pressRelease/idUS155240+19-May-2009+BW20090519
- EE Times, April 21, 2008, "Lab-on-chip design automation takes cue from EDA," http://www.eetimes.com/electronics-news/4076826/Lab-on-chip-design-automation-takes-cue-from-EDA
- EE Times, April 17, 2008, "Future of chip design revealed at ISPD," http://www.eetimes.com/showArticle.jhtml?articleID=207400313
- EE Times (China/Taiwan), April 30, 2007, "VLSI-DAT 盛况空前，业界专家布道前瞻新技术" (in Chinese), http://www.eetchina.com/ART_8800462927_480401_NT_0f306e22.HTM
- EE Times, April 2, 2007, "Rethinking statistical timing analysis," http://eetimes.com/news/design/showArticle.jhtml?articleID=198700121
- EE Times, March 22, 2007, "IC routing contest boosts CAD research," http://eetimes.com/news/design/showArticle.jhtml?articleID=198500084
- EE Times, June 19, 2006, "Chip designers feel the heat - Accurate thermal analysis cools the effects of sub-90-nm design," http://www.eetimes.com/news/design/showArticle.jhtml?articleID=189400781
- EE Times, April 17, 2006, "Paths to better timing analysis," http://www.eet.com/news/latest/showArticle.jhtml?articleID=185302541
- EE Times, October 28, 2005, "EDA startup forms technical advisory board," http://www.eetimes.com/news/design/showArticle.jhtml?articleID=172901367
- EE Times, July 11, 2005, "Shift to 65 nm has its costs," http://www.eetimes.com/news/latest/showArticle.jhtml?articleID=165701002

CURRENT PHD/MS STUDENTS AND VISITING SCHOLARS:

- **Students admitted to Ph.D. candidacy**:
  - Yibo Lin
  - Joydeep Mitra (part-time, with Mentor Graphics)
  - Jiaojiao Ou
- **Post M.S. students preparing to take Ph.D. qualifying exam**:
  - Shounak Dhar
  - Meng Li
  - Wuxi Li
  - Derong Liu
  - Biying Xu
  - Zheng Zhao
  - Abhishek Bhaduri (part-time, with Cirrus Logic)
  - Che-Lun Hsu (part-time, with Oracle)
  - Jingyi Zhou (part-time, with Cadence)
- **M.S. in progress:**
  - Wei Ye
- **Visiting Scholars:**

- Taiki Kimura (Toshiba, Japan), May 2015 – October, 2016
- Ronghua Jiang (Sichuan University, China), March 2016 – March 2017
- Jun Liu
- Jun Zhang
- Zhijian Pan

PH.D. SUPERVISIONS COMPLETED:

Name	PhD Dissertation	Semester	First job after PhD (current position)
1. Haoxing Ren	Incremental Placement for Modern VLSI Design Closure	Spring 2006	Research Staff Member, IBM T. J. Watson Research (now Senior Research Scientist, NVIDIA)
2. Gang Xu	Layout Optimization Algorithms for VLSI Design and Manufacturing	Summer 2007	R&D Engineer, Mentor Graphics (now Software Engineer, Google)
3. Tao Luo	Nanometer VLSI Placement and Optimization for Multi-Objective Design Closure	Fall 2007	Sr. MTS, Magma (now Sr. Software Engineer, AppLovin)
4. Anand Ramalingam	Analysis Techniques for Nanometer Digital Integrated Circuits	Fall 2007	Member of Consulting Staff, Magma Design Automation (acquired by Synopsys)
5. Minsik Cho	Physical Synthesis for Nanometer VLSI and Emerging Technologies	Summer 2008	Research Staff Member, IBM T. J. Watson Research Center
6. Anand Rajaram	Synthesis of Variation Tolerant Clock Distribution Networks	Fall 2008	Member of Consulting Staff, Magma Design Automation (acquired by Synopsys)
7. Peng Yu	Fast and Accurate Lithography Simulation and Optical Proximity Correction for Nanometer Design for Manufacturing	Spring 2009	Post-Doc Researcher, Baylor College of Medicine (now Assistant Professor, Texas A&M University)
8. Xiaokang (Sean) Shi	Modeling and Optimization to Connect Layout with Silicon for Nanoscale IC	Fall 2009	Sr. Component Engineer, Intel Corporation
9. Kun Yuan	VLSI Physical Design Automation for Double Patterning and Emerging Lithography	Fall 2010	Sr. Member of Technical Staff, Cadence (now Software Engineer at Facebook)
10. Ashutosh Chakraborty	Mechanical Stress and Circuit Aging Aware VLSI CAD	Fall 2010	Senior Hardware Engineer, Oracle (now Sr. Staff R&D Engineer, Synopsys)
11. Jae-Seok Yang	Nanometer VLSI Design-Manufacturing Interface for Large Scale Integration	Spring 2011	Senior Engineer, Samsung (now Principal Engineer)
12. Wooyoung Jang	Architecture and Physical Design for Advanced Networks-on-Chip	Spring 2011	Senior Engineer, Samsung (now Assistant Professor, Dankook University, Korea)
13. Yongchan (James) Ban	Lithography Variability Driven Cell Characterization and Layout Optimization for Manufacturability	Spring 2011	Senior Engineer, Intel (now Senior Member of Technical Staff, Globalfoundries)

14. Duo Ding	CAD for Nanolithography and Nanophotonics	Summer 2011	Senior Hardware Engineer, Oracle (now Principal Engineer)
15. Samuel Ward	Physical Design Automation of Structured High-Performance Integrated Circuits	Fall 2013	Data Scientist, Apple Inc.
16. Jhih-Rong (Jerrica) Gao	Lithography Aware Physical Design and Layout Optimization for Manufacturability	Spring 2014	Senior Member of Technical Staff, Cadence (now Principal Software Engineer)
17. Jiwoo Pak	Electromigration Modeling and Layout Optimization for Advanced VLSI	Spring 2014	Senior Member of Technical Staff, Cadence (now Principal Software Engineer)
18. Bei Yu	Design for Manufacturing with Advanced Lithography	Summer 2014	Post-doc Researcher, UT Austin (now Assistant Professor at Chinese University of Hong Kong)
19. Yilin Zhang	Interconnect Optimizations for Nanometer VLSI Design	Summer 2014	Software Scientist, Rocket Fuel Inc. (now Software Engineer, Google)
20. Subhendu Roy	Logic and Clock Network Optimization in Nanometer VLSI Circuits	Summer 2015	Principal Software Engineer, Cadence
21. Xiaoqing Xu	Standard Cell Optimization and Physical Design in Advanced Technology Nodes	Spring 2017	Senior Researcher, ARM Research

M.S. SUPERVISIONS COMPLETED (with Thesis or Report):

1. Jun Liu, August 2005
2. Andy Havlir, December 2005
3. Emiliano Lozano, May 2008
4. Varsha Dadlani, May 2008
5. Duo Ding, May 2008
6. Ashutosh Chakraborty, May 2008
7. Sean Xiaokang Shi, December 2008
8. Katrina Lu, December 2008
9. Tony Quan, August 2009
10. Anurag Kumar, December 2009
11. Boyang Zhang, May 2012
12. Wen Zhang, August 2012
13. Jagmohan Singh, August 2013

BS and REU Alumni:

- Joshua Gnanayutham
- Saanika Kenkare
- Rohan Tanna
- Miranda M. Pacheco
- August Shi
- Michael Booker
- Doug Ilijev
- Marc Anthony Gonzalez (B.S. 2011)
- Dhruv Mehrotra (B.S. in Jan. 2004)

Visiting Scholars/Students Alumni:

- Tung-Chieh Chen (National Taiwan University, Taiwan), Jan. – Dec. 2007
- Shanhu Shen (Zhejiang University, China), Sept. 2007 to Aug. 2008
- Ou He (Tsinghua University, China), October 2009 – October 2010
- Yen-Hung Lin (National Chiao Tung University, Taiwan), Mar. to Dec. 2011 (now TSMC)
- Prof. Weifeng Lv (Hangzhou Dianzi University, China), Sept. 2013 – Feb. 2014
- Dr. Junhyung Um (Samsung Electronics Principal Engineer), Jan. to Dec. 2014
- Wei Ye (Zhejiang University), Internship, July to Dec. 2014
- Dr. Tetsuaki Matsunawa (Toshiba), Oct. 2013 – April, 2015
- Vinícius dos Santos Livramento (Federal University of Santa Catarina, Brazil), Jan. 2016 – June 2016

David Z. Pan's IEEE-style Biography:

David Z. Pan (S'97–M'00–SM'06–F'14) received his B.S. degree from Peking University, and his M.S. and Ph.D. degrees from University of California, Los Angeles (UCLA). From 2000 to 2003, he was a Research Staff Member with IBM T. J. Watson Research Center. He is currently the Engineering Foundation Professor at the Department of Electrical and Computer Engineering, The University of Texas at Austin. His research interests include cross-layer nanometer IC design for manufacturability, reliability, security, physical design, analog design automation, and CAD for emerging technologies such as 3D-IC and nanophotonics. He has published over 280 papers in refereed journals and conferences, and is the holder of 8 U.S. patents. He has graduated 21 PhD students who are now holding key academic and industry positions.

He has served as a Senior Associate Editor for ACM Transactions on Design Automation of Electronic Systems (TODAES), an Associate Editor for IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Very Large Scale Integration Systems (TVLSI), IEEE Transactions on Circuits and Systems PART I (TCAS-I), IEEE Transactions on Circuits and Systems PART II (TCAS-II), IEEE Design & Test, Science China Information Sciences, Journal of Computer Science and Technology, IEEE CAS Society Newsletter, etc. He has served in the Executive and Program Committees of many major conferences, including DAC, ICCAD, ASPDAC, and ISPD. He is the ASPDAC 2017 Program Chair, ICCAD 2016 Vice Program Chair, ICCAD 2016 Special Session/Tutorial Chair, DAC 2014 Tutorial Chair, and ISPD 2008 General Chair. He has served as Chair of the IEEE CANDE Committee and ACM/SIGDA Physical Design Technical Committee.

He has received a number of awards for his research contributions, including the SRC 2013 Technical Excellence Award, DAC Top 10 Author in Fifth Decade, DAC Prolific Author Award, ASP-DAC Frequently Cited Author Award, 13 Best Paper Awards at premier venues (HOST 2017, SPIE 2016, ISPD 2014, ICCAD 2013, ASPDAC 2012, ISPD 2011, IBM Research 2010 Pat Goldberg Memorial Best Paper Award, ASPDAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007, 2012 and 2015) plus 11 additional Best Paper Award nominations at DAC/ICCAD/ASPDAC/ISPD, Communications of the ACM Research Highlights (2014), ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award (2009), UT Austin RAISE Faculty Excellence Award (2014), and many international CAD contest awards, among others. He is a Fellow of IEEE and SPIE.