EE382M-7 VLSI I (Fall 2014; Unique ID: 17385)

Instructor: **Prof. David Z. Pan**
TTh 9:30 – 11:00am, BUR 224

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Course description:
This course covers the fundamental process of designing CMOS VLSI circuits. It will begin with a review of the basics of CMOS transistor operation and the manufacturing process for CMOS VLSI chips. We will then study in detail the problem of implementing logic gates in CMOS. Specifically, we will cover layout, design rules, and circuit families. Afterwards, we will examine techniques for timing and power analysis, as well as other key issues such as interconnect. We will also examine ways to optimize timing and power. This will be followed by an overview of datapath design, specifically adders. We will also study memory arrays, including SRAM and DRAM cell and clock design. The course will conclude with a survey level treatment of various peripheral topics, including functional verification, test, design-for-test, electrical effects, and future trends. We may have guest lecturers from industry to talk about real-world design practices.

Prerequisite:
This course is intended for ECE graduate students. A knowledge of Electrical Circuits (EE411 or equivalent), and Digital Logic Design (EE316 or its equivalent) is required.

Textbook:

- N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* (*the 4th Edition)*, 2011. Addison-Wesley.

Grading Policy:
- 10% homework
- 35% three major labs
- 30% two in-class midterms
- 25% final project

Lecture Outline (tentative):

1. Introduction, CMOS Transistors
2. CMOS Fabrication and Layout

3. CMOS Logic
4. MOS Transistor Theory
5. DC and Transient Gate Characteristics
6. Logical Effort
7. Combinational Circuits
8. Design of Adders
9. Interconnects in CMOS Technology
10. Sequential Elements
11. Hardware Description Languages, Synthesis
12. Design Styles
13. Datapath Design
14. Memories
15. Dynamic CMOS Logic
16. Deep Submicron Issues
17. CAMs, ROMs, PLAs
18. Circuit Pitfalls
19. Manufacturing Test
20. Design for Testability
21. Design Verification
22. Packaging and I/O
23. Design for Low Power
24. Skew-Tolerant Design
25. Scaling
26. Future Directions

College of Engineering Drop/Add Policy:

The Dean must approve adding or dropping courses after the fourth class day of the semester.

Students with Disabilities:

The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4641 TTY or the College of Engineering Director of Students with Disabilities at 471-4382.

Emergency Preparedness and Emergency Plan Instructions:

Every member of the university community must take appropriate and deliberate action when an emergency strikes a building, a portion of the campus, or entire campus community. Emergency preparedness means we are all ready to act for our own safety and the safety of others during a crisis. It takes an effort by all of us to create and sustain an effective emergency preparedness system. Your support is important to achieving the best possible outcomes during a crisis event. An emergency preparedness review will be given at the first class.