EE382V: Optimization Issues in VLSI CAD
(Fall 2013 - 17305)

Instructor: Prof. David Z. Pan

Lecture hours and location: Tue/Thu 11-12:30pm, ENS 116
Office hours: M/W 1:30-2:30pm and by appointment. ACES Building 5.434
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Course description:
As CMOS scales into very deep-submicron dimensions, modern VLSI designs have become interconnect-dominated for the overall chip performance. Meanwhile, as CMOS scaling continues to 45nm, 32nm, 22nm, and beyond, power, manufacturability, reliability have become key limiting factors in achieving the ultimate design and manufacturing closure with stringent turn-around-time. Intelligent computer-aided design (CAD) and optimization are essential to providing the best overall system performance, power, reliability, and yield. This course will study a number of key *optimization techniques with underlying modeling issues* to deal with these nanometer design challenges. Guest lecturers from industry will be invited to provide supplementary views and current industry challenges/practices.

Prerequisite:
Introduction to VLSI (460R or equivalent) and Algorithms (360C), or consent of the instructor.

Textbook and Reader:
No textbook is required. A collection of reference books and papers will be posted on the class web site as a course reader.

Grading Policy (tentative):
10% class participation/presentation, 20% homework, 30% midterm, 40% project.

College of Engineering Drop/Add Policy:
The Dean must approve adding or dropping courses after the fourth class day of the semester.

Students with Disabilities:
The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4641 TTY or the College of Engineering Director of Students with Disabilities at 471-4382.

TOPICS OUTLINE (tentative)

1. Introduction and IC technology trends
2. Modeling and optimization in VLSI/CAD overview
3. Transistor/gate sizing, wire sizing/spacing/planning
4. Buffer insertion, optimization, and planning
5. Congestion modeling and optimization
6. Noise modeling and reduction
7. Clock network synthesis
8. Modern large-scale VLSI placement
9. Low power design and optimizations
10. Design for manufacturability and reliability
11. Modeling and optimization for 3D-IC
12. Design Automation for emerging technologies (biochip, nanophotonics…)

REFERENCES

- **Mainly based on technical papers from journals and conference proceedings, such as TCAD, TVLSI, DAC, ICCAD, ASPDAC, ISPD, ISLPED, etc.**
- Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, *Handbook of Algorithms for Physical Design Automation*, CRC Press, 2009
- Luciano Lavagno, Grant Martin, and Louis Scheffer, *Electronic Design Automation for Integrated Circuits Handbook* - 2 Volume Set, April 2006
- Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, *VLSI Physical Design: From Graph Partitioning to Timing Closure*, Springer 2011
- Jan Rabaey, *Low Power Design Essentials*, Springer 2009
- Michael Orshansky, Sani Nassif, Duane Boning, Design for Manufacturability and Statistical Design: A Constructive Approach, Springer 2008
- David Z. Pan, Minsik Cho, Yuan Kun, *Manufacturability Aware Routing in Nanometer VLSI (Foundations and Trends in Electronic Design Automation),* Now Publishers, 2010
- Yuan Xie, Jingsheng Jason Cong, Sachin Sapatnekar, *Three-Dimensional Integrated Circuit Design: EDA, Design and Microarchitectures*, Springer, 2010
- Sung Kyu Lim, *Design for High Performance, Low Power, and Reliable 3D Integrated Circuits*, Springer 2012