Nanometer IC Design for Manufacturability Research at UT Austin

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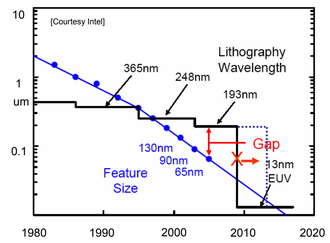
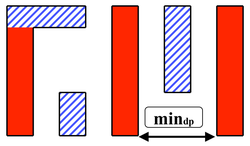
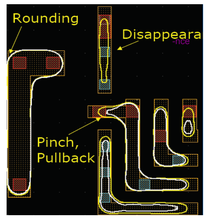
Motivations

- 193nm lithography extension: double/multiple patterning
- EUV and other emerging lithography
- Much closer design and manufacturing interaction

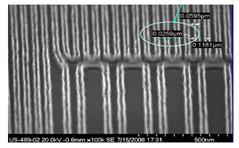


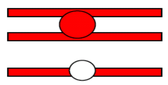
193i w/ DPL





Quadruple patterning





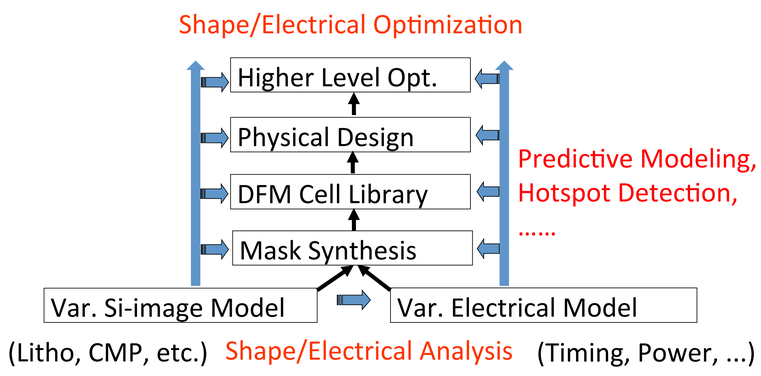
Random defects

EUV still messy

Related SRC Tasks

- Task 1362 - RET Aware Routing with Design-Oriented Lithography Modeling (11/2005-10/2008)
- Task 1422 - Unified Treatment of Systematic and Random Variations for Analysis/Optimization with Variational Litho-Modeling (07/2006-06/2009)
- Task 1833 - An Exploratory DFM Toolkit for Standard Cell Library Analysis and Design in 32nm and Below (08/2008-07/2011)
- Task 2414 - Robust Standard Cell Design and Layout Regularity Study with Nanolithography (04/2013-03/2016)

Cross-Layer Synergistic DFM



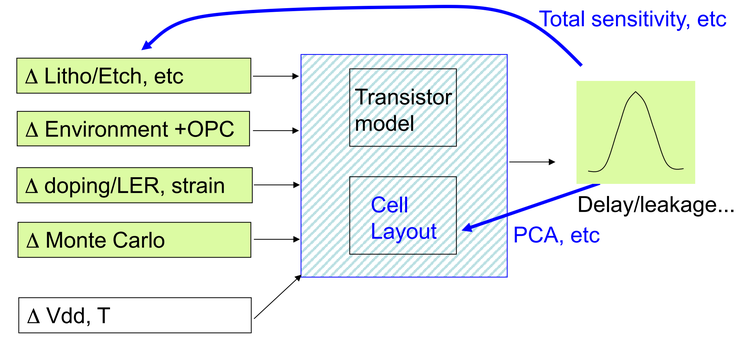
Research Highlights

Problems	Solutions	Selected Pubs
Litho Modeling, OPC, Variation Analysis	Variational lithography modeling; PV-OPC	DAC06, ICCAD06, ICCAD07, SRC Inventor Recognition Award
Litho Hotspot Detection & Mitigation	Data/machine learning; meta-classification; multi-level	ICICDT09 BPA*, DAC11, TCAD11, ASPDAC12 BPA
Double/Triple Patterning Lithography (DPL/TPL)	Layout decomposition; early physical design optimization; deal with both LELE and SADP	ICCAD08, ISPD09, DAC09, ASPDAC10 BPA, IBM Research 2010 BPA, ICCAD10, DAC11, ICCAD11 BPC*, ICCAD13
Standard Cell DFM & Opt.	Total sensitivity based modeling and optimization; cell placement	ISPD10, DAC10, DAC11, ICCAD13
DFM Aware Routing	Systemic framework from global to detailed routing, dealing with litho, redundant via, CMP, random defect, DPL, TPL	DAC06 BPC, ICCAD06, DAC07, DAC08, ICCAD08, DAC09, FTEDA10, DAC11, ICCAD11, ISPD12, ICCAD12, SRC Inventor Recognition Award
Emerging Lithography	E-beam throughput optimization	ISPD11 BPA, ASPDAC13 BPC, DAC13

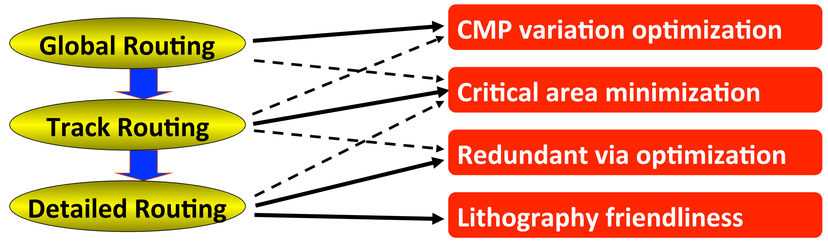
*** BPA – Best Paper Award; BPC – Best Paper Candidate**

Sample Results

- Standard cell library DFM tool kit

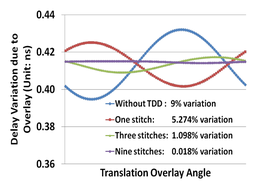


- DFM aware routing

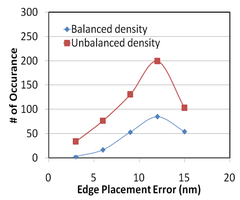


Sample Results

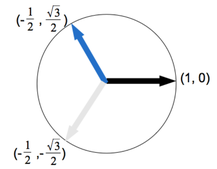
- Multi-objective double/multiple patterning decomposition



Overlay compensation

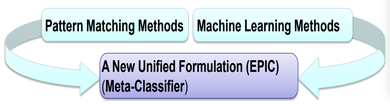


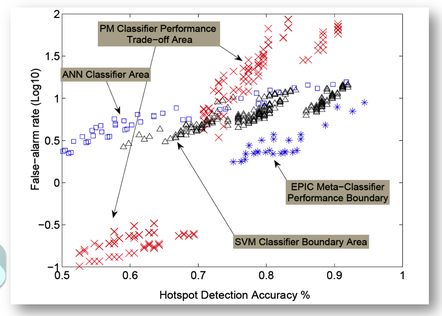
Balancing Density



Novel vector programming formulation for TPL

- Lithography hotspot detection and mitigation
  - Detailed litho simulations : too slow to guide PD
  - Proposed novel machine learning and hybrid pattern matching methods
  - Accuracy vs. false alarm





Students & Technology Transfer

- Students involved and SRC companies they joined
  - Yongchan Ban (PhD'11, Intel), Ashutosh Chakraborty (PhD'10), Minsik Cho (PhD'08, IBM), Duo Ding (PhD'11), Jhih-Rong Gao, Katrina Lu (MS'08, SRC Scholarship, Intel), Joydeep Mitra, Xiaokang Shi (PhD'09, Intel), Gang Xu (PhD'07, Mentor), Xiaoqing Xu, Jae-seok Yang (PhD'11), Bei Yu, Peng Yu (PhD'09), Kun Yuan (PhD'10)
- Technology transfer
  - DFM aware routing algorithms and methodologies widely adopted in industry (EDA companies and in-house EDA tools such as IBM and Intel)
  - DFM standard cell tool kit used by Freescale
  - Lithography hotspot detection algorithms and tools used by Mentor Graphics
  - Double/triple patterning layout decomposition and physical design a must for 22nm/14nm (IBM, Globalfoundries, Mentor Graphics…)
  - Open-sourced award winning BoxRouter
  - SRC sponsored patents on variational lithography modeling/PV-OPC and BoxRouter
- Many (20+) SRC liaisons: thank you very much!