Global Interconnect Sizing and Spacing with Consideration of Coupling Capacitance *

Jason Cong, Lei He, Cheng-Kok Koh, and Zhigang Pan
{cong, helei, kohck, pan}@cs.ucla.edu
Department of Computer Science
University of California, Los Angeles, CA 90095

May 1, 1998

Abstract

This paper presents an efficient approach to perform *global interconnect sizing and spacing* (GISS) for multiple nets to minimize interconnect delays with consideration of coupling capacitance, in addition to area and fringing capacitances. We introduce the formulation of *symmetric* and *asymmetric* wire sizing and spacing. We prove two important results on the *symmetric* and *asymmetric effective-fringing properties* which lead to a very effective bound computation algorithm to compute the upper and lower bounds of the optimal wire sizing and spacing solution for *all* nets under consideration. Our experiments show that the upper and lower bounds often meet quickly or become close after a few iterations for most wire segments. When the lower and upper bounds do not meet, we then apply a bottom-up dynamic programming-based refinement algorithm to compute the final wire sizing and spacing solution for each net. To our knowledge, this is the first in-depth study of global wire sizing and spacing for *multiple nets* with consideration of coupling capacitance. Experimental results show that our GISS solutions lead to substantial delay reduction than existing single net wire-sizing solutions without consideration of coupling capacitance.

* This work is partially supported by the NSF Young Investigator Award MIP-9357582 and a grant from Intel under the California MICRO Program.

1 Introduction

There have been extensive studies in recent years on the optimal wire-sizing problem. Most early works used Elmore delay model [1] for interconnects and study the discrete wire sizing [2, 3, 4] and continuous wire shaping or sizing [5, 6]. The wire-sizing problem is also studied under high-order delay model in [7, 8]. A comprehensive survey of these optimization techniques can be found in [9]. These works showed that significant delay reduction can be achieved by optimal wire-sizing in submicron designs. However, none of them explicitly considered the coupling capacitance.

As VLSI technology continues to push toward deep submicron, the coupling capacitance between adjacent wires has become the dominating component in the total interconnect capacitance, due to the decreasing spacing between adjacent wires and the increasing wire aspect ratio for deep submicron processes (the minimum spacing for $0.35\mu m$ it has reached 1.5 in $0.35\mu m$ logic processes, and will reach 2.5 in $0.18\mu m$ logic processes [10]).

In order to understand the importance of the coupling capacitance, we conducted some experiments based on a set of advanced process parameters from Intel and use the nets extracted from an Intel microprocessor chip [1]. We first obtain routing and wire sizing solutions by the simultaneous topology construction and wiresizing algorithm [12] with consideration of only the area and the fringing capacitances. We then run HSPICE simulations on these solutions under different spacing assumptions with consideration of coupling capacitances provided by Intel. Table 1 shows the maximum delays of the same routing and wire sizing solution under four different spacings: the infinite spacing means that all same-layer neighboring wires to these nets are too far away to have coupling effect, the $0.5\mu m$ for layer M1 and $1.5\mu m$ for layer M5 mean that same-layer neighboring wires are always $0.5\mu m$ or $1.5\mu m$ away from these nets, and $random1$ and $random2$ mean that same-layer neighboring wires are at random spacings (from $0.32\mu m$ to $2.72\mu m$ for layer M1, and from $1.28\mu m$ to $4.48\mu m$ for layer M5, with step to be $0.2\mu m$) for each segment of these nets. The coupling capacitance is determined according to these spacings, except that there is no such capacitance in the infinite spacing case. Both the maximum delay and the power dissipation may increase drastically when the coupling capacitance is taken into account. For example, the maximum delay for Net5 on layer M1 at spacing *random1* is increased by 38.7% when compared with that at the infinite spacing; the power dissipation for Net5 on M1 layer at the infinite spacing is 1.53 mW, but becomes 3.83 mW (a factor of 2.5x increase) at $0.5\mu m$ spacing. These results show that it is unlikely that an optimal wiresizing solution which considers only the area and the fringing capacitances would remain optimal when the coupling capacitance is considered.

High coupling capacitance in deep submicron design results in both noise (capacitive crosstalk) and additional delay. In this paper, we study the *global interconnect sizing and spacing* (GISS) problem for delay minimization with consideration of the coupling capacitance, in addition to the area and fringing capacitances. In Section 2, we introduce the problem formulation

[1] These nets are multi-source nets originally used in [11, 4]. We randomly assign one as the unique single source for each net in our experiments.

maximum delay (ns) under different spacings								
	All wires in M1 layer				All wires in M5 layer			
spacing	∞	0.5 μm	random1	random2	∞	1.5 μm	random1	random2
Net1	0.1356	0.3750	0.2386	0.2363	0.1617	0.2890	0.2496	0.2017
Net2	0.2542	0.7143	0.4494	0.3930	0.2713	0.4711	0.3903	0.3544
Net3	0.7376	1.9168	0.8964	0.9613	0.5870	1.0029	0.7927	0.7502
Net4	0.8851	2.2896	1.3343	1.4783	0.5895	1.0071	0.8417	0.8038
Net5	2.7637	5.7931	3.7653	3.4119	1.7838	3.6393	2.8732	2.7871

Table 1: Maximum delays (ns) for Intel nets with neighboring wires at different spacings (the driver resistance is 270 Ω)

for *symmetric* and *asymmetric* wire sizing and spacing for both single and multiple nets. In Section 3, we present a dynamic programming based algorithm for single net optimization. Then in Section 4, we reveal two *effective-fringing properties* for both symmetric and asymmetric wire-sizing, and propose a very efficient bound computation algorithm to compute the upper and lower bounds of the optimal wire sizing and spacing solution for *all* nets under consideration, not just *one* net. When the lower and upper bounds do not meet, we then apply a bottom-up dynamic programming-based refinement algorithm to compute the final wire sizing and spacing solution for each net. Experimental results in Section 5 show substantial improvement of GISS algorithm over previous single-net optimal wire-sizing algorithm without coupling capacitance consideration. Discussion and Future work will be given in Section 6.

2 Problem Formulation

2.1 Symmetric and Asymmetric Wire Sizing

Given a layout of n nets, denoted $\mathcal{N}_i$ for $i = 1...n$. Net $\mathcal{N}_i$ consists of $n_i + 1$ terminals $\{s_0^i, \cdots, s_{n_i}^i\}$ connected by a routing tree, denoted T_i. s_0^i is the source of $\mathcal{N}_i$, and the driver D_i at the source has an effective output resistance of R_i. The rest of the terminals are sinks. The terminals (source and sinks) of T_i are at fixed locations, and T_i consists of m_i wire segments denoted by $\{E_1^i, \cdots, E_{m_i}^i\}$. The *center-line* of a wire segment divides the original wire segment evenly. In Figure 1(a), for example, two horizontal wire segments E_1 and E_2 are shown with their center-lines. We assume that the center-line for each wire segment is fixed during wire sizing and spacing.

Each wire segment has a set of discrete choices of wire widths $\{W_1 = W_{min}, W_2, \cdots, W_r\}$. We use w_E to denote the width of the wire segment E. All previous works implicitly assumed *symmetric wire-sizing*, which widens or narrows each wire segment in a symmetric way above and below the center-line of the original wire segment, i.e, each wire segment has one piece wirewidth. An example of symmetric wire-sizing of the two wire segments E_1 and E_2 with a neighboring net is shown in Figure 1(b).

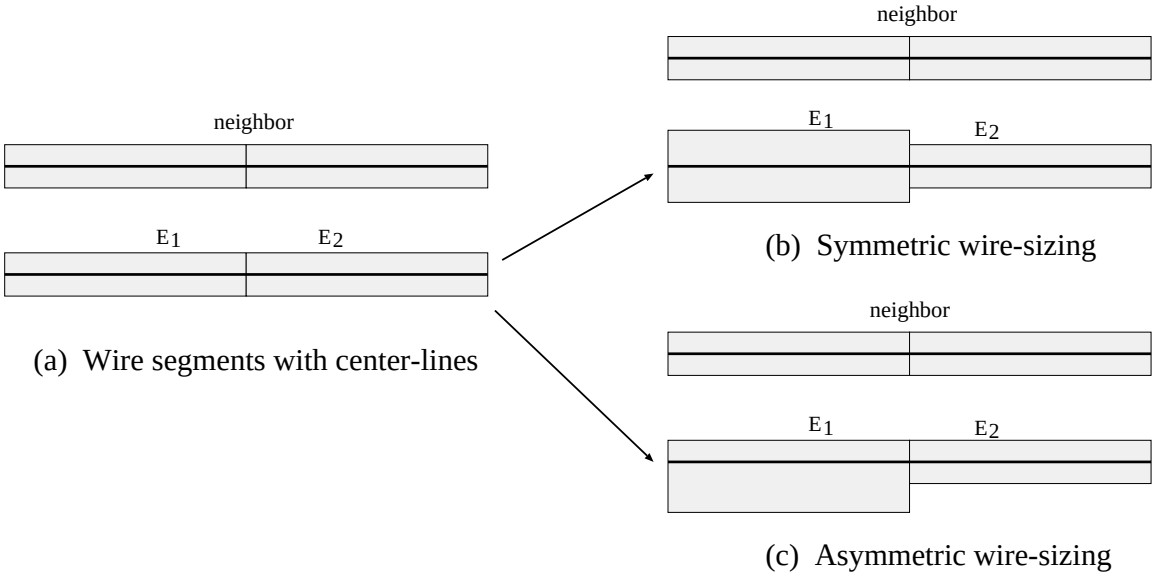

Figure 1: (a) Wire segments with center-lines. (b) Symmetric wire-sizing. (c) Asymmetric wire-sizing.

However, symmetric wire-sizing may be too restrictive for interconnect sizing and spacing, especially when coupling capacitance is considered. In this paper, we propose an *asymmetric wire-sizing* scheme in which we may widen or narrow above and below the center-line of the original wire segment asymmetrically, i.e, each wire segment has two pieces of wirewidth. Using the same example as in Figure 1(b), we would like E_1 to be farther away from its neighboring wire. As a result, we grow only the bottom half piece of the wire segment, keeping the top half intact, as shown in Figure 1(c). Let $w_E^{\downarrow}$ ($w_E^{\uparrow}$) represent the width of the wire below (above) a horizontal line segment. The new wire width is defined as $w_E = w_E^{\downarrow} + w_E^{\uparrow}$. An asymmetric wire-sizing solution is valid if $w_E^{\downarrow} \geq W_{min}/2$ and $w_E^{\uparrow} \geq W_{min}/2$. Note that for symmetric wire-sizing, $w_E^{\downarrow} = w_E^{\uparrow} = w_E/2$. To avoid introducing additional notation, we also use $w_E^{\downarrow}$ and $w_E^{\uparrow}$ to denote the asymmetric wire widths for the left and right parts of a vertical wire segment, respectively.

2.2 Interconnect Sizing and Spacing for Single Net

Given a layout of n routing trees T_i's, the interconnect sizing and spacing problem for a single net is to find a symmetric wire assignment $\mathcal{W} = \{w_{E_1^j}, \cdots, w_{E_{m_j}^j}\}$ or an asymmetric wire assignment $\mathcal{W} = \{w_{E_1^j} = (w_{E_1^j}^{\downarrow}, w_{E_1^j}^{\uparrow}), \cdots, w_{E_{m_j}^j} = (w_{E_{m_j}^j}^{\downarrow}, w_{E_{m_j}^j}^{\uparrow})\}$ for a routing tree of interest, say T_j, in order to optimize the following weighted delay objective (as used in [2]) with consideration of *the area, fringing* and *coupling* capacitances:

$$t_{T_j}(\mathcal{W}) \;=\; \sum_{k=1}^{m_j} \lambda_k^j \cdot t_{T_j}(s_k^j, \mathcal{W}), \tag{1}$$

where λ_k^j is the criticality of sink s_k^j in net $\mathcal{N}_j$, and $t_{T_j}(s_k^j, \mathcal{W})$ is the delay from source s_0^j to sink s_k^j in the routing tree T_j with wire-sizing solution $\mathcal{W}$.

We model the routing tree of each net by an RC tree and use the distributed Elmore delay model [1] to measure the interconnect delays for performance optimization. The formulations used in this section are similar to those in [2]. For clarity of presentation, we assume that a uniform grid structure is superimposed on the routing plane, and each wire segment in the routing plane is divided into a sequence of wires of unit length. Nonetheless, the results presented in this paper can be extended easily to the case where the wire segments are of non-uniform lengths in the same way as in [2].

Assume that the sheet resistance is r, the unit wire area capacitance coefficient c_a, the unit wire fringing capacitance coefficient c_f, and the unit wire lateral capacitance c_{xl}, then the wire resistance r_E and wire capacitance c_E for any grid edge E can be written as follows:

$$r_E = \frac{r}{w_E} \quad \text{and} \quad c_E = c_a \cdot w_E + c_f + c_{xl}(w_E, s_E^{\downarrow}, s_E^{\uparrow})$$

Note that $c_{xl}(w_E, s_E^{\downarrow}, s_E^{\uparrow})$ depends on the spacings $s_E^{\downarrow}$ and $s_E^{\uparrow}$ between E and its lower and upper (or left and right) neighboring wire segments, respectively, whereas c_a and c_f are assumed constants depending only the technology [2].

We now define for each grid edge E, the *effective-fringing capacitance coefficient* $c_{ef}(E) = c_f + c_{xl}(w_E, s_E^{\downarrow}, s_E^{\uparrow})$ which incorporates the lateral coupling capacitance. It shall be clear later on that this set of effective-fringing capacitance coefficients for all edges allows us to capture both the fringing capacitance and the lateral coupling capacitance effectively.

Given a grid edge E, we use $Des(E)$ to denote the set of grid edges in the subtree rooted at E (excluding E), and $Ans(E)$ to denote the set of grid edges $\{E' | E \in Des(E')\}$ (again, excluding E). Also, we use $sink(E)$ to denote the set of sinks in the subtree rooted at E, and C_E to denote the *total* capacitance in the subtree rooted at E (including both the wire capacitances and the sink capacitances):

$$C_E = \sum_{s_k \in sink(E)} c_{s_k} + \sum_{E' \in Des(E)} (c_a \cdot w_{E'} + c_{ef}(E'))$$

Furthermore, $sink(T_j)$ denotes the set of sinks, $P_{T_j}(u, v)$ denotes the unique path from u to v for any grid points u, v in T_j, and R_j denotes the driver resistance of the routing tree T_j of interest. The distributed Elmore delay for s_k^j from the source s_0^j is given by:

$$t_{T_j}(s_k^j, \mathcal{W}) = R_j \cdot \left(\sum_{E \in T_j} c_E + \sum_{s_k \in sink(T_j)} c_{s_k} \right) + \sum_{E \in P_{T_j}(s_0^j, s_k^j)} r_E \cdot (\frac{c_E}{2} + C_E) \tag{2}$$

[2] In fact, in deep sub-micron designs, c_a and c_f are no longer constants. Their values depend on the width and spacings. A more general notation should be $c_a(w_E, s_E^{\downarrow}, s_E^{\uparrow})$ and $c_f(w_E, s_E^{\downarrow}, s_E^{\uparrow})$. Our GISS algorithm for single-net optimization (Section 3) is able to handle this general capacitance model. The optimality of our bound computation algorithm for multiple nets (Section 4), however, assumes that both c_a and c_f are constants. Its extension for more general 2D capacitance model is discussed in Section 4.3.

Let $\lambda_k^j \geq 0$ be the criticality of sink s_k^j in T_j. Let $\lambda(s_0^j) = \sum_{s_k^j \in sink(T_j)} \lambda_k^j$ and $\lambda(E) = \sum_{s_k^j \in sink(E)} \lambda_k^j$, the performance measure $t_{T_j}(\mathcal{W})$ of T_j can be re-written as:

$$\begin{aligned} t_{T_j}(\mathcal{W}) &= \sum_{s_k^j \in sink(T_j)} \lambda_k^j \cdot \left\{ R_j \cdot \left(\sum_{E \in T_j} c_E + \sum_{s_k^j \in sink(T_j)} c_{s_k^j} \right) + \sum_{E \in P_{T_j}(s_0^j, s_k^j)} r_E \cdot (\frac{c_E}{2} + C_E) \right\} \\ &= \lambda(s_0^j) \cdot R_j \cdot \sum_{E \in T_j} (c_a \cdot w_E + c_{ef}(E)) + \\ &\quad \sum_{E \in T_j} \lambda(E) \cdot \frac{r}{w_E} \cdot \left\{ \frac{c_a \cdot w_E + c_{ef}(E)}{2} + \right. \\ &\quad \left. \sum_{s_k^j \in sink(E)} c_{s_k^j} + \sum_{E' \in Des(E)} (c_a \cdot w_{E'} + c_{ef}(E')) \right\} \end{aligned} \tag{3}$$

Note that if we treat $\lambda(s_0) \cdot R$ as the effective driver resistance and $\lambda(E) \cdot \frac{r}{w_E}$ as the effective wire resistance of edge E, then Eqn. (3) is very similar to Eqn. (2).

Note that we focus on the objective of minimizing the weighted sum of sink delays as in [2]. A previous work [13] showed that by assigning appropriate criticality/weight of each sink based on Lagrangian relaxation, the weighted-sum formulation can be used iteratively to meet the required arrival times.

2.3 Global Interconnect Sizing and Spacing for Multiple Nets

In the global interconnect sizing and spacing problem for multiple nets, again, we assume that an initial layout of n routing trees T_i's is given. With consideration of the area, fringing and coupling capacitances, the GISS problem for multiple nets is to find a symmetric wire assignment $\mathcal{W} = \{w_{E_1^1}, \cdots, w_{E_{m_1}^1}, \cdots, w_{E_1^n}, \cdots, w_{E_{m_n}^n}\}$ or an asymmetric wire assignment $\mathcal{W} = \{w_{E_1^1} = (w_{E_1^1}^{\downarrow}, w_{E_1^1}^{\uparrow}), \cdots, w_{E_{m_1}^1} = (w_{E_{m_1}^1}^{\downarrow}, w_{E_{m_1}^1}^{\uparrow}), \cdots w_{E_1^n} = (w_{E_1^n}^{\downarrow}, w_{E_1^n}^{\uparrow}), \cdots, w_{E_{m_n}^n} = (w_{E_{m_n}^n}^{\downarrow}, w_{E_{m_n}^n}^{\uparrow})\}$ for all T_i's such that, the summation of the weighted performance measure of all nets, i.e.,

$$t(\mathcal{W}) = \sum_{j=1}^{n} \delta_j t_{T_j}(\mathcal{W}) \tag{4}$$

is minimized, where δ_j indicates the criticality of net j. This delay formulation is similar to [16].

2.4 2D Capacitance Model

A table-based 2.5D capacitance model suitable for layout optimization was presented in [14] recently, where the lumped capacitance for a wire contains the following components: area and fringing capacitances, lateral coupling capacitance, and cross-over and cross-under capacitances. Based on this model, we consider only area, fringing and lateral coupling capacitances in this paper, since they are the major part of the lumped capacitance. That is, we use a 2D capacitance model simplified from the original 2.5D model. We first use 3D field solver to build tables for area, fringing and lateral coupling capacitances under different

width and spacing combinations. During layout optimization, we generate area, fringing and lateral coupling capacitances from pre-built tables. Details and justification of this method can be found in [14].

3 Optimal Sizing and Spacing for Single Net

The optimal wire sizing and spacing problem for a single net with fixed surrounding wire segments can be solved by adapting the bottom-up dynamic programming(DP)-based buffer insertion and wire-sizing algorithm proposed by [3]. Note that in [3], the objective function is to minimize the maximum delay or to meet arrival time requirements, while our objective is to minimize the weighted sum of all sink delays, which is similar to that in [15]. The major differences of the bottom-up dynamic programming part between this paper and [15] are: (1) we include lateral coupling capacitance between neighboring wires for delay calculation; (2) for the more general asymmetric wire sizing and spacing formulation, we keep two-piece ($w_E^{\downarrow}$ and $w_E^{\uparrow}$) information for each grid edge while performing bottom-up accumulation and top-down pruning. A simple flow of the algorithm is given as follows. Other details about the DP-based algorithm can be found in [3] and [15].

Each edge E in our optimal bottom-up wire sizing and spacing algorithm for single net is associated with a set of (c, t) pairs, called *options*. Let T_E denote the subtree rooted at the upstream end-point of E. Each (c, t) pair of E corresponds to a wire sizing and spacing solution for T_E, with c being the total capacitance of T_E, and t the performance measure (i.e., the weighted sum of sink delays from the upstream end-point of E) of T_E. Similarly, each node v is also associated with a set of (c, t) pairs defined in a similar manner for the subtree rooted at v.

The algorithm performs optimal wire sizing and spacing for a single net in a bottom-up fashion, starting from the sinks. At the beginning, each sink is assigned with a (c, t), with c being its loading capacitance, and $t = 0$. We consider the sizing of an edge $E = uv$ as follows: Let (c', t') be an option of the subtree rooted at node v, the downstream end-point of E. For a particular candidate wire width W of E, we can compute the corresponding option (c, t) of E as follows:

$$c = c_E + c'$$

$$t = \lambda(E) \cdot r_E \cdot \left(\frac{c_E}{2} + c'\right) + t'$$

Note that r_E and c_E are wire resistance and the total capacitance (including lateral coupling capacitance, wire area and fringing capacitances) of E for a wire width W, respectively. In the GISS problem for single net, only the wire widths of the net of interest is changeable, and the layout of other nets is fixed. Therefore, given a particular candidate width W for edge E (possibly symmetric and asymmetric), one can calculate the spacings between edge E and its neighbors easily. The wire width and spacing information is then passed to the 2D capacitance model to calculate the total wire capacitance. Suppose E has r candidate widths (symmetric or asymmetric), and node v has k options, we compute in total $r \times k$ options for E. On the other hand, if we have

one option (c', t') of edge $E = uv$ and and the other option (c'', t'') of edge $E' = uw$, then the corresponding option (c, t) of node u is simply calculated as follows:

$$c = c' + c''$$

$$t = t' + t''$$

Similarly, if E has I options and E' has J options, then u will have $I \times J$ options.

As in [15], it is observed that for two options (c, t) and (c', t') at a particular node or edge, if $c \leq c'$ and $t' \geq t$, then (c', t') is sub-optimal. In other words, the wire sizing and spacing solution corresponding to (c', t') is *redundant*, and can be pruned from the set of options of the node or edge. We apply the pruning rule as we enumerate all irredundant wire sizing and spacing solutions for the net in the bottom-up computation.

At the end of the bottom-up computation of (c, t) pairs, the root have a set of irredundant solutions. The optimal solution is achieved by choosing the (c, t) pair with the smallest t at the root, and tracing back from the optimal (c, t) pair, we obtain the corresponding optimal wire sizing and spacing solution that leads to this optimal option for the net.

Note that in the case of single net optimization, we do not have to assume constant wire area capacitance and fringing capacitance coefficients. In other words, the single-net bottom-up dynamic programming-based wire sizing and spacing algorithm is still optimal under the more general capacitance model.

The single net wire-sizing and spacing can be used for the post-layout optimization for a single critical net. However, this optimization will largely depend on the previous layout of other neighboring nets. And also since many critical nets may share the limited routing resource, just optimizing one net may indeed sacrifice the performance of other critical nets. In the next section, we will look into the global layout optimization for multiple nets.

4 Global Interconnect Sizing and Spacing for Multiple Nets

The difficulty of the GISS problem for multiple nets arises from the fact that the lateral coupling capacitance coefficient for each wire segment changes with the width and spacings. Moreover, there is no closed form representation for lateral coupling capacitance. The key to solving the multiple-net wire sizing and spacing problem is the *effective-fringing property* of wire-sizing solutions under different spacing conditions. The beauty of this property is that we are able to reduce the GISS problem with variable lateral coupling capacitance to an optimal wire-sizing problem with consideration of only constant area capacitance coefficient and different effective-fringing capacitance coefficients for different wire segments. Such a reduction allows us to compute *global* upper and lower bounds of the optimal wire sizing and spacing solution for *all* nets. In the following, we first state the symmetric and asymmetric effective-fringing properties and discuss their implications. Then, we will describe the bound

computation algorithm, followed by a refinement algorithm to obtain the final global interconnect sizing and spacing solution when the lower and upper bounds computed as above do not meet. Extensions to more general 2D capacitance models will then be discussed.

4.1 Effective-Fringing Property: Theorems and Implications

First, we consider the case of symmetric GISS. We define the dominance relation between symmetric wire-sizing solutions of a routing tree in the same way as in [2]:

Definition 1 Symmetric Dominance Relation: *Given two wire width assignments $\mathcal{W}$ and $\mathcal{W}'$, let w_E be the width assignment of edge E in $\mathcal{W}$ and w'_E be the wire width of E in $\mathcal{W}'$. Then, $\mathcal{W}$* dominates *$\mathcal{W}'$ ($\mathcal{W} \geq \mathcal{W}'$) if for any segment E, $w_E \geq w'_E$.*

In the following, we consider an optimization problem called *optimal wire-sizing under variable effective-fringing coefficients (OWS-EF)*. While we still assume a constant area capacitance coefficient c_a, we now define for each wire segment E the *effective-fringing capacitance coefficient* $c_{ef}(E) = c_f + c_{xl}(w_E, s_E^{\downarrow}, s_E^{\uparrow})$ which incorporates the lateral coupling capacitance. It shall be clear later on that this set of effective-fringing capacitance coefficients for all edges allows us to capture the lateral coupling capacitance effectively. The performance measure that we aim at optimizing for OWS-EF problem is the same as in Eqn. (1) except that c_f is replaced by $c_{ef}(E)$ and c_{xl} disappears. Let $\mathcal{C}_{ef}$ denote the set of effective-fringing capacitance coefficients $c_{ef}(E)$'s for all edges in T. We define $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$ if $c_{ef}(E) \geq c'_{ef}(E)$ for every E in T. Then the symmetric effective-fringing property can be stated as follows:

Theorem 1 Symmetric Effective-Fringing Property: *For the same routing tree T and a constant c_a, let $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ be an optimal wire-sizing solution to the OWS-EF problem under a set of variable effective-fringing capacitance coefficients $\mathcal{C}_{ef} = \{c_{ef}(E) \mid E \in T\}$, and $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef})$ be an optimal sizing solution under a different set of $\mathcal{C}'_{ef} = \{c'_{ef}(E) \mid E \in T\}$. Then if $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$, there exist optimal solutions such that $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ dominates $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef})$.*

The proof of this theorem can be found at the appendix. The theorem can be used very effectively to determine the upper and lower bounds of the original optimal GISS problem. Suppose $\mathcal{W}^*$ denotes the global optimal wire-sizing solution optimizing t_T. Let $\mathcal{S}^{\downarrow *}$ and $\mathcal{S}^{\uparrow *}$ denote the spacings obtained based on $\mathcal{W}^*$, and $c_{xl}(w_E^*, s_E^{\downarrow *}, s_E^{\uparrow *})$ be the lateral coupling capacitance coefficient for each edge E based on $\mathcal{W}^*$, $\mathcal{S}^{\downarrow *}$, and $\mathcal{S}^{\uparrow *}$. Let $\mathcal{W}^{\downarrow U}$ and $\mathcal{W}^{\uparrow U}$ be upper bounds of $\mathcal{W}^{\downarrow *}$ and $\mathcal{W}^{\uparrow *}$, and $\mathcal{S}^{\downarrow L}$ and $\mathcal{S}^{\uparrow L}$ be lower bounds of $\mathcal{S}^{\downarrow *}$ and $\mathcal{S}^{\uparrow *}$, respectively. Then $c_{xl}(w_E^U, s_E^{\downarrow L}, s_E^{\uparrow L}) \geq c_{xl}(w_E^*, s_E^{\downarrow *}, s_E^{\uparrow *})$, as the lateral coupling capacitance coefficient decreases when the width of E decreases and the spacings between E and its neighbors increases.

Now consider two instances of the OWS-EF problem. In the first instance, the effective-fringing capacitance coefficient of edge E is $c_{ef}(E) = c_f + c_{xl}(w_E^U, s_E^{\downarrow L}, s_E^{\uparrow L})$. In the second instance, the effective-fringing capacitance coefficient of edge E

is $c'_{ef}(E) = c_f + c_{xl}(w^*_E, s^{\downarrow *}_E, s^{\uparrow *}_E)$. Clearly, $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$. From the symmetric effective-fringing property, the optimal solution $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ dominates the optimal solution $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef})$. Note that $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef}) = \mathcal{W}^*$. Therefore, $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ is also an upper bound of the optimal solution $\mathcal{W}^*$. This procedure can be applied to compute wire width upper bounds (equivalently, spacing lower bounds) for *all* nets.

Similarly, suppose we are given a lower bound of the optimal wire-sizing solution, denoted $\mathcal{W}^L$. From $\mathcal{W}^L$, we can calculate a spacing upper bound $\mathcal{S}^U$. Now, applying the optimization process for the OWS-EF problem as in the above discussion, $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ will be dominated by $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef}) = \mathcal{W}^*$, since $\mathcal{C}_{ef} \leq \mathcal{C}'_{ef}$. In other words, we have computed a lower bound of the optimal solution.

For asymmetric GISS, we can define

Definition 2 Asymmetric Dominance Relation:

Given two wire width assignments $\mathcal{W} = (\mathcal{W}^{\downarrow}, \mathcal{W}^{\uparrow})$ and $\mathcal{W}' = (\mathcal{W}^{\downarrow'}, \mathcal{W}^{\uparrow'})$, let $w_E = (w^{\downarrow}_E, w^{\uparrow}_E)$ be the width assignment of edge E in $\mathcal{W}$ and $w'_E = (w^{\downarrow}_E{}', w^{\uparrow}_E{}')$ be the wire width of E in $\mathcal{W}'$. Then, $\mathcal{W}$ dominates *$\mathcal{W}'$ if for any segment E, $w^{\downarrow}_E \geq w^{\downarrow}_E{}'$ and $w^{\uparrow}_E \geq w^{\uparrow}_E{}'$ for any edge E, respectively.*

Then, the asymmetric effective-fringing property can be stated as follows:

Theorem 2 Asymmetric Effective-Fringing Property:[3] *For the same routing tree and a constant c_a, let $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}_{ef}, \mathcal{W}^{\downarrow})$ be an optimal asymmetric wire-sizing solution to the OWS-EF problem with a fixed $\mathcal{W}^{\downarrow}$ and a set of effective-fringing capacitance coefficients $\mathcal{C}_{ef}$, and $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}'_{ef}, \mathcal{W}^{\downarrow'})$ be an optimal sizing solution under another fixed $\mathcal{W}^{\downarrow'}$ and a different set of $\mathcal{C}'_{ef}$. Then if $\mathcal{W}^{\downarrow} \leq \mathcal{W}^{\downarrow'}$ and $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$, there exist optimal solutions $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}_{ef}, \mathcal{W}^{\downarrow})$ dominates $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}'_{ef}, \mathcal{W}^{\downarrow'})$.*

Proof of Theorem 2: Consider two OWS-EF problems under the same c_a, but different $\mathcal{C}_{ef}$ and $\mathcal{C}'_{ef}$ with $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$. From Theorem 1, we conclude that there exist two optimal solutions $\hat{\mathcal{W}}$ and $\hat{\mathcal{W}}'$ for them respectively, such that $\hat{\mathcal{W}}$ dominates $\hat{\mathcal{W}}'$, i.e., $w^{\downarrow} + w^{\uparrow} \geq w'^{\downarrow} + w'^{\uparrow}$ for each wire segment if we view each wire segment as two pieces. Now consider the two optimal solutions under the two-piece width formulation with same $\mathcal{C}_{ef}$ and $\mathcal{C}'_{ef}$ as above, since we have $\mathcal{W}^{\downarrow'}$ dominates $\mathcal{W}^{\downarrow}$, i.e., $w^{\downarrow'} \geq w^{\downarrow}$ for each wire segment, combined with $w^{\downarrow} + w^{\uparrow} \geq w^{\downarrow'} + w^{\uparrow'}$, we obtain $w^{\uparrow} \geq w^{\uparrow'}$ for each wire segment, and therefore conclude that there exist two optimal solutions such that $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}_{ef}, \mathcal{W}^{\downarrow})$ dominates $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}'_{ef}, \mathcal{W}^{\downarrow'})$. □

We can also apply the asymmetric effective-fringing property to compute global upper and lower bounds of the optimal wire sizing and spacing solution by solving asymmetric OWS-EF problem. From an upper bound $(\mathcal{W}^{\downarrow U}, \mathcal{W}^{\uparrow U})$, we can again compute lower bound spacings $\mathcal{S}^{\downarrow L}$ and $\mathcal{S}^{\uparrow L}$, and set of lateral coupling capacitance coefficients $c_{xl}((w^{\downarrow U}_E, w^{\uparrow U}_E), s^{\downarrow L}_E, s^{\uparrow L}_E)$'s.

[3] This is the corrected version of what has been presented on the Proceeding of IEEE/ACM 1997 International Conference on Computer Aided Design, Nov. 9-13, San Jose, CA.

Similarly, we can compute another set of lateral coupling capacitance coefficients, $c_{xl}((w_E^{\downarrow *}, w_E^{\uparrow *}), s_E^{\downarrow *}, s_E^{\uparrow *})$'s from an optimal wire-sizing solution $\mathcal{W}^* = (\mathcal{W}^{\downarrow *}, \mathcal{W}^{\uparrow *})$.

We denote $c_{ef}(E) = c_f + c_{xl}((w_E^{\downarrow U}, w_E^{\uparrow U}), s_E^{\downarrow L}, s_E^{\uparrow L})$ and $c'_{ef}(E) = c_f + c_{xl}((w_E^{\downarrow *}, w_E^{\uparrow *}), s_E^{\downarrow *}, s_E^{\uparrow *})$ as before. By the asymmetric effective-fringing property, $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}_{ef}, \mathcal{W}^{\downarrow L})$ dominates $\hat{\mathcal{W}}^{\uparrow}(c_a, \mathcal{C}'_{ef}, \mathcal{W}^{\downarrow *}) = \mathcal{W}^{\uparrow *}$, and therefore, it is still an upper bound of $\mathcal{W}^{\uparrow *}$, the optimal wire-sizing for the top or right portion of each edge. Similar argument applies for the lower bounds and for the bottom (or left) portion of each edge.

4.2 Algorithm for Upper and Lower Bound Computation

The effective-fringing properties (both symmetric and asymmetric) lead to very effective algorithms to compute the upper and lower bounds of the optimal wire sizing and spacing solution for all nets under consideration.

For the symmetric wire sizing and spacing, an upper and lower bound computation algorithm based on the symmetric effective-fringing property is given in Figure 2. Notice that for the symmetric case, each wire segment just has one piece of wire width.

Upper and Lower Bound Computation (Symmetric wire-sizing)

$i \leftarrow 0$
$\mathcal{W}_U(i) \leftarrow$ `Initialize Wire Width Upper Bound`
$\mathcal{W}_L(i) \leftarrow$ `Initialize Wire Width Lower Bound`
do
 `/* Upper bound computation */`
 $\mathcal{C}_{xl}^U(i) \leftarrow$ `Compute Lateral Coefficient`$(\mathcal{W}_U(i))$
 $\mathcal{C}_{ef}^U(i) \leftarrow$ `Compute Effective-Fringing Coefficient`$(\mathcal{C}_{xl}^U(i))$
 $\mathcal{W}_U(i+1) \leftarrow$ `DPW`$(\mathcal{C}_{ef}^U(i))$ `/* for all nets */`
 `/* Lower bound computation */`
 $\mathcal{C}_{xl}^L(i) \leftarrow$ `Compute Lateral Coefficient`$(\mathcal{W}_L(i))$
 $\mathcal{C}_{ef}^L(i) \leftarrow$ `Compute Effective-Fringing Coefficient`$(\mathcal{C}_{xl}^L(i))$
 $\mathcal{W}_L(i+1) \leftarrow$ `DPW`$(\mathcal{C}_{ef}^L(i))$ `/* for all nets */`
 $i \leftarrow i + 1$
while $(\mathcal{W}_U(i) \neq \mathcal{W}_U(i-1)$ OR $\mathcal{W}_L(i) \neq \mathcal{W}_L(i-1))$

Figure 2: Algorithm to compute upper and lower bounds of the global optimal symmetric wire-sizing solution for multiple nets.

For the asymmetric wire sizing and spacing, an iterative upper and lower bound computation algorithm based on the asymmetric effective-fringing property is given in Figure 3. Notice that we have a two-piece width for each wire segment. Since the overall flow for bound computation of symmetric and asymmetric cases is similar, we will explain the asymmetric case (which is more complicated) in detail in the following. The algorithm starts at the iteration $i = 0$. First we initialize upper and lower bounds of all wire widths specified by the layout constraints. A sample initialization is shown in Figure 4. Let E_l and E_u be two

parallel horizontal edges, with E_l below E_u. Let W_{min} be the minimum wire width, and S_{min} be the minimum spacing between two parallel wires from the layout constraints. If the distance between the center-lines of E_l and E_u is d, then the maximum width (i.e., the initial upper bound) for $w^{\uparrow}_{E_l}$ (the side closer to E_u) and $w^{\downarrow}_{E_u}$ (the side closer to E_l) is $d - W_{min}/2 - S_{min}$.

Upper and Lower Bound Computation (Asymmetric wire-sizing)

$i \leftarrow 0$
$(\mathcal{W}^{\downarrow}_U(i), \mathcal{W}^{\uparrow}_U(i)) \leftarrow$ `Initialize Wire Width Upper Bound`
$(\mathcal{W}^{\downarrow}_L(i), \mathcal{W}^{\uparrow}_L(i)) \leftarrow$ `Initialize Wire Width Lower Bound`
do
`/* Upper bound computation */`
$\mathcal{C}^U_{xl}(i) \leftarrow$ `Compute Lateral Coefficient`$(\mathcal{W}^{\downarrow}_U(i), \mathcal{W}^{\uparrow}_U(i))$
$\mathcal{C}^U_{ef}(i) \leftarrow$ `Compute Effective-Fringing Coefficient`$(\mathcal{C}^U_{xl}(i))$
$\mathcal{W}_U(i+1) \leftarrow$ Compute Upper-Bound Lumped Width `DPW`$(\mathcal{C}^U_{ef}(i))$
$\mathcal{W}^{\downarrow}_U(i+1) \leftarrow \mathcal{W}_U(i+1) - \mathcal{W}^{\uparrow}_L(i)$
$\mathcal{W}^{\uparrow}_U(i+1) \leftarrow \mathcal{W}_U(i+1) - \mathcal{W}^{\downarrow}_L(i)$
`/* Lower bound computation */`
$\mathcal{C}^L_{xl}(i) \leftarrow$ `Compute Lateral Coefficient`$(\mathcal{W}^{\downarrow}_L(i), \mathcal{W}^{\uparrow}_L(i))$
$\mathcal{C}^L_{ef}(i) \leftarrow$ `Compute Effective-Fringing Coefficient`$(\mathcal{C}^L_{xl}(i))$
$\mathcal{W}_L(i+1) \leftarrow$ Compute Lower-Bound Lumped Width `DPW`$(\mathcal{C}^L_{ef}(i))$
$\mathcal{W}^{\downarrow}_L(i+1) \leftarrow max(W_{min}, \mathcal{W}_L(i+1) - \mathcal{W}^{\uparrow}_U(i+1))$
$\mathcal{W}^{\uparrow}_L(i+1) \leftarrow max(W_{min}, \mathcal{W}_L(i+1) - \mathcal{W}^{\downarrow}_U(i+1))$
$i \leftarrow i+1$
while $((\mathcal{W}^{\downarrow}_U(i), \mathcal{W}^{\uparrow}_U(i)) \neq (\mathcal{W}^{\downarrow}_U(i-1), \mathcal{W}^{\uparrow}_U(i-1))$ OR $(\mathcal{W}^{\downarrow}_L(i), \mathcal{W}^{\uparrow}_L(i)) \neq (\mathcal{W}^{\downarrow}_L(i-1), \mathcal{W}^{\uparrow}_L(i-1)))$

Figure 3: Algorithm to compute upper and lower bounds of the global optimal asymmetric wire-sizing solution for multiple nets.

From the upper bound $(\mathcal{W}^{\downarrow}_U, \mathcal{W}^{\uparrow}_U)$, we compute the upper bound effective-fringing capacitance coefficients. Again, consider E_l and E_u which are of distance d. Let $w^{\uparrow U}_{E_l}$ be the width of E_l in $\mathcal{W}^{\uparrow}_U$, and $w^{\downarrow U}_{E_u}$ the width of E_u in $\mathcal{W}^{\downarrow}_U$. If $d - w^{\uparrow U}_{E_l} - w^{\downarrow U}_{E_u} < S_{min}$, then, the upper bound wire widths overlap and we assign the lower bound spacing between E_l and E_u to be S_{min}, i.e., $s^{\uparrow L}_{E_l} = s^{\downarrow L}_{E_u} = S_{min}$. Otherwise, the lower bound spacings $s^{\uparrow L}_{E_l}$ and $s^{\downarrow L}_{E_u}$ are $d - w^{\uparrow U}_{E_l} - w^{\downarrow U}_{E_u}$. Similarly, for E_l and its lower neighbor we compute $s^{\downarrow L}_{E_l}$. From $s^{\uparrow L}_{E_l}$ and $s^{\downarrow L}_{E_l}$, we can compute $c_{xl}((w^{\downarrow U}_{E_l}, w^{\uparrow U}_{E_l}), s^{\downarrow L}_{E_l}, s^{\uparrow L}_{E_l})$. Let $\mathcal{C}^U_{xl}$ denote such set of lateral coupling capacitance coefficients obtained from $(\mathcal{W}^{\downarrow}_U, \mathcal{W}^{\uparrow}_U)$. We then compute the effective-fringing coefficient $c_{ef}(E_l) = c_f + c_{xl}((w^{\downarrow U}_{E_l}, w^{\uparrow U}_{E_l}), s^{\downarrow L}_{E_l}, s^{\uparrow L}_{E_l})$. Similarly we can calculate the upper bound $c_{ef}(E_u)$. We refer to the set of upper bound $c_{ef}(E)$ for all edges based on $\mathcal{C}^U_{xl}$ as $\mathcal{C}^U_{ef}$.

We then perform the following iterative process to update the wire width upper bounds. First we compute $\mathcal{W}_U(i+1)$ by using the bottom-up dynamic programming-based wire-sizing (DPW) algorithm outlined in Section 3 to each net with fixed $\mathcal{C}^U_{ef}(i)$, without explicitly dealing with lateral coupling capacitance. Then we deduct the lower bound $\mathcal{W}^{\uparrow}_L(i)$ from the above upper bound lumped width for each wire segment and get $\mathcal{W}^{\downarrow}_U(i+1)$. Similarly, we can get $\mathcal{W}^{\uparrow}_U(i+1)$.

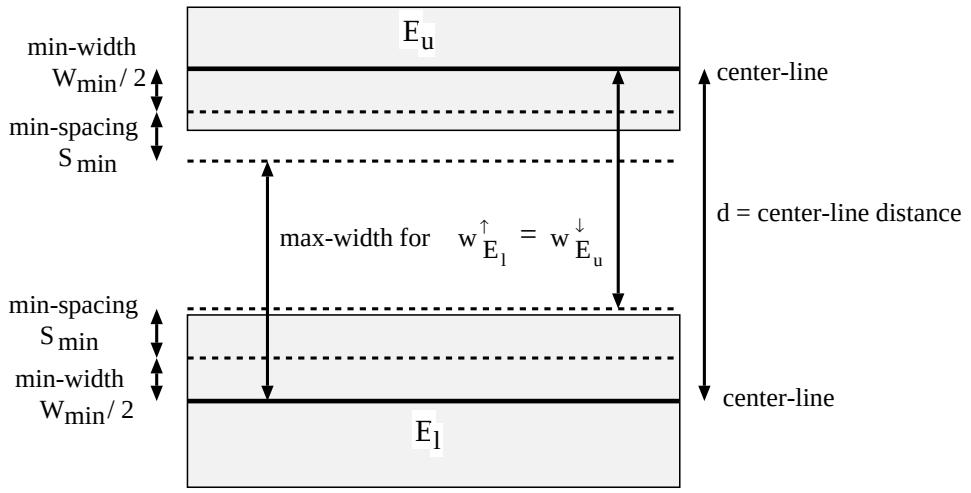

Figure 4: Initialization of upper-bound wire widths.

For the lower bound computation, the process is similar. We use the lower bound wire width for each wire segment $(\mathcal{W}_L^{\downarrow}(i), \mathcal{W}_L^{\uparrow}(i))$, and compute $\mathcal{C}_{xl}^L(i)$, a set of lower bound lateral capacitance coefficients. Subsequently, $\mathcal{C}_{ef}^L(i)$ is computed from $\mathcal{C}_{xl}^L(i)$. We then apply the DPW with fixed $\mathcal{C}_{ef}^L$ and obtain the new lower bound lumped width $\mathcal{W}_L(i+1)$. Deduct from it the upper bound $\mathcal{W}_U^{\uparrow}(i+1)$, we get $\mathcal{W}_L^{\downarrow}(i+1)$. Similarly, we can get $\mathcal{W}_L^{\uparrow}(i+1)$.

This interleaved upper and lower bound computation is iterated until $(\mathcal{W}_U^{\downarrow}(i), \mathcal{W}_U^{\uparrow}(i))$ is identical to $(\mathcal{W}_U^{\downarrow}(i+1), \mathcal{W}_U^{\uparrow}(i+1))$, and $(\mathcal{W}_L^{\downarrow}(i), \mathcal{W}_L^{\uparrow}(i))$ is identical to $(\mathcal{W}_L^{\downarrow}(i+1), \mathcal{W}_L^{\uparrow}(i+1))$, i.e., we cannot get further improvement from the bound computations. Our experiments show that the upper and lower bound widths often meet or become close for most wire segments in a few iterations. So we will get near optimal GISS solution from the bound computations. We note that a brute-force lower bound computation may lead to adjacent wire overlapping if the lower bound widths between these wires overlap. To avoid this scenario, we need to add some constraint such that the bound computation will always give valid lower and upper bounds. This is an inherent problem for some multiple nets when they compete intensively for very limited routing resources.

When the upper and lower bounds do not meet, we will use the following refinement algorithm to obtain the final wire sizing and spacing solution for each net: We first take the lower bound of each side for each wire segment as our initial layout. Then we will iteratively perform single net wire sizing and spacing optimization method presented in Section 3 to obtain the final GISS solution following the order of each net's priority. We call the overall bound computations and final refinement algorithm GISS/FAF, where FAF denotes the fixed area and fringing capacitance coefficients.

4.3 Extension to Variable Area and Fringing Capacitance Coefficients

The optimality of bound computation in the above GISS/FAF algorithm is based on the effective-fringing properties which assume the area capacitance coefficient c_a and the fringing capacitance coefficient c_f are constants independent of wire widths and spacings. However, in deep submicron designs, similar to the lateral coupling capacitance c_{xl}, c_a and c_f are dependent on wire widths and spacings (e.g., there are about 30% variations on c_a and c_f values in our 2D capacitance tables). Nevertheless, the GISS algorithm can still be used in this case simply by computing the area and fringing capacitances from the general 2D model directly during the bottom up dynamic programming optimization. However, the effective-fringing properties cannot be used to guarantee that the optimal solution is always within the upper and lower bounds computed by the GISS algorithm. We call the algorithm using variable c_a and c_f's as GISS/VAF. Experimental results in Section 5.2 show that GISS/VAF often achieves better results when compared with GISS/FAF.

5 Experimental Results

We have implemented GISS using C++ under the Sun SPARC station environment. In this section, we present the experimental results. The parameters used in our experiments are based on the $0.18\mu m$ technology specified in the SIA roadmap [10]. The sheet resistance is 0.0638 $\Omega/\Box$. The minimum wire sizing W_{min} is $0.22\mu m$ and minimum spacing S_{min} between neighboring wires is $0.33\mu m$. Then, $pitch$ spacing, defined as the sum of minimum spacing and minimum wire size, is equal to $0.55\mu m$. The allowable wire widths for each side along the center line are from 0.11 to 1.1 μm, with the incremental step to be 0.11 μm. The area, fringing and lateral coupling capacitances are obtained by a look-up table obtained through the 2D capacitance extraction model [14]. The driver effective resistance is 119 Ω. The input capacitance for each sink is set to be 12.0fF.

5.1 Optimal Sizing and Spacing for a Single Net

We perform experiments for the optimal single-net sizing and spacing algorithm on 5 nets provided by Intel. The routing trees are the same as used in [4]. These trees originally have multiple sources and we randomly assign one as the unique single source. We assign equal criticality for each sink so the weighted delay becomes the average delay. Given the initial layout of these five nets, we randomly assign some surrounding wire segments with spacing from the net being 1 to $5 \times pitch$.

In Table 2, we summarize the average and maximum HSPICE delays from different algorithms: minimum wire sizing (MIN); symmetric optimal wire-sizing (OWS-S) algorithm without considering the coupling capacitance (but coupling capacitance through the 2D model is included in its final HSPICE simulation); symmetric GISS algorithm (GISS-S) and asymmetric GISS algorithm (GISS-A). In the parentheses under OWS-S, GISS-S and GISS-A, we list the percentage of improvement over MIN. From the table, we can see that GISS-A consistently outperforms all other algorithms. In terms of its average delay, which

	length	Average Delay (ns)				Maximum Delay (ns)			
	(mm)	MIN	OWS-S	GISS-S	GISS-A	MIN	OWS-S	GISS-S	GISS-A
Net1	3.6	0.08	0.08 (-0.00%)	0.08 (-0.00%)	0.08 (-0.00%)	0.14	0.14 (-0.00%)	0.14 (-0.00%)	0.14 (-0.00%)
Net2	6.6	0.31	0.19 (-38.7%)	0.18 (-41.9%)	0.15 (-51.6%)	0.34	0.22 (-35.3%)	0.22 (-35.3%)	0.19 (-44.1%)
Net3	10.07	0.78	0.71 (-9.0%)	0.71 (-9.0%)	0.61 (-21.8%)	1.03	0.96 (-6.8%)	0.95 (-7.8%)	0.83 (-19.4%)
Net4	10.57	0.54	0.41 (-24.1%)	0.39 (-27.8%)	0.27 (-50.0%)	0.84	0.71 (-15.5%)	0.65 (-22.6%)	0.44 (-47.6%)
Net5	31.98	3.19	2.57 (-19.4%)	2.57 (-19.4%)	1.73 (-45.8%)	4.92	4.26 (-13.4%)	4.27 (-13.2%)	3.26 (-33.7%)

Table 2: Comparison of the average and maximum delays using different algorithms.

	Average Delay (ns)				Normalized wire width			
center spacing	MIN	OWS	GISS/FAF	GISS/VAF	MIN	OWS	GISS/FAF	GISS/VAF
$2 \times pitch$	1.51	1.26 (-16.6%)	0.81 (-46.4%)	0.80 (-47.0%)	1.00	2.90	3.07	3.29
$3 \times pitch$	1.33	0.73 (-45.1%)	0.57 (-57.1%)	0.52 (-60.9%)	1.00	4.65	4.76	4.70
$4 \times pitch$	1.28	0.46 (-64.1%)	0.46 (-64.1%)	0.42 (-67.2%)	1.00	6.20	6.11	6.00
$5 \times pitch$	1.25	0.38 (-69.6%)	0.39 (-68.8%)	0.37 (-70.4%)	1.00	6.90	6.63	7.17
$6 \times pitch$	1.23	0.35 (-71.5%)	0.36 (-70.7%)	0.34 (-72.4%)	1.00	6.90	6.73	7.68

Table 3: Comparison of average delays and normalized wire widths for a 16-bit parallel bus structure under 5 different pitch spacings using different algorithms.

is our objective function, the reduction is up to 51.6% compared with the MIN solution (Net2), and 34.1% with OWS-S (Net4) and 32.7% with GISS-S (Net5).

Although the average delay is our objective, experimental results show that this formulation reduces the maximum delays as well. From the table, we can see that GISS-A outperform MIN, OWS-S and GISS-S by up to 47.6%, 38.0% and 32.3% (Net5) compared with MIN, OWS-S and GISS-S respectively.

5.2 Optimal Sizing and Spacing for Multiple Nets

To demonstrate the effectiveness of GISS algorithm, we perform experiments for global optimal wire sizing and spacing for multiple nets on a 16-bit parallel bus structure of 10 mm long with the center distance between adjacent bus line set to be $\{2, 3, 4, 5, 6\} \times pitch$ respectively. Each wire segment is set to be 1000 μm (we also try the wire segment of 500 μm, the sizing result is almost the same.)

In Table 3, we give the average delays from HSPICE simulations and normalized wire widths (ratio of average wire size to W_{min}). We still list in the parentheses the percentage of delay reduction over MIN. In the table, column OWS uses single-net OWS in a net by net manner, column GISS/FAF uses the GISS algorithm with fixed c_a and c_f (obtained through the 2D table-look-up with $3 \cdot W_{min}$ width and $3 \cdot S_{min}$ spacing) to guide the layout optimization, whereas GISS/VAF directly uses the 2D

Figure 5: The OWS sizing result for the upper 4 bits bus lines of the $3 \times pitch$ bus structure.

model with variable area and fringing capacitance coefficients during the layout optimization. All these algorithms use the 2D model for final HSPICE simulations. The average running time for these 5 bus cases using GISS algorithm is 102 seconds.

From the table, we can see that the average delays of GISS/FAF outperform those of MIN by up to 70.7%, and outperform those of OWS by up to 35.7% respectively. Although GISS/VAF cannot guarantee optimality, our experiments do show that it can outperform GISS/FAF by up to 8.8%. This is due to that: (i) c_a and c_f are no longer constants for deep submicron design, (ii) we use the 2D model with variable c_a and c_f's for both HSPICE simulations, which GISS/VAF also uses during GISS optimization. It actually suggests that our GISS algorithm may indeed have the capability to handle more general capacitance models.

The OWS and GISS sizing results for a 4-bit bus structure with $3 \times pitch$ between adjacent lines are shown in Fig. 5 and Fig. 6, respectively. They are drawn using the MAGIC tool. The vertical dimension is scaled up by 1000x for better visual effect. We can see that OWS loses global optimality for multiple nets as it can only size those nets one by one, without consideration of the neighborhood structures and the coupling capacitance. However, GISS takes those factors into consideration and performs global optimization. Therefore, it leads to much better performance, in both average delay and maximimu delay.

It is also observed that for $5 \times pitch$ and $6 \times pitch$ center spacing, the improvement of GISS/VAF over OWS is very marginal. This is because the coupling capacitance becomes less important as spacing goes up. For example, the average edge to edge spacing for the $6 \times pitch$ is about $6 \times 0.55 - 7 \times 0.22 = 1.76\mu m$, but for the $2 \times pitch$ is about $2 \times 0.55 - 3 \times 0.22 = 0.44\mu m$

6 Discussions and Future Work

Our study has shown convincingly that it is very important to consider coupling capacitance into VLSI interconnect optimization for deep submicron designs. We have proposed two general formulations, symmetric and asymmetric, for the global interconnect

Figure 6: The GISS/VAF sizing result for the upper 4 bits bus lines of the $3 \times pitch$ bus structure.

sizing and spacing problem and revealed the effective-fringing properties for both symmetric and asymmetric scenarios. We develop an effective algorithm to compute the lower and upper bounds for the global optimal sizing and spacing solution. Our experiments show that the upper and lower bound widths often meet or become close in a few iterations if the lower bounds between adjacent wires do not overlap, so we will get near optimal GISS solution. To make sure that the lower bounds between adjacent wires do not overlap, we need to add some constraints such that the design rules will not be violated. Note that adding these constraints may limit the convergence of the lower and upper bound computation. However, as we observe, this is an inherent problem for some multiple nets when they compete intensively for very limited routing resources.

We prove the effective-fringing properties and derive the GISS algorithm under the assumption of fixed c_a and c_f. Our experiments indeed show that it is also very effective under variable c_a and c_f's. It suggests that the GISS algorithm actually have the capability to handle more general capacitance models. Further validation is planned as a future work.

An alternative for computing lower and upper bounds is to use the local refinement (*LR*) operations similar to those used in [2, 4, 15]. Preliminary results of this approach are being reported in [18]. It shows that the GISS problem under variable c_a and c_f's can be formulated as a general CH-posynomial program, which enables the application of the local refinement operations [16, 18] and leads to very efficient bound computation.

In the future, we plan to develop efficient noise models and extend both dynamic-programming based algorithm and LR-based algorithm for noise control and minimization.

Acknowledgments

The authors would like to thank Mosur K. Mohan, Krishnamurthy Soumyanath, Ganapati Srinivasa from Intel for their input and support of this project, and Kei-Yong Khoo, Patrick Madden at UCLA for their helpful discussions.

References

[1] W. C. Elmore, "The transient response of damped linear networks with particular regard to wide-band amplifiers," *Journal of Applied Physics*, vol. 19, no. 1, pp. 55–63, Jan. 1948.

[2] J. Cong and K. S. Leung, "Optimal wiresizing under the distributed Elmore delay model," *IEEE Trans. on Computer-Aided Design*, vol. 14, no. 3, pp. 321–336, Mar. 1995.

[3] J. Lillis, C. K. Cheng, and T. T. Y. Lin, "Simultaneous routing and buffer insertion for high performance interconnect," in *Proc. the Sixth Great Lakes Symp. on VLSI*, 1996.

[4] J. Cong and L. He, "Optimal wiresizing for interconnects with multiple sources," *ACM Trans. on Design Automation of Electronic Systems*, vol. 1, pp. 478–511, Oct. 1996.

[5] J. P. Fishburn and C. A. Schevon, "Shaping a distributed-RC line to minimize elmore delay," *IEEE Trans. on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 42, pp. 1020–1022, Dec., 1995.

[6] C. P. Chen, Y. P. Chen, and D. F. Wong, "Optimal wire-sizing formula under the Elmore delay model," in *Proc. Design Automation Conf.*, pp. 487–490, 1996.

[7] N. Menezes, S. Pullela, F. Dartu, and L. Pillage, "RC interconnect synthesis – a moment fitting appraoch," in *Proc. Int. Conf. Computer Aided Design*, pp. 418–425, 1994.

[8] T. Xue, E. Kuh, and Q. Yu, "A sensitivity-based wiresizing approach to interconnect optimization of lossy transmission line topologies," in *Proc. IEEE Multi-Chip Module Conf.*, pp. 117–121, 1996.

[9] J. Cong, L. He, C.-K. Koh, and P. H. Madden, "Performance optimization of vlsi interconnect layout," *Integration, the VLSI Journal*, vol. 21, pp. 1–94, 1996.

[10] Semiconductor Industry Association, *National Technology Roadmap for Semiconductors*. 1994.

[11] J. Cong and P. H. Madden, "Performance driven routing with multiple sources," in *Proc. IEEE Int. Symp. on Circuits and Systems*, pp. 1.203–1.206, 1995.

[12] T. Okamoto and J. Cong, "Buffered Steiner tree construction with wire sizing for interconnect layout optimization," in *Proc. Int. Conf. Computer Aided Design*, pp. 44–49, Nov. 1996.

[13] C. P. Chen, Y. W. Chang, and D. F. Wong, "Fast performance-driven optimization for buffered clock trees based on Lagrangian relaxation," in *Proc. Design Automation Conf.*, pp. 405–408, 1996.

[14] J. Cong, L. He, A. B. Kahng, D. Noice, N. Shirali, and S. H.-C. Yen, "Analysis and justification of a simple, practical 2 1/2-d capacitance extraction methodology," in *Proc. ACM/IEEE Design Automation Conf.*, pp. 40.1.1–40.1.6, June, 1997.

[15] J. Cong, C.-K. Koh, and K.-S. Leung, "Simultaneous buffer and wire sizing for performance and power optimization," in *Proc. Int. Symp. on Low Power Electronics and Design*, pp. 271–276, Aug. 1996.

[16] J. Cong and L. He, "An efficient approach to simultaneous transistor and interconnect sizing," in *Proc. Int. Conf. on Computer Aided Design*, pp. 181–186, Nov. 1996.

[17] J. Cong and C.-K. Koh, "Simultaneous driver and wire sizing for performance and power optimization," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 2, pp. 408–423, Dec. 1994.

[18] J. Cong and L. He, "Theory and Algorithm of Local Refinement Based Optimization, " Manuscript, 1998.

Appendix: Proof of Symmetric Effective-Fringing Property

In the following, we prove the symmetric effective-fringing property. First, we state two previously reported results that will be used in our proof. [17] showed the following relation between driver sizing and wire sizing solutions.

Lemma 1 *[17]* **DS/WS Relation:** *For any tree T with one or more critical sinks, let R be the resistance of the driver driving the routing tree and $\mathcal{W}$ be the corresponding optimal wire width assignment. Let R' be the resistance of another driver and $\mathcal{W}'$ be the corresponding optimal wire width assignment. Then, $R < R'$ implies $\mathcal{W}$ dominates $\mathcal{W}'$.* □

The authors of [15] investigated the relation between the loading capacitances and wiresizing solutions and showed the following:

Lemma 2 *[15]* **WS/CL Relation:** *Let c_{s_k} be the loading capacitance of one of the sinks, say s_k, of T, and $\mathcal{W}$ be the corresponding optimal wiresizing solution. If we increase the loading capacitance of a sink from c_{s_k} to c'_{s_k}, and let $\mathcal{W}'$ be a corresponding optimal wire width assignment. Then, then there exists an optimal wiresizing solution $\mathcal{W}'$ that dominates $\mathcal{W}$.* □

For ease of reference, we re-write the performance measure t_T for a routing tree T based on the Eqn (3) (for compaction of notations, we drop the superscript or subscript j, since we just consider any routing tree T):

$$\begin{aligned} t_T(\mathcal{W}) &= \lambda(s_0)\cdot R\cdot\sum_{E\in T}(c_a\cdot w_E + c_{ef}(E)) \; + \\ &\sum_{E\in T}\lambda(E)\cdot\frac{r}{w_E}\cdot\left\{\frac{c_a\cdot w_E + c_{ef}(E)}{2} \; + \sum_{s\in sink(E)} c_s \; + \sum_{E'\in Des(E)}(c_a\cdot w_{E'} + c_{ef}(E'))\right\} \end{aligned} \tag{5}$$

Recall that $\lambda(s_0) = \sum_{s_k\in sink(T)}\lambda_k$ and $\lambda(E) = \sum_{s_k\in sink(E)}\lambda_k$, where λ_k is the criticality of sink s_k. In this formulation, we assume a fixed area capacitance c_a, but edges may have different effective fringing capacitance coefficients. Let the set of effective fringing capacitance coefficients be $\mathcal{C}_{ef}$. Let $\hat{\mathcal{W}}(c_a,\mathcal{C}_{ef})$ be an optimal sizing solution for some constant c_a and a given set of effective fringing capacitance coefficients $\mathcal{C}_{ef}$ (for ease of presentation, we will abbreviate $\hat{\mathcal{W}}(c_a,\mathcal{C}_{ef})$ into $\hat{\mathcal{W}}$. Similarly, we define $\hat{\mathcal{W}}'$ to be an optimal sizing solution for the same c_a, but under a different set of effective fringing capacitance coefficients $\mathcal{C}'_{ef}$. Let $\hat{w}_E$ be the width of E in $\hat{\mathcal{W}}$ and $\hat{w}'_E$ be the width of E in $\hat{\mathcal{W}}'$. In the following, we assume that $\lambda(E) > 0$.

First, we introduce the following lemma for a simple scenario. Consider a particular edge E. Let $c_{ef}(E') = c'_{ef}(E')$ for any edge $E' \neq E$, but $c_{ef}(E) > c'_{ef}(E)$. Then, we show that $\hat{\mathcal{W}}$ still dominates $\hat{\mathcal{W}}'$.

Lemma 3 *For two different sets of effective-fringing capacitance coefficients $\mathcal{C}_{ef}$ and $\mathcal{C}'_{ef}$ with $c_{ef}(E') = c'_{ef}(E')$ for any edge $E' \neq E$, but $c_{ef}(E) > c'_{ef}(E)$, we have*

$$\frac{\lambda(E)}{2}\cdot\left(\frac{1}{\hat{w}_E} - \frac{1}{\hat{w}'_E}\right) \; + \sum_{E'\in Ans(E)}\lambda(E')\cdot\left(\frac{1}{\hat{w}_{E'}} - \frac{1}{\hat{w}'_{E'}}\right) \; \leq \; 0 \tag{6}$$

Proof of Lemma 3: In the following, we use $t_T(c_{ef}(E),\hat{\mathcal{W}})$ to denote the performance measure corresponding to the case where the effective-fringing capacitance coefficient of E is $c_{ef}(E)$ with corresponding optimal wire sizing solution $\hat{\mathcal{W}}$. Similarly, we can denote $t_T(c'_{ef}(E),\hat{\mathcal{W}}')$ to be the performance measure under the $c'_{ef}(E)$ and the corresponding optimal wire sizing solution $\hat{\mathcal{W}}'$. Suppose we swap the two sizing solutions. Then, we obtain new performance measures $t_T(c_{ef}(E),\hat{\mathcal{W}}')$ and $t_T(c'_{ef}(E),\hat{\mathcal{W}})$. Let Δ_1 denote the difference $t_T(c_{ef}(E),\hat{\mathcal{W}}) - t_T(c_{ef}(E),\hat{\mathcal{W}}')$. Then, from Eqn. (5):

$$\begin{aligned} \Delta_1 &= \lambda(s_0)\cdot R\cdot\sum_{E'\in T} c_a\cdot(\hat{w}_{E'} - \hat{w}'_{E'}) \\ &+ \sum_{E'\in T, E'\neq E}\lambda(E')\cdot\frac{r}{\hat{w}_{E'}}\cdot\left\{\frac{c_a\cdot\hat{w}_{E'} + c_{ef}(E')}{2} \; + \sum_{s_k\in sink(E')} c_{s_k} \; + \sum_{E''\in Des(E'),E''\neq E}(c_a\cdot\hat{w}_{E''} + c_{ef}(E''))\right\} \\ &- \sum_{E'\in T, E'\neq E}\lambda(E')\cdot\frac{r}{\hat{w}'_{E'}}\cdot\left\{\frac{c_a\cdot\hat{w}'_{E'} + c_{ef}(E')}{2} + \sum_{s_k\in sink(E')} c_{s_k} \; + \sum_{E''\in Des(E'),E''\neq E}(c_a\cdot\hat{w}'_{E''} + c_{ef}(E''))\right\} \\ &+ \sum_{E'\in Ans(E)}\lambda(E')\cdot\frac{r}{\hat{w}_{E'}}\cdot(c_a\cdot\hat{w}_E + c_{ef}(E)) \; - \sum_{E'\in Ans(E)}\lambda(E')\cdot\frac{r}{\hat{w}'_{E'}}\cdot(c_a\cdot\hat{w}'_E + c_{ef}(E)) \end{aligned}$$

$$
\begin{aligned}
&+ \ \lambda(E)\cdot\frac{r}{\hat{w}_E}\cdot\left\{\frac{c_a\cdot\hat{w}_E+c_{ef}(E)}{2}+\sum_{s_k\in sink(E)}c_{s_k}\ +\ \sum_{E'\in Des(E)}(c_a\cdot\hat{w}_{E'}+c_{ef}(E'))\right\}\\
&- \ \lambda(E)\cdot\frac{r}{\hat{w}'_E}\cdot\left\{\frac{c_a\cdot\hat{w}'_E+c_{ef}(E)}{2}+\sum_{s_k\in sink(E)}c_{s_k}\ +\ \sum_{E'\in Des(E)}(c_a\cdot\hat{w}'_{E'}+c_{ef}(E'))\right\}\\
\leq\ & 0
\end{aligned}
$$

where the first line corresponds to the terms related with the driver resistance, the second and the third lines correspond to those edge terms not related with E, the fourth line corresponds to E and its ancestor edges, and the fifth and the sixth lines correspond to E and its downstream subtrees.

Let Δ_2 denote $t_T(c'_{ef}(E),\hat{\mathcal{W}}')-t_T(c'_{ef}(E),\hat{\mathcal{W}})$. The inequality for $\Delta_2\leq 0$ can be similarly obtained. Summing Δ_1 and Δ_2, we can easily cross the common terms out and obtain

$$
\lambda(E)\cdot r\cdot(\frac{1}{\hat{w}_E}-\frac{1}{\hat{w}'_E})\cdot(\frac{c_{ef}(E)-c'_{ef}(E)}{2})\ +\ \sum_{E'\in Ans(E)}\lambda(E')\cdot r\cdot(\frac{1}{\hat{w}_{E'}}-\frac{1}{\hat{w}'_{E'}})\cdot(c_{ef}(E)-c'_{ef}(E))\quad\leq\quad 0
$$

Since $c_{ef}(E)>c'_{ef}(E)$, the result follows. □

Let T_E be the single stem sub-tree rooted at E and T_v be the downstream subtree rooted at node v [2]. Let $\hat{\mathcal{W}}(T_E)$ and $\hat{\mathcal{W}}'(T_E)$ denote the sizing solutions $\hat{\mathcal{W}}$ and $\hat{\mathcal{W}}'$ restricted to edges in T_E only. Then we have the following lemma.

Lemma 4 *For two different sets of effective-fringing capacitance coefficients $\mathcal{C}_{ef}$ and $\mathcal{C}'_{ef}$ with $c_{ef}(E')=c'_{ef}(E')$ for any edge $E'\neq E$, but $c_{ef}(E)>c'_{ef}(E)$, we have $\hat{\mathcal{W}}(T_E)$ dominates $\hat{\mathcal{W}}'(T_E)$.*

Proof of Lemma 4: Denote the two end nodes of E being u and v in T, where u is the upstream node and v is the downstream node. We first argue that $\hat{\mathcal{W}}(T_v)$ dominates $\hat{\mathcal{W}}'(T_v)$ where $\hat{\mathcal{W}}(T_v)$ and $\hat{\mathcal{W}}'(T_v)$ are the wire sizing solutions $\hat{\mathcal{W}}$ and $\hat{\mathcal{W}}'$ restricted to edges in T_v only. We observe that the total weighted upstream resistance of T_v for $\hat{\mathcal{W}}$ is

$$
R(T_v)\ =\ \lambda(s_0)\cdot R+\lambda(E)\cdot r\cdot\frac{1}{2\hat{w}_E}\ +\ \sum_{E'\in Ans(E)}\lambda(E')\cdot r\cdot\frac{1}{\hat{w}_{E'}}
$$

and the total upstream resistance of T_v for $\hat{\mathcal{W}}'$ is

$$
R'(T_v)\ =\ \lambda(s_0)\cdot R+\lambda(E)\cdot r\cdot\frac{1}{2\hat{w}'_E}\ +\ \sum_{E'\in Ans(E)}\lambda(E')\cdot r\cdot\frac{1}{\hat{w}'_{E'}}
$$

From Lemma 3, $R(T_v)\leq R'(T_v)$. Applying Lemma 1, we can conclude $\hat{\mathcal{W}}(T_v)$ dominates $\hat{\mathcal{W}}'(T_v)$.

Now, consider the edge E. We keep the wire width assignment of all other edges, and swap only the wire width assignment of edge E in the two wire sizing solutions $\hat{\mathcal{W}}$ and $\hat{\mathcal{W}}'$, i.e., $\hat{\mathcal{W}}_{swap}$=$\hat{\mathcal{W}}$ except $\hat{w_E}\leftarrow\hat{w'_E}$ and $\hat{\mathcal{W}}'_{swap}$=$\hat{\mathcal{W}}'$ except $\hat{w'_E}\leftarrow\hat{w_E}$. Let Δ_1 be $t_T(c_{ef}(E),\hat{\mathcal{W}})-t_T(c_{ef}(E),\hat{\mathcal{W}}_{swap})$ and Δ_2 be $t_T(c'_{ef}(E),\hat{\mathcal{W}}')-t_T(c'_{ef}(E),\hat{\mathcal{W}}'_{swap})$. Then,

$$
\Delta_1\quad=\quad\lambda(s_o)\cdot R\cdot c_a\cdot(\hat{w}_E-\hat{w}'_E)\ +
$$

$$\sum_{E' \in Ans(E)} \lambda(E) \cdot \frac{r}{\hat{w}_{E'}} \cdot c_a \cdot (\hat{w}_E - \hat{w}'_E) \; +$$

$$\lambda(E) \cdot \left(\frac{r}{\hat{w}_E} - \frac{r}{\hat{w}'_E} \right) \cdot \left(\frac{c_{ef}(E)}{2} + \sum_{s_k \in sink(E)} c_{s_k} + \sum_{E' \in Des(E)} (c_a \cdot \hat{w}_{E'} + c_{ef}(E')) \right)$$

$$\leq \; 0$$

Obtaining Δ_2 in a similar fashion, and then summing Δ_1 and Δ_2 together, we obtain the following expression:

$$c_a \cdot (\hat{w}_E - \hat{w}'_E) \cdot \sum_{E' \in Ans(E)} \lambda(E') \cdot \left(\frac{r}{\hat{w}_{E'}} - \frac{r}{\hat{w}'_{E'}} \right) \; +$$

$$\lambda(E) \cdot \left(\frac{r}{\hat{w}_E} - \frac{r}{\hat{w}'_E} \right) \cdot \left(\frac{c_{ef}(E) - c'_{ef}(E)}{2} + \sum_{E' \in Des(E)} c_a \cdot (\hat{w}_{E'} - \hat{w}'_{E'}) \right) \quad \leq \quad 0$$

Since $\mathcal{W}(T_v)$ dominates $\mathcal{W}'(T_v)$, $c_{ef}(E) > c'_{ef}(E)$, if we assume that $\hat{w}_E < \hat{w}'_E$, we get

$$\sum_{E' \in Ans(E)} \lambda(E') \cdot \left(\frac{1}{\hat{w}_{E'}} - \frac{1}{\hat{w}'_{E'}} \right) \; \geq \; 0$$

Combining it with Lemma 3, we will have $\frac{1}{\hat{w}_E} - \frac{1}{\hat{w}'_E} \leq 0$, which is a contradiction to the assumption that $\hat{w}_E < \hat{w}'_E$. Therefore, $\hat{w}_E \geq \hat{w}'_E$, and $\hat{\mathcal{W}}(T_E)$ dominates $\hat{\mathcal{W}}'(T_E)$. □

We can now prove the following lemma:

Lemma 5 *Consider any edge E in T. If $c_{ef}(E') = c'_{ef}(E')$ for any edge $E' \neq E$, but $c_{ef}(E) > c'_{ef}(E)$. Then, $\hat{\mathcal{W}}$ dominates $\hat{\mathcal{W}}'$.*

Proof of Lemma 5: Now consider node u, the upstream node of E. Create a sink s_u such that the loading capacitance of s_u is equivalent to the total capacitance of T_E under wiresizing solution $\hat{\mathcal{W}}$. Create another tree $T' = T - T_E$, and that at node u, it has sink s_u. Note that the optimal wiresizing solution of T' combines with $\hat{\mathcal{W}}(T_E)$ is exactly $\hat{\mathcal{W}}$. Similarly, let $T'' = T - T_E$, and the at node u, it has sink s'_u which has a loading capacitance equivalent to the total capacitance of T_E under wiresizing solution $\hat{\mathcal{W}}'$. By Lemma 4, $c_{s_u} > c_{s'_u}$. By applying Lemma 2, the wiresizing solution of T' dominates T''. Therefore, the lemma holds. □

This leads to Theorem 1:

Theorem 1 Symmetric Effective-Fringing Property: *For a fixed area capacitance c_a, let $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ be an optimal wiresizing solution to optimize the performance measure t_T under a set of effective fringing capacitance coefficients $\mathcal{C}_{ef} = \{c_{ef}(E) \mid E \in T\}$, and $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef})$ be an optimal sizing solution under a different set of effective fringing capacitance coefficients $\mathcal{C}'_{ef} = \{c'_{ef}(E) \mid E \in T\}$. Then if $\mathcal{C}_{ef} \geq \mathcal{C}'_{ef}$, i.e., $c_{ef}(E) \geq c'_{ef}(E)$ for all edges E, we can conclude that there exist optimal solutions such that $\hat{\mathcal{W}}(c_a, \mathcal{C}_{ef})$ dominates $\hat{\mathcal{W}}(c_a, \mathcal{C}'_{ef})$.*

Proof of Theorem 1: By a simple induction on all edges E with $c_{ef}(E) > c'_{ef}(E)$ based on Lemma 5. □

Note that the above results are obtained under the assumption that $\lambda(E) > 0$. In the case of $\lambda(E) = 0$, let E' be the last edge (in a bottom-up order) in $Ans(E) \cup \{E\}$ such that $\lambda(E') = 0$. Note that E' may be E. Then, $\hat{\mathcal{W}}(T_{E'})$ and $\hat{\mathcal{W}}'(T_{E'})$ will have identical wiresizing solutions, i.e., all edges in $T_{E'}$ are assigned the minimum width allowed. However, the total capacitance in $\hat{\mathcal{W}}(T_{E'})$ is strictly larger than that in $\hat{\mathcal{W}}'(T_{E'})$ since $c_{ef}(E) > c'_{ef}(E)$. Therefore, applying Lemma 2 again, $\hat{\mathcal{W}}$ still dominates $\hat{\mathcal{W}}'$.