

Interconnect Estimation and Planning for Deep Submicron Designs

Jason Cong and David Zhigang Pan

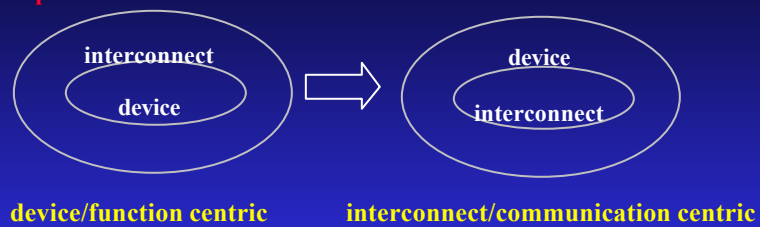
UCLA Computer Science Department
Los Angeles, CA 90095

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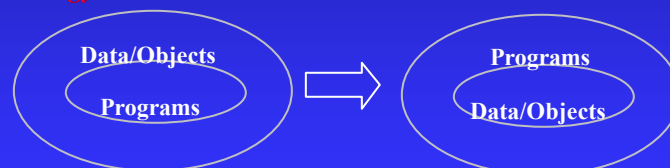


Interconnect-Centric Design Methodology


■ Proposed transition



■ Analogy



Interconnect-Centric Design Flow

- At UCLA, we are working on an interconnect-centric design flow, which includes:
 - ◆ Interconnect Planning 
 - ◆ Interconnect Synthesis
 - ◆ Interconnect Layout
- Other supporting tools
 - ◆ Interconnect performance estimation
 - ◆ Interconnect performance verification
- Integration for design convergence

Interconnect Architecture Planning

- Pre-design planning (within the fabrication technology)
 - ◆ number of routing layers
 - ◆ metal and isolation material at each layer
 - ◆ thickness of each metal and isolation layer
 - ◆ nominal width and spacing on each layer
 - ◆ ...
- Problem in this talk: optimal wire width planning for each metal layer, with performance-area optimization

Problem Formulation

■ Given:

- ◆ Certain technology
- ◆ Wire assignment for each metal layer

■ Find:

- ◆ A small set of “globally optimal” widths per layer
- ◆ Performance/Area optimization

■ Motivation

- ◆ Simplify interconnect optimization
- ◆ Ease routing architecture

Design Optimization Objective

- Given some weight function $I(l)$ for wire length range $[l_{\min}, l_{\max}]$, we want to find *a small set of optimal widths* W^* to minimize

$$\Phi(\vec{W}, l_{\min}, l_{\max}) = \int_{l_{\min}}^{l_{\max}} I(l) \cdot f(\vec{W}, l) dl$$

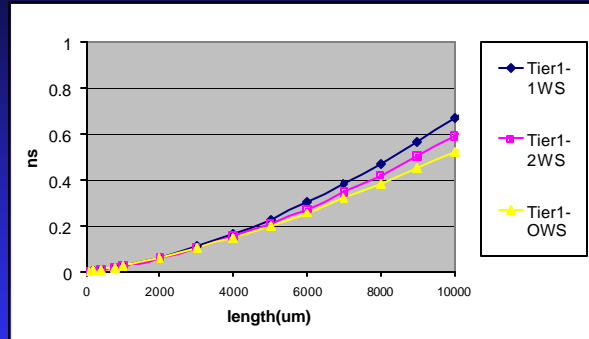
- $f(\vec{W}, l)$: the objective function to be minimized by the design using \vec{W}

$$f(\vec{W}, l) = A^j(\vec{W}, l) \cdot T^k(\vec{W}, l) \quad (A\text{-area } T\text{-delay})$$

$$f(\vec{W}, l) = T(\vec{W}, l) \quad (\text{performance only})$$

or $f(\vec{W}, l) = A(\vec{W}, l) \cdot T^4(\vec{W}, l) \quad (\text{performance-driven and area-saving})$

1-WS and 2-WS



- 1-WS and 2-WS have less than 10% difference from OWS for length <4mm in Tier1 (Metal 1-2)
- Both work well in upper metal layer up to chip dimension
- In above figure, **different widths** for different lengths.

Overall Approach

For each metal layer i

Assign length range l_{min} and l_{max} ;
Find W^* or $\{W_1^*, W_2^*\}$ to minimize

$$\Phi(\bar{W}, l_{min}, l_{max}) = \int_{l_{min}}^{l_{max}} \mathbf{I}(l) \cdot f(\bar{W}, l) dl$$

Method: Analytical and numerical

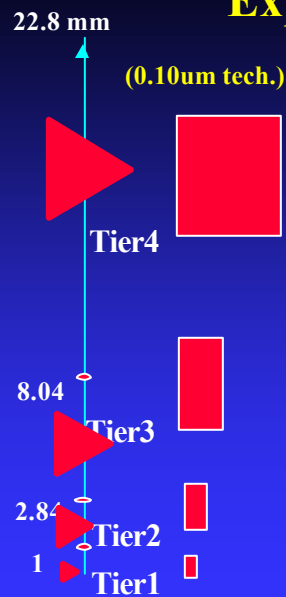
Overall Approach (Cont'd)

- Analytical formula for 1-width planning for best T

$$W^* = \sqrt{\frac{\frac{1}{3}rc_f(l_{\max}^3 - l_{\min}^3) + rCL(l_{\max}^2 - l_{\min}^2)}{RdCa(l_{\max}^2 - l_{\min}^2)}}$$

- Numerical method by effectively searching the best 1-width planning under AT⁴ metric and the best 2-width planning under T and AT⁴ metrics

Experimental Setting



- Parameters based on NTRS'97 and Strawman [Otten&Brayton, DAC'98]
- Assume uniform weight function and the max length in Tier1 is 10,000x feature size, and in top tier is the chip dimension
- Intermediate tier's length range follows a geometric sequence
- Representative driver size for each metal layer (10x, 40x, 100x, and 250x for tiers 1-4)
- Verify against optimal wire sizing and spacing algorithm (using many widths) [Cong+, ICCAD'97]

Surprising Result: Two widths good enough!

scheme	pitch-sp=2um			pitch-sp=2.9um			pitch-sp=3.8um		
	avg-d	max-err	avg-w	avg-d	max-err	avg-w	avg-d	max-err	avg-w
1-width	0.245	28%	1.98	0.177	16%	1.83	0.143	6%	1.63
2-width	0.215	7%	1.08	0.167	5.90%	1.23	0.14	4%	1.41
m-width	0.204	0%	1.03	0.159	0%	1.19	0.136	0%	1.38

- Case study of 0.10um using upper metal pair
- 2-width design superior than 1-width design
 - ◆ delay reduction up to 12.4%
 - ◆ area saving up to 48% !
- 2-width design comparable to many-width design
 - ◆ Avg. delay less than 5% and Max. delay less than 7%
 - ◆ Area difference less than 4.7%

Max-error Theorem

$$\Phi(\vec{W}, l_{\min}, l_{\max}) = \int_{l_{\min}}^{l_{\max}} I(l) \cdot f(\vec{W}, l) dl$$

If $\frac{f(\vec{W}, l) - f(\vec{W}^*, l)}{f(\vec{W}^*, l)} \leq d_{\max}$ for any $l \in (l_{\min}, l_{\max})$

⇒ $\left| \frac{\Phi(\vec{W}, l_{\min}, l_{\max}) - \Phi(\vec{W}^*, l_{\min}, l_{\max})}{\Phi(\vec{W}^*, l_{\min}, l_{\max})} \right| \leq d_{\max}$ for any $I(l)$

- Max-error of any length is less than 7% in our expt =>
- For any weight function $I(l)$, the max-error of weighted integral (our objective function) is less than 7% !

Recommendation for Future Tech.

- 2-width design under objective function of AT^4
- Wiring hierarchy for both performance and density !

Technology (um)		0.25	0.18	0.13	0.10	0.07
M12	W (um)	0.25	0.18	0.13	0.10	0.07
M34	W1(um)	0.25	0.18	0.13	0.10	0.08
	W2(um)	0.50	0.36	0.26	0.20	0.16
M56	W1(um)	0.65	0.47	0.24	0.22	0.23
	W2(um)	1.30	0.94	0.48	0.44	0.46
M78	W1(um)	-	-	0.98	1.00	1.06
	W2(um)	-	-	1.96	2.00	2.12

Conclusion

- Interconnect architecture planning
 - ◆ In-depth study of optimal wire-width planning
 - ◆ An analytical formulation considering both delay and area optimization
 - ◆ A surprising result showing that 2-width planning achieves near-optimal solution
- Closed-form interconnect area estimation model for optimal wire sizing optimization
- Application:
 - ◆ Simplify routing architecture with consideration of interconnect optimization
 - ◆ Simplify many other related problems ...