Interconnect Estimation and Planning for Deep Submicron Designs

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Sponsored by SRC

Interconnect-Centric Design Methodology

- Proposed transition
- Analogy

- Interconnect centric vs. device centric
  - device/function centric
  - interconnect/communication centric

- Data/Objects vs. Programs
  - Programs
  - Data/Objects
At UCLA, we are working on an interconnect-centric design flow, which includes:

- Interconnect Planning
- Interconnect Synthesis
- Interconnect Layout

Other supporting tools:

- Interconnect performance estimation
- Interconnect performance verification

Integration for design convergence

Pre-design planning (within the fabrication technology):

- number of routing layers
- metal and isolation material at each layer
- thickness of each metal and isolation layer
- nominal width and spacing on each layer
- ...

Problem in this talk: optimal wire width planning for each metal layer, with performance-area optimization
Problem Formulation

**Given:**
- Certain technology
- Wire assignment for each metal layer

**Find:**
- A small set of “globally optimal” widths per layer
- Performance/Area optimization

**Motivation**
- Simplify interconnect optimization
- Ease routing architecture

Design Optimization Objective

- Given some weight function $\lambda(l)$ for wire length range $[l_{\text{min}}, l_{\text{max}}]$, we want to find a small set of optimal widths $W^*$ to minimize

$$\Phi(W, l_{\text{min}}, l_{\text{max}}) = \int_{l_{\text{min}}}^{l_{\text{max}}} \lambda(l) \cdot f(W, l) dl$$

- $f(W, l)$: the objective function to be minimized by the design using $W$

$$f(W, l) = A^4(W, l) \cdot T^4(W, l)$$

- (A-area T-delay)

- (performance only)

or

$$f(W, l) = A(W, l) \cdot T(W, l)$$

- (performance-driven and area-saving)
1-WS and 2-WS

- 1-WS and 2-WS have less than 10% difference from OWS for length <4mm in Tier1 (Metal 1-2)
- Both work well in upper metal layer up to chip dimension
- In above figure, different widths for different lengths.

Overall Approach

For each metal layer $i$

Assign length range $l_{\text{min}}$ and $l_{\text{max}}$;

Find $W^*$ or $\{W_1^*, W_2^*\}$ to minimize

$$\Phi(W, l_{\text{min}}, l_{\text{max}}) = \int_{l_{\text{min}}}^{l_{\text{max}}} \lambda(l) \cdot f(W, l) dl$$

Method: Analytical and numerical
Overall Approach (Cont’d)

- Analytical formula for 1-width planning for best T
  \[ W^* = \sqrt{\frac{1}{3} rCf (l_{\text{max}}^2 - l_{\text{min}}^2) + rCf (l_{\text{max}}^2 - l_{\text{min}}^2)} \]
  \[ R_{\text{dca}} (l_{\text{max}}^2 - l_{\text{min}}^2) \]

- Numerical method by effective searching the best 1-width planning under AT^4 metric and the best 2-width planning under T and AT^4 metrics

Experimental Setting

- Parameters based on NTRS’97 and Strawman [Otten&Brayton, DAC’98]
- Assume uniform weight function and the max length in Tier1 is 10,000x feature size, and in top tier is the chip dimension
- Intermediate tier’s length range follows a geometric sequence
- Representative driver size for each metal layer (10x, 40x, 100x, and 250x for tiers 1-4)
- Verify against optimal wire sizing and spacing algorithm (using many widths) [Cong+, ICCAD’97]
Surprising Result: Two widths good enough!

Case study of 0.10um using upper metal pair

- 2-width design superior than 1-width design
  - delay reduction up to 12.4%
  - area saving up to 48%

- 2-width design comparable to many-width design
  - Avg. delay less than 5% and Max. delay less than 7%
  - Area difference less than 4.7%

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Max-error Theorem

\[ \Phi(\vec{W}, l_{\min}, l_{\max}) = \int_{l_{\min}}^{l_{\max}} \lambda(l) \cdot f(\vec{W}, l) dl \]

If \[ \frac{f(\vec{W}, l) - f(\vec{W}^*, l)}{f(\vec{W}^*, l)} \leq \delta_{\max} \text{ for any } l \in (l_{\min}, l_{\max}) \]

\[ \left| \frac{\Phi(\vec{W}, l_{\min}, l_{\max}) - \Phi(\vec{W}^*, l_{\min}, l_{\max})}{\Phi(\vec{W}^*, l_{\min}, l_{\max})} \right| \leq \delta_{\max} \text{ for any } \lambda(l) \]

- Max-error of any length is less than 7% in our expt =>
- For any weight function \( \lambda(l) \), the max-error of weighted integral (our objective function) is less than 7%! 

**Recommendation for Future Tech.**

- 2-width design under objective function of AT^4
- Wiring hierarchy for both performance and density!

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**Conclusion**

- Interconnect architecture planning
  - In-depth study of optimal wire-width planning
  - An analytical formulation considering both delay and area optimization
  - A surprising result showing that 2-width planning achieves near-optimal solution
- Closed-form interconnect area estimation model for optimal wire sizing optimization
- Application:
  - Simplify routing architecture with consideration of interconnect optimization
  - Simplify many other related problems...