System-on-a-Chip (SoC) Design

EE382M.20, Unique: 16930, Fall 2018

Lectures: TTh 12:30-2:00pm, ECJ 1.316

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Class website: Canvas and http://www.ece.utexas.edu/~gerstl/ee382m_f18/

Description

With technological advances that allow us to integrate complete multi-processor systems on a single die, Systems-on-Chip (SoCs) are at the core of most embedded computing and consumer devices, such as smart phones and automotive, aerospace, robotics or medical electronics. This course will provide an understanding of the concepts, issues, and process of designing highly integrated SoCs following systematic hardware/software co-design & co-verification principles. Specifically, the class project involves taking public domain C++ code for a machine learning based visual object detection application utilizing a deep/convolutional neural network (DNN/CNN) and mapping it to an ARM-based virtual and FPGA prototyping platform using state-of-the-art synthesis and verification tools and design flows.

Goals

This course is designed for students to learn and be able to:

- Model and specify embedded systems at high levels of abstraction.
- Analyze the functional and nonfunctional performance of the system early in the design process to support design decisions.
- Analyze hardware/software tradeoffs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.
- Analyze tradeoffs and explore architecture and mico-architecture design spaces to develop and synthesize custom hardware accelerators.
- Understand hardware, software, and interface synthesis.
- Understand issues in interface design.
- Use co-simulation to validate system functionality.
- Describe examples of applications and systems developed using a co-design approach.
- Appreciate issues in system-on-chip design associated with co-design, such as intellectual property, reuse, and verification.

Course Description and Course Topics

Methodologies and tools for System-on-Chip (SoC) and hardware/software co-design and co-verification:

- Hardware/software co-design: partitioning, real-time scheduling, hardware acceleration;
- Virtual prototyping: electronic system-level languages and hardware/software co-simulation;
- High-level synthesis: allocation, scheduling and binding algorithms for C-to-RTL synthesis;
- SoC integration: SoC communication architectures, IP interfacing, verification and test;
- FPGA prototyping of hardware/software systems.

Prerequisites

- Working knowledge of C and C++, including software development and debugging (e.g. EE322C Data Structures, or equivalent);
- Embedded real-time system design and hardware/software interfacing (e.g. EE445M Embedded & Real-time Operating Systems, or equivalent);
- Digital hardware design and hardware description languages (e.g. EE460M Digital System Design using Verilog, or equivalent);
- It is helpful to have some basic knowledge of advanced linear algebra and machine/deep learning algorithms.

Textbooks

No required textbook. Optional textbooks:

- P. Marwedel, *Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems, and the Internet of Things*, Third Edition, Springer, 2018.
- D. C. Black, J. Donovan, B. Bunton, A. Keist, *SystemC: From the Ground Up*, Second Edition, Springer, 2010.
- G. De Micheli, *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994.

Grading

Homework:	15%
Exam:	20%
Labs:	30%
Project:	35%

Late penalty: 20% per day (24 hours).

Oral discussion of homework problems is encouraged but solutions have to be submitted individually and independently. Labs and the final project will be done in teams. Copying of any part of a homework, lab or project solution without explicit reference to its source is plagiarism and considered cheating.

Tentative Course Outline and Schedule

Week	Lecture Topic
1 (Aug 30)	Class and Project Overview
2 (Sep 4/6)	SoC and Electronic System-Level (ESL) Design Methodology
3 (Sep 11/13)	Virtual Platform Prototyping and SystemC Language Introduction
4 (Sep 18/20)	Transaction-Level Modeling (TLM) in SystemC
5 (Sep 25/27)	HW/SW Co-Design
6 (Oct 2/4)	Application Mapping and Real-Time Task Scheduling
7 (Oct 9/11)	SoC Communication and Hardware Accelerator Architectures
8 (Oct 16/18)	C-to-RTL High-Level Synthesis
9 (Oct 23/25)	Operation Scheduling and Resource Binding
10 (Oct 30/Nov 1)	Advanced High-Level Synthesis

11 (Nov 6/8)	Emulation and FPGA Prototyping
12 (Nov 13/15)	Review, **Exam**
13 (Nov 20/22)	System Integration, *Thanksgiving*
14 (Nov 27/29)	SoC Verification and Testing
15 (Dec 4/6)	**Project Design Reviews**
Finals (TBD)	**Project Presentations**

Electronic Mail Notification Policy

In this course e-mail will be used as a means of communication with students. You will be responsible for checking your e-mail regularly for class work and announcements. The complete text of the University electronic mail notification policy and instructions for updating your e-mail address are available at http://cio.utexas.edu/policies/university-electronic-mail-student-notification-policy.

Use of Canvas and Class Web Site

This course uses the class web page and Canvas to distribute course materials, to communicate and collaborate online, to submit assignments and to post solutions and grades. You will be responsible for checking the class web page and the Canvas course site regularly for class work and announcements. As with all computer systems, there are occasional scheduled downtimes as well as unanticipated disruptions. Notification of disruptions will be posted on the Canvas login page. Scheduled downtimes are not an excuse for late work. However, if there is an unscheduled downtime for a significant period of time, I will make an adjustment if it occurs close to the due date.

Students with Disabilities

The University of Texas at Austin provides upon request appropriate academic accommodations for qualified students with disabilities. For more information, contact the Services for Students with Disabilities (SSD) at 471-6259, http://diversity.utexas.edu/disability.

Religious Holidays

Religious holy days sometimes conflict with class and examination schedules. If you miss an examination, work assignment, or other project due to the observance of a religious holy day you will be given an opportunity to complete the work missed within a reasonable time after the absence. It is the policy of The University of Texas at Austin that you must notify each of your instructors at least fourteen days prior to the classes scheduled on dates you will be absent to observe a religious holy day.

Counseling and Mental Health

Do your best to maintain a healthy lifestyle this semester by eating well, exercising, avoiding drugs and alcohol, getting enough sleep and taking some time to relax. This will help you achieve your goals and cope with stress. All of us benefit from support during times of struggle. You are not alone. There are

many helpful resources available on campus and an important part of the college experience is learning how to ask for help. Asking for support sooner rather than later is often helpful. If you or anyone you know experiences any academic stress, difficult life events, or feelings like anxiety or depression, we strongly encourage you to seek support. The Counseling and Mental Health Center (CMHC) provides counseling, psychiatric, consultation, and prevention services that facilitate students' academic and life goals and enhance their personal growth and well-being: http://cmhc.utexas.edu/.

Classroom Evacuation and Emergency Preparedness

All occupants of university buildings are required to evacuate a building when a fire alarm and/ or an official announcement is made indicating a potentially dangerous situation within the building. Familiarize yourself with all exit doors of each classroom and building you may occupy. Remember that the nearest exit door may not be the one you used when entering the building. If you require assistance in evacuation, inform your instructor in writing during the first week of class. For evacuation in your classroom or building:

1. Follow the instructions of faculty and teaching staff.
2. Exit in an orderly fashion and assemble outside.
3. Do not re-enter a building unless given instructions by emergency personnel.

Emergency evacuation route information and emergency procedures can be found at http://www.utexas.edu/emergency and https://preparedness.utexas.edu.