

EE382N.23: Embedded System Design and Modeling

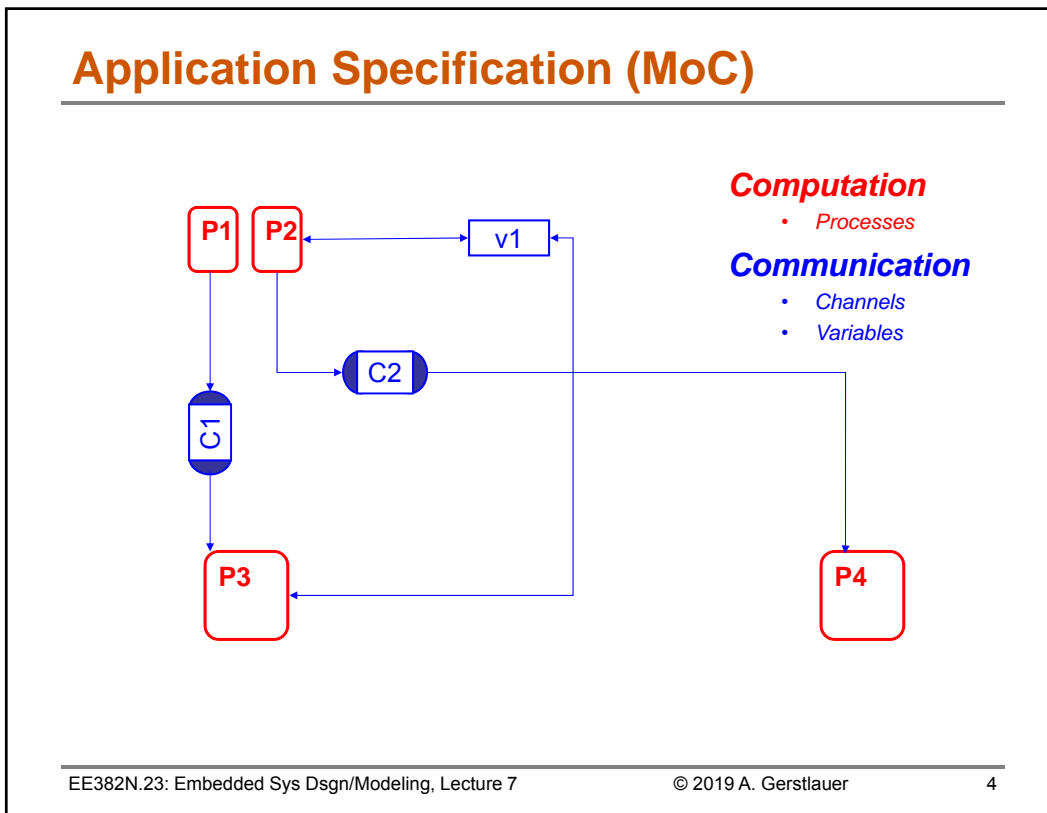
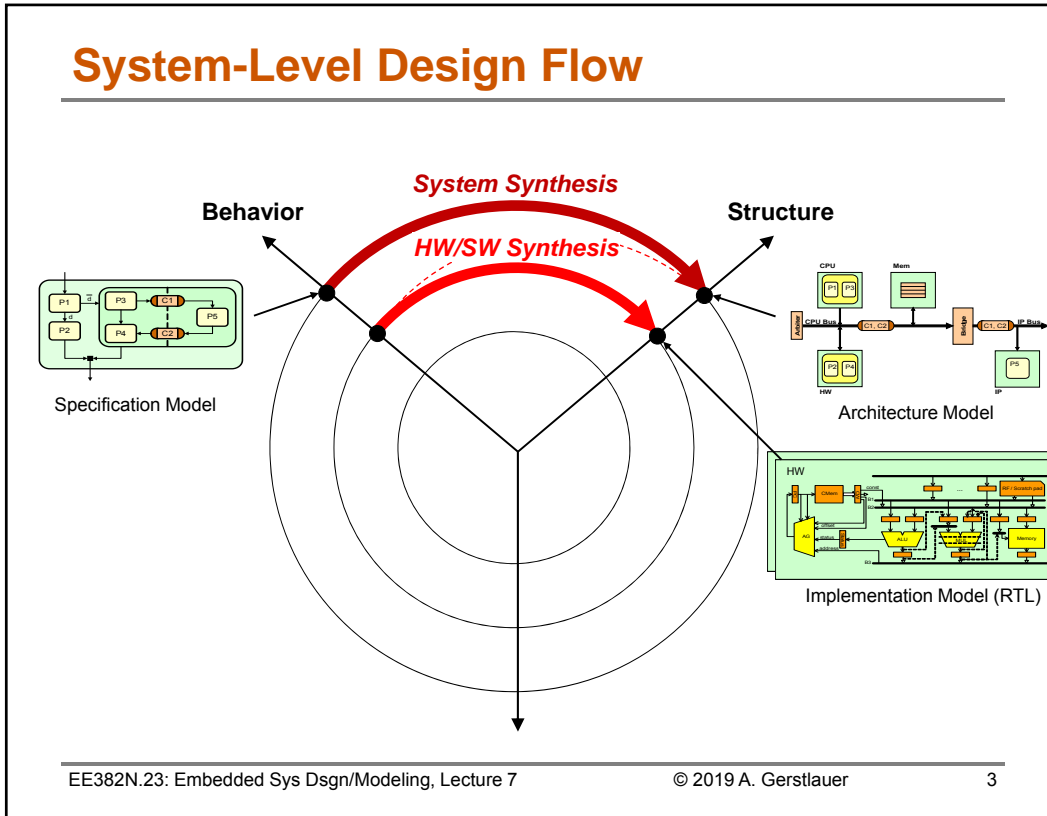
Lecture 7 – System Refinement

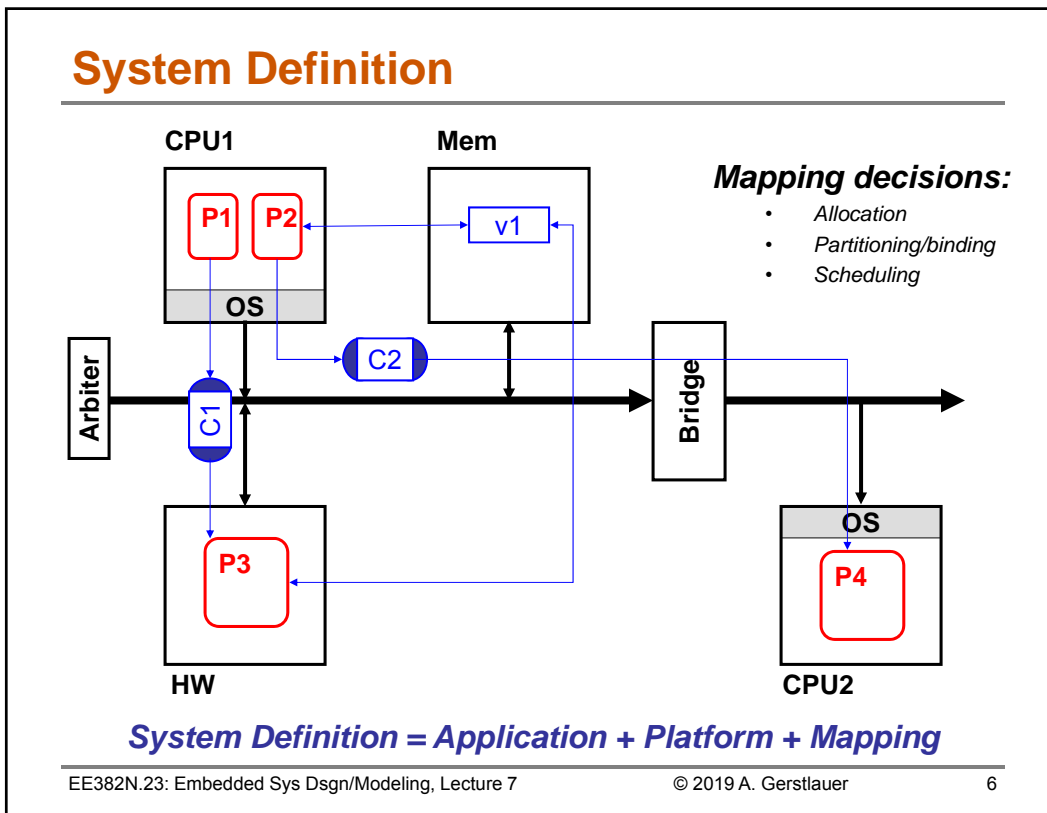
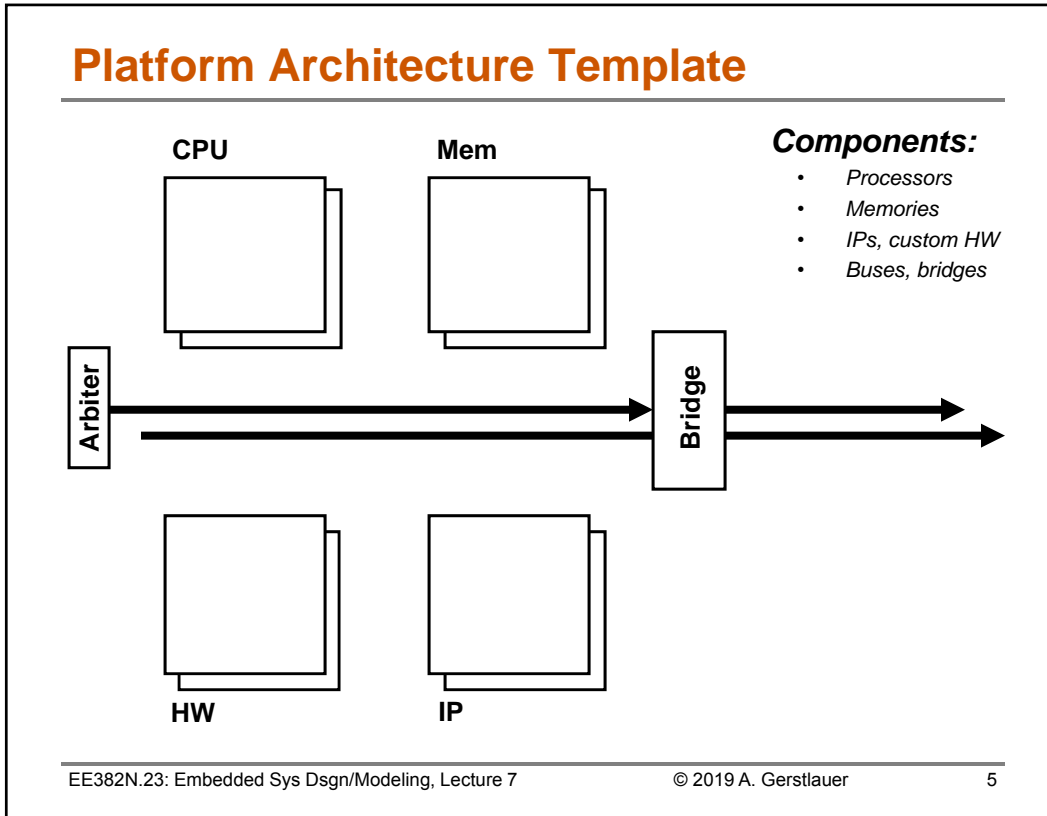
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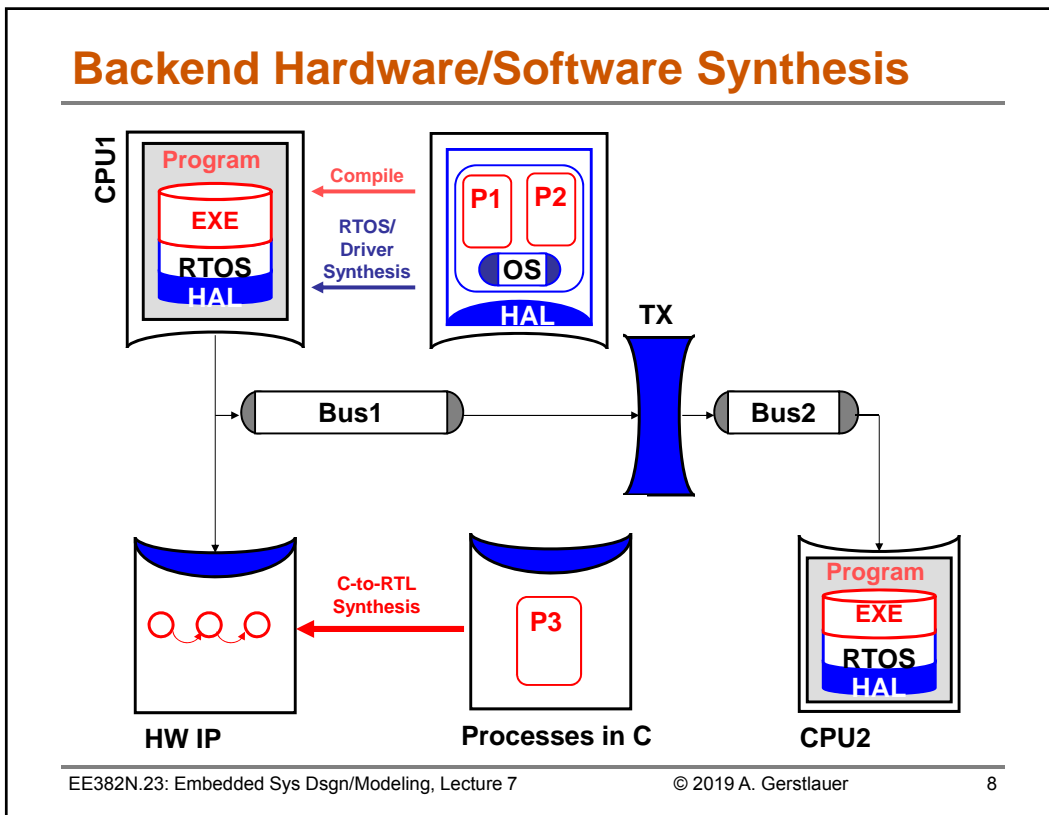
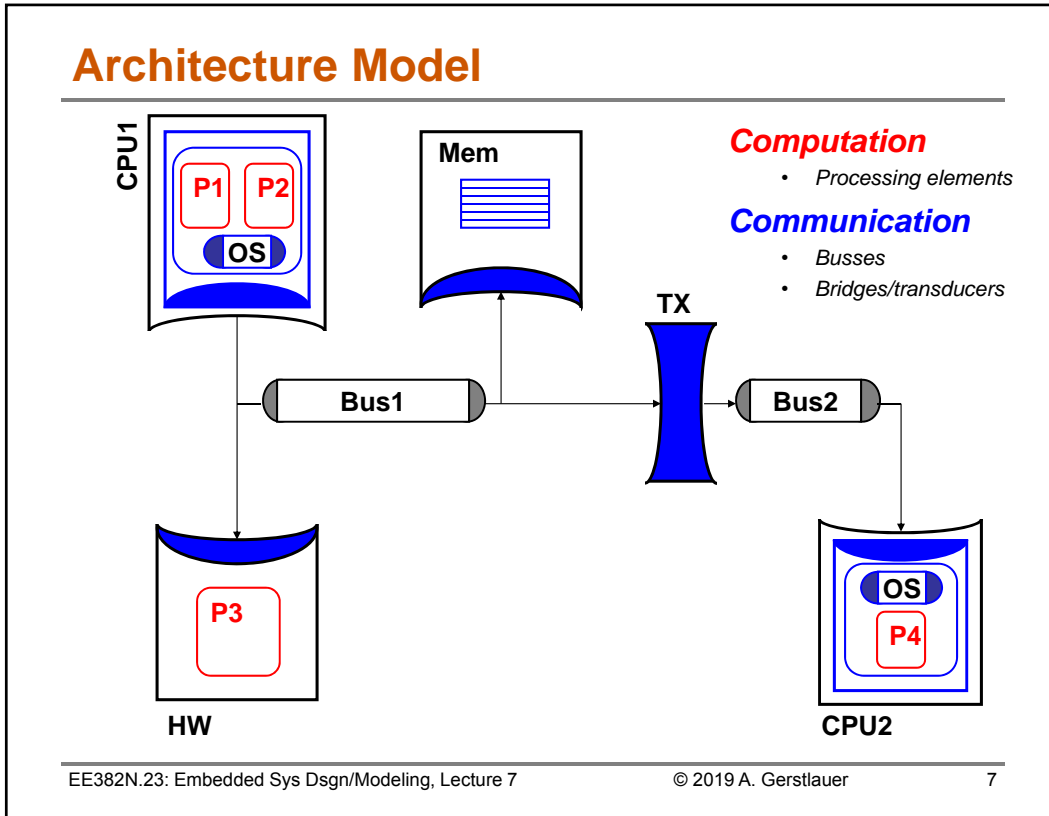


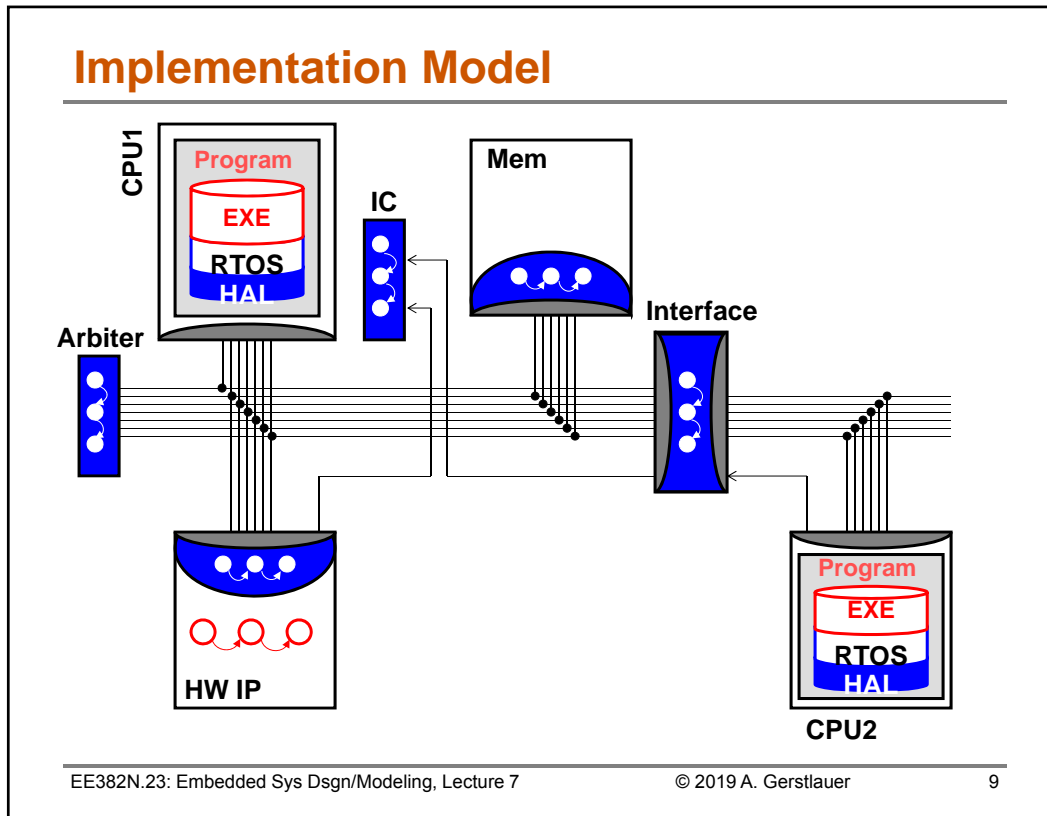
Lecture 7: Outline

- **System-level design flow**
 - From specification to implementation
- **System-level refinement**
 - Modeling flow & refinement process
- **System-level modeling**
 - Virtual prototyping & virtual platform models



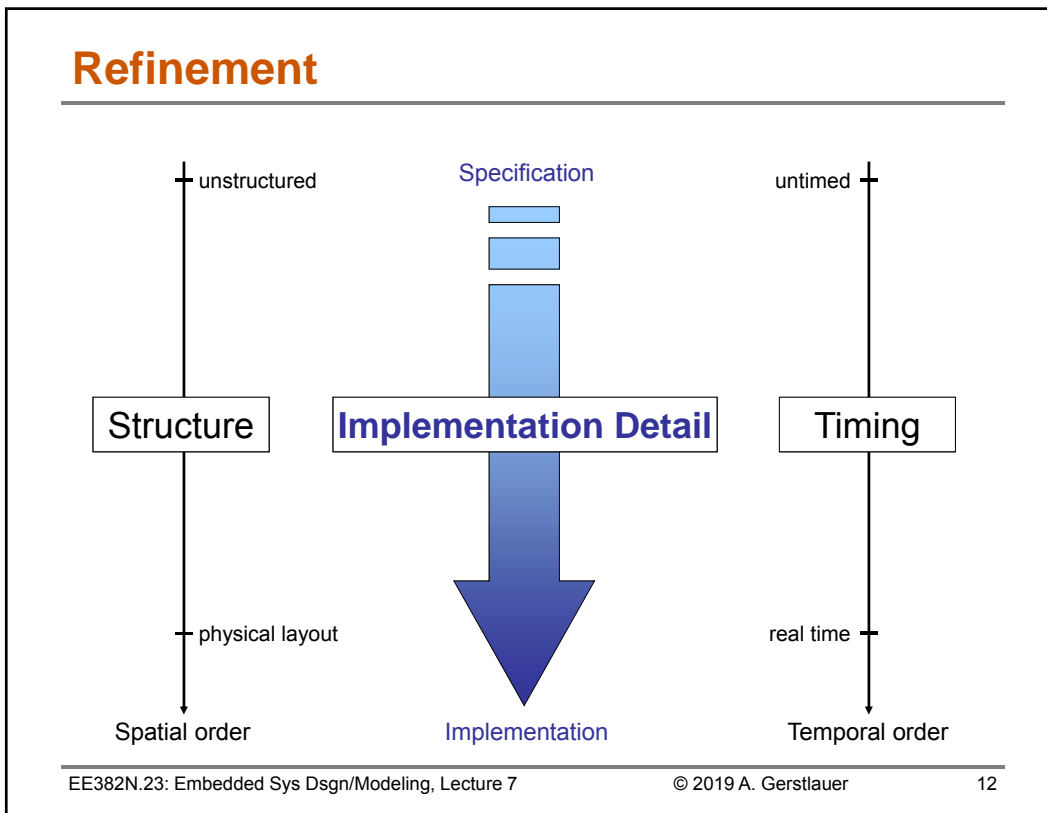
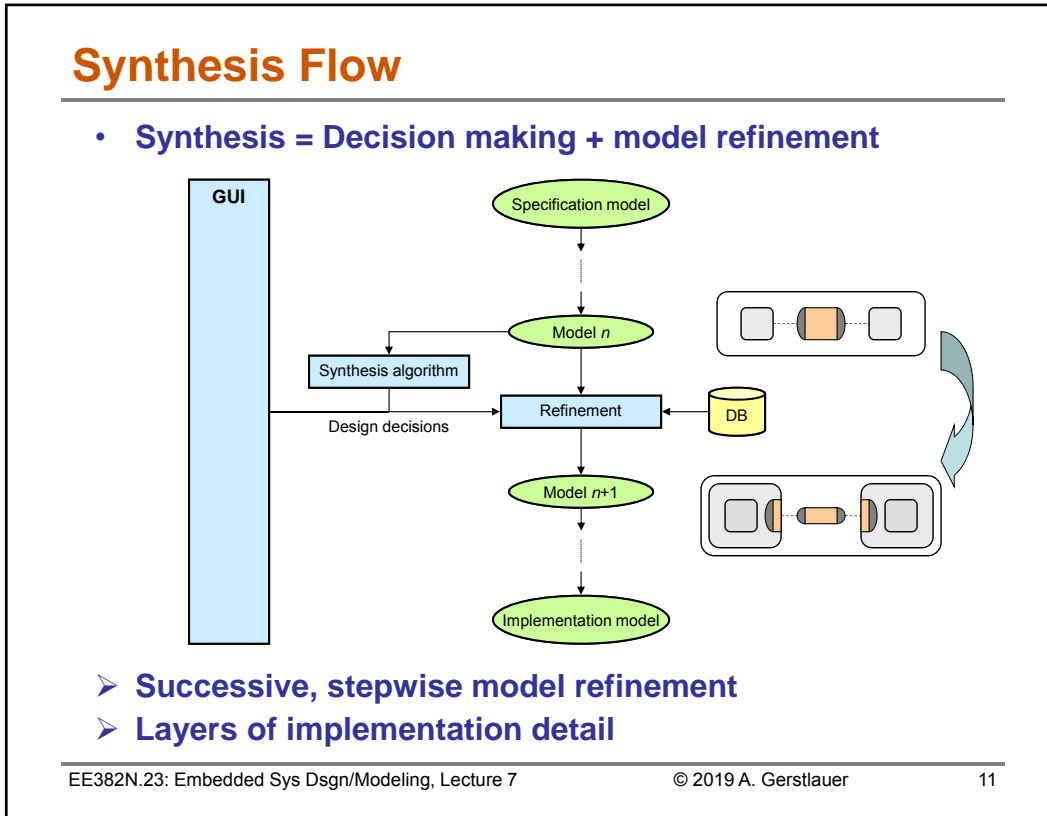






Modeling

- **Basis of any design flow and design automation**
 - Inputs and outputs of design steps
 - Capability to capture complex systems
 - Precise, complete and unambiguous
 - Models at varying levels of abstraction
 - Level and granularity of implementation detail
 - Speed vs. accuracy
- **Design models as an abstraction of a design instance**
 - Representation of some aspect of reality
 - Virtual prototyping for validation through simulation or formal analysis
 - Specification for further implementation
 - Describe desired functionality
 - Documentation & Specification (Simulation & Synthesis)
 - Abstraction to hide details that are not relevant or not yet known
 - Different parts of the model or different use cases for the same model



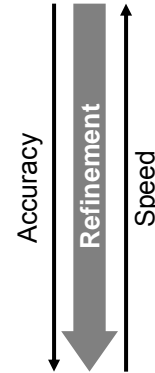
Speed vs. Accuracy

- **Discrete-event simulation speed**

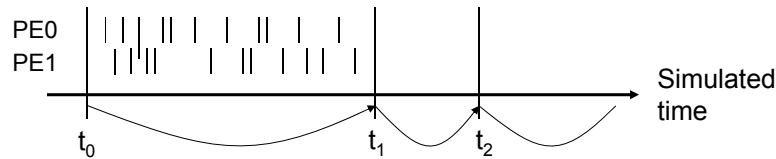
- Proportional to number of simulated events
- Proportional to granularity of simulated time/detail
 - “Real-time”: simulated vs. simulation time > 1

- **Discrete-event simulation accuracy**

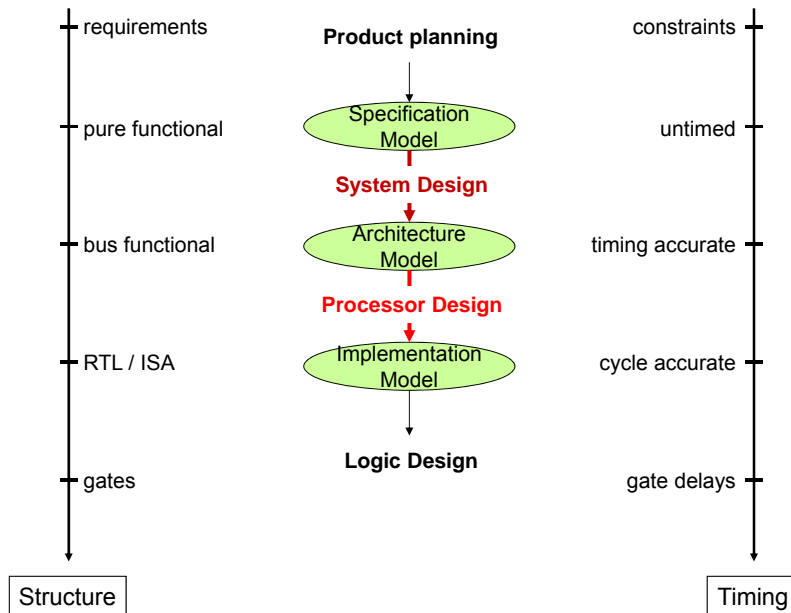
- Proportional to simulated implementation order
- Inversely proportional to simulated granularity
 - Where order matters (structural concurrency)



- **Fundamental modeling tradeoff**



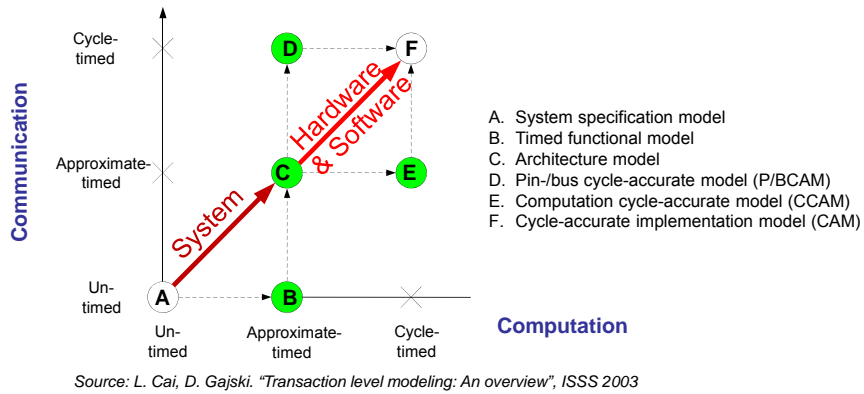
Abstraction Levels



Computation vs. Communication

➤ **System design flow**

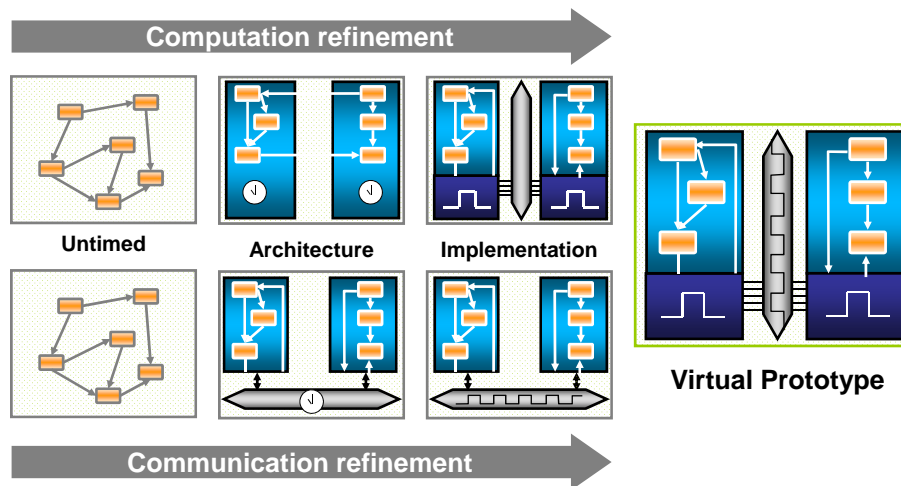
➤ Path from model A to model F



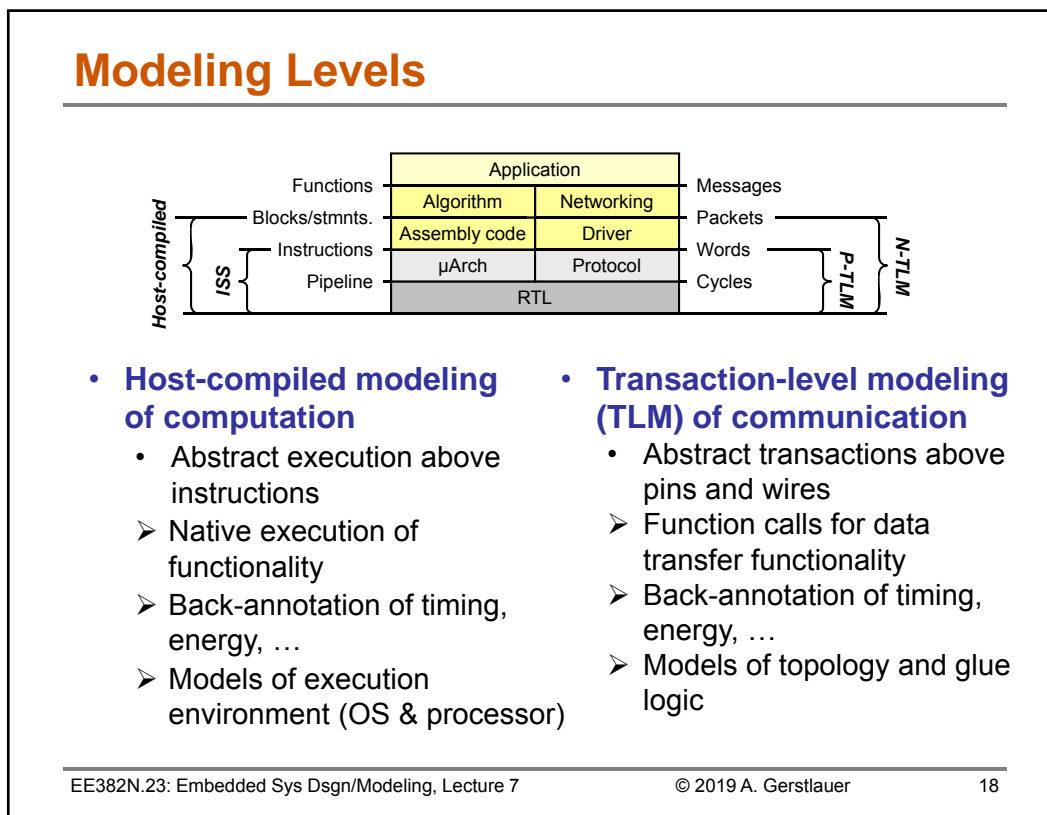
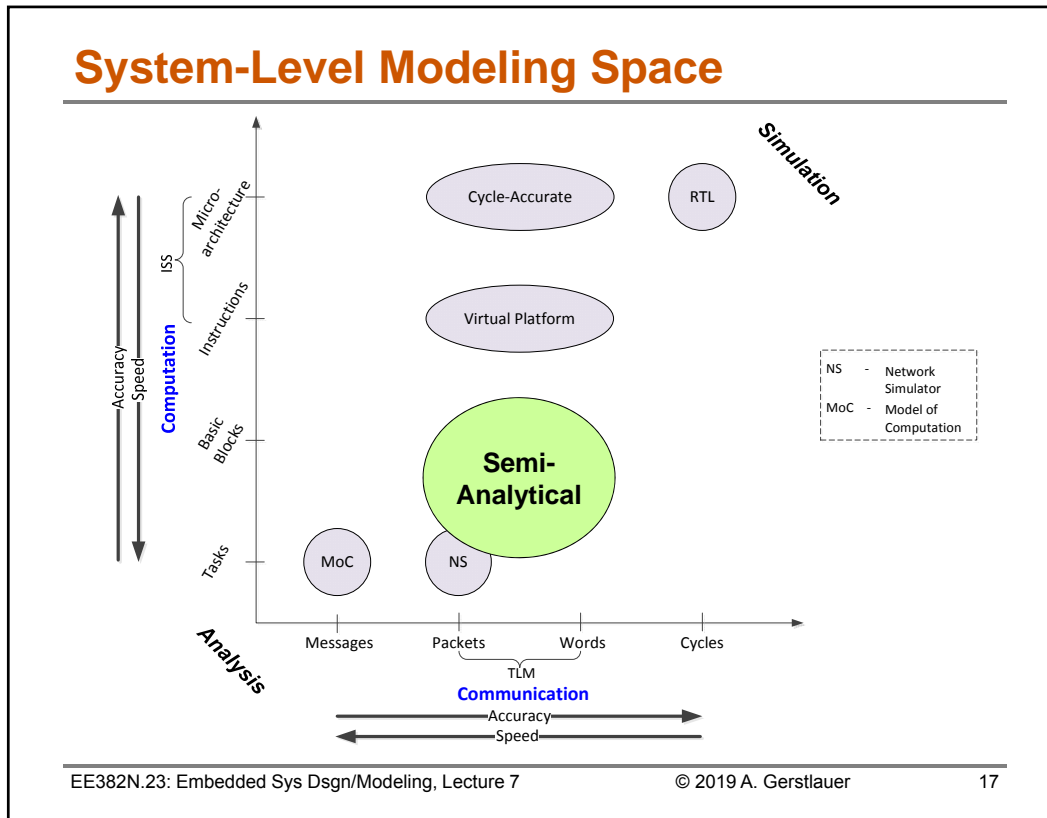
➤ **Design methodology and modeling flow**

➤ Set of models and transformations between models

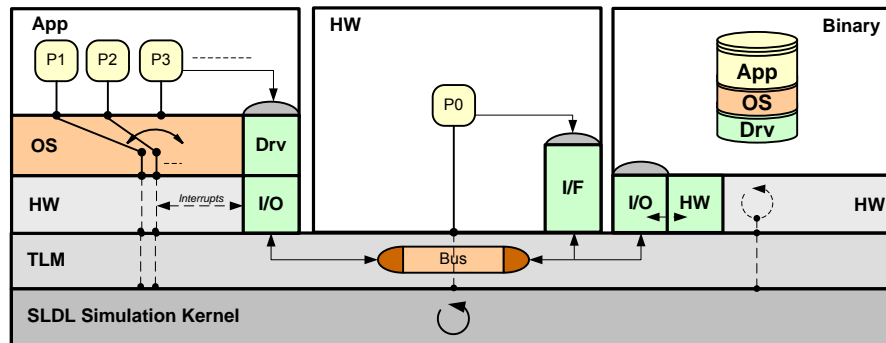
Virtual Platform Prototyping



Source: C. Haubelt, Univ. of Rostock



Virtual Platform Models



- **CPU model**
 - Source-level timing, energy, .. back-annotation
 - OS & processor models
 - **Hardware/IP model**
 - Functional model
 - Timing, energy, ... back-annotation
 - **ISS model**
 - Cycle-accurate [GEM5]
 - Functional [QEMU] + timing, energy, ... back-annotation
- **System-level design language (SLDL) & TLM backplane [SystemC]**

Lecture 7: Summary

- **System-level design flow**
 - Decision making + refinement
- **System refinement**
 - Structure and timing
- **System modeling**
 - Computation and communication