# EE382V-SoC-ICS, Fall 2009 -- HW #2

**Assigned: Sep 18th, 2009 Due: Oct 16th, 2009**

## Instructions:

- Please submit your solutions via Blackboard. Submissions should include a single PDF with the writeup.
- You may discuss the problems with your classmates but make sure to submit your own independent and individual solutions.

## Problem: Algorithmic Mapping

Consider an embedded system for portable video scene analysis used for identification and recognition of numerals on the sides of cargo containers. The recognition process takes a frame of high-resolution video as input and produces from zero to several recognized number sequences as output. When number recognition is disabled, the system performs to specification using a single general-purpose processor and a dedicated digital video input subsystem. Profiling indicates that the general-purpose processor would be 100% consumed by the number recognition task. You are asked to provide a solution using one of three options:

1) Add a second general-purpose processor
2) Add a programmable DSP subsystem
3) Add a fixed-function hardware accelerator

**Questions to be answered:**

a) What general tradeoffs do you see among these approaches?

b) What mechanism would you suggest for having this new subsystem access the relatively large amounts of input data it requires?

c) How would you control execution on the new subsystem from the perspective of the existing processor?

d) How do you propose the new subsystem notify the existing processor when a number is detected?