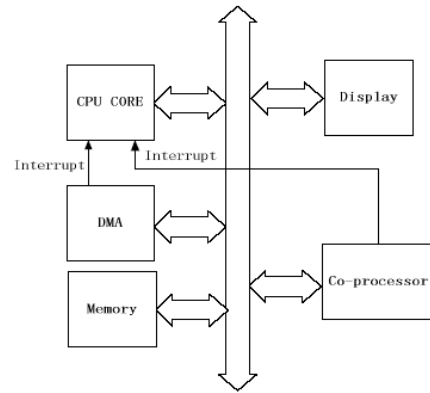


Problem: Task Scheduling (20 Points)

This is a simple single microprocessor core platform with a video coprocessor, which is configured to process 32 bytes of video data and produce a 1 byte result. Each display frame contains 30 X 10 words of data. The CPU or the DMA is used to transfer data between the memory, display or coprocessor.

The bus cycle count for each transaction is:

- CPU CORE can access data from any module.
 - Requires 3 bus cycles of overhead for each bus cycle. Remember it requires a load and store to move any word.
- DMA is Direct Memory Access module which can be used to transfer data between the memory block, the display module or co-processor module.
 - 15 bus cycles for CPU to configure the DMA controller.
 - 2 cycles per data word transfer (one read, one write).
- Access times (read and write):
 - Memory: 1 bus cycle in addition to any overhead.
 - Co-processor: 4 bus cycles in addition to any overhead
 - Display: 165 bus cycles for each word in addition to any overhead cycles
- Interrupt
 - The coprocessor and display module will generate interrupt after completing their tasks
 - Interrupt subroutine takes 100 bus cycles.
- Co-processor cycle times:
 - CPU CORE or DMA will write 32 data words to the coprocessor. The coprocessor will start processing the data **after** the CPU CORE or DMA writes a one word **command**. It will take 170 cycles for the co-processor to process the data and the result is 1 word, i.e., the coprocessor compresses 32 words down to one word. The CPU CORE or DMA will read the word in the coprocessor and transfer it.
- All ports and buses width are 1 word wide (32 bits)
- You cannot do more than one transfer on the bus at one time.



Question: What is the minimum number of bus cycles that it will take to process one frame of data (each frame is 30 X 10 words)? Use back of this page to show your work and any assumptions that you make.

Problem: Product Definition (20 Points)

What are the essential factors to be considered and analyzed at the architectural definition phase of a portable wireless terminal?

Answer:

Problem: System Level Languages (25 Points)

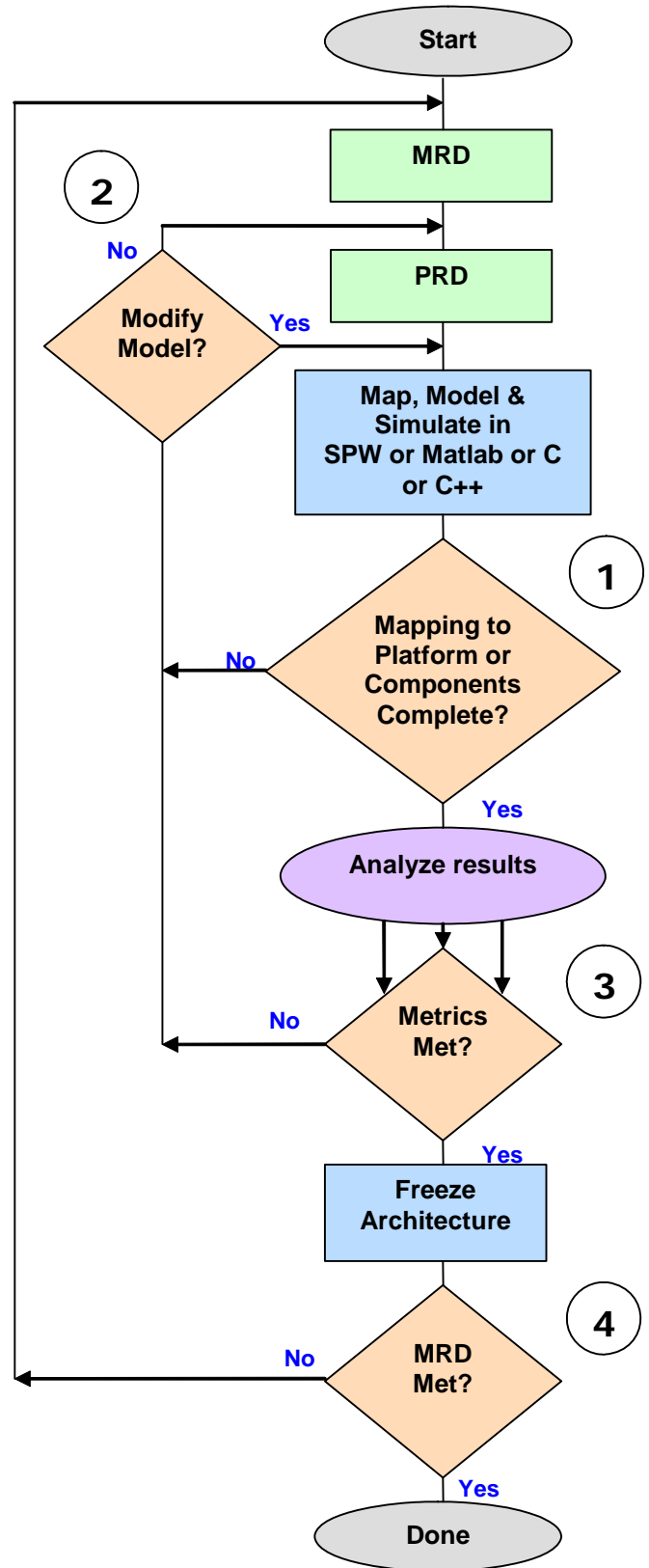
In recent years, there has been an increasing focus on electronic system-level (ESL) modeling languages, such as SystemC. Discuss the factors driving the high interest in ESL languages, and how such languages hope to address those issues.

Answer:

Problem: Design Methodology (25 Points)

Explain in detail what decisions are being made in this flow chart? Hint: there are 4 decision points. Use the back of the sheet if you need more room to write.

Answer:



Problem: SOC Definition (25 Points)

In the definition phase of a SoC architecture, a number of technical factors are considered for the implementation and mapping of the appropriate algorithms. Describe in detail with an application such as a wireless terminal the factors you would consider essential for achieving your goal.

Answer:

Problem: Task Scheduling (25 Points)

Consider a system comprised of three processes with the following execution times and periods:

Execution time	Period
$T_1 = 1$	$\tau_1 = 10$
$T_2 = 1$	$\tau_2 = 2$
$T_3 = 2$	$\tau_3 = 5$

Give a rate-monotonic-schedule (RMS) for the processes, and indicate the corresponding processor utilization. Could an early-deadline-first (EDF) scheduler also generate this schedule? Justify your answer (hint: give the EDF dynamic priorities at each relevant time step).

Answer:

Problem (20 Points)

A system requires the computation of the equation, $x^3 + A.x^2 + B.x + C$.

(a) If only two operations (multiplications or additions) can be done in one cycle, schedule the operations in order to complete the computation in the minimum number of cycles.



Use these symbols to represent the multiplication and addition.

(b) In order to reduce power, only one operation (multiplication or addition) can be done in one cycle. Find the schedule which obeys this constraint and takes the minimum number of cycles.

Problem. (20 Points)

Given the inner loop of the BCH encoding algorithm in C below, identify the number of XOR and AND operations performed in the loop as a function of k . Assume that $length = 1024$, and that in any bit position, a 0 and a 1 are equally likely.

```

encode_bch()
/*
 * Compute redundancy bb[], the coefficients of b(x). The redundancy
 * polynomial b(x) is the remainder after dividing  $x^{length-k} \cdot data(x)$ 
 * by the generator polynomial g(x).
 * k = dimension (no. of information bits/codeword) of the code
 */
{
    register int    i, j;
    register int    feedback;

    for (i = 0; i < length - k; i++)
        bb[i] = 0;
    for (i = k - 1; i >= 0; i--) {
        feedback = data[i] ^ bb[length - k - 1];
        if (feedback != 0) {
            for (j = length - k - 1; j > 0; j--)
                if (g[j] != 0)
                    bb[j] = bb[j - 1] ^ feedback;
                else
                    bb[j] = bb[j - 1];
            bb[0] = g[0] && feedback;
        } else {
            for (j = length - k - 1; j > 0; j--)
                bb[j] = bb[j - 1];
            bb[0] = 0;
        }
    }
}

```

Answer: