DRM Class Project

EE382V-SoC
Fall 2009

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Project Description

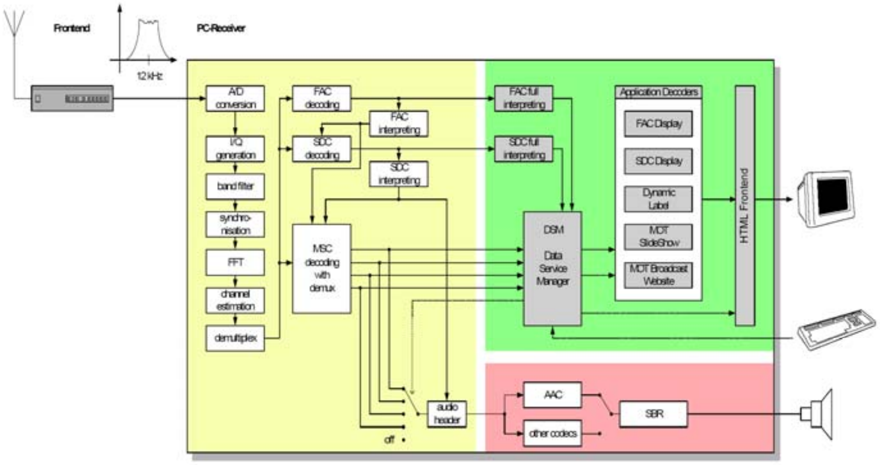
The class will be assigned to teams to do the various components of the design. The intent of the project is to do a HW/SW co-design of an embedded SOC. The design is a low power SOC implementation of the public domain DRM software implementation. We will use both a virtual platform (ARM) and a hardware platform (TLL5000-TLL6219) to simulate the design.

These platforms consist of an ARM processor, I/O devices, memory components, hardware accelerators interconnected via a standard bus.

Project Objectives and Activities

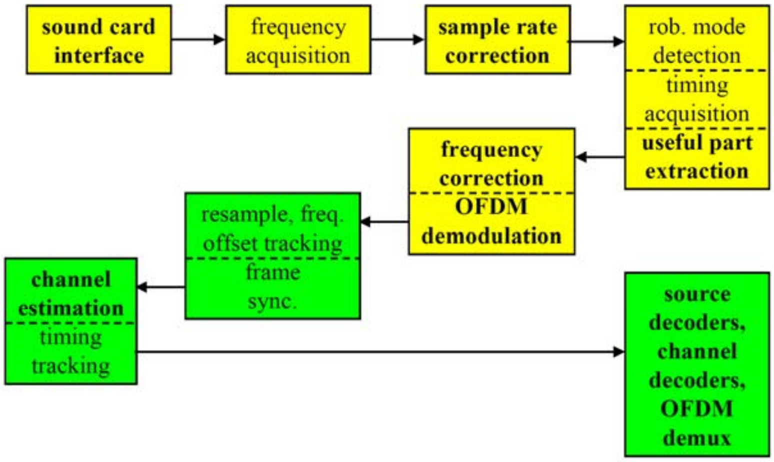
- **The objectives of the project are as follows:**
  1. Implement the DRM C++ code on a ARM based platform while meeting the performance, area and power metrics.
- **The project activities include:**
  - Optimize the DRM C++ software for fixed point operation
  - Profile the updated DRM C++ software implementation to determine performance bottlenecks
  - Convert time critical functions to pseudo ANSI-C/SystemC code. Synthesize C code to Verilog for gate level implementation
  - Partition the software into components which will run on the ARM processor and on the hardware accelerators
  - Co-simulate and co-verify the HW/SW implementation
  - Develop a high level power model of the system

DRM PC Based System Architecture

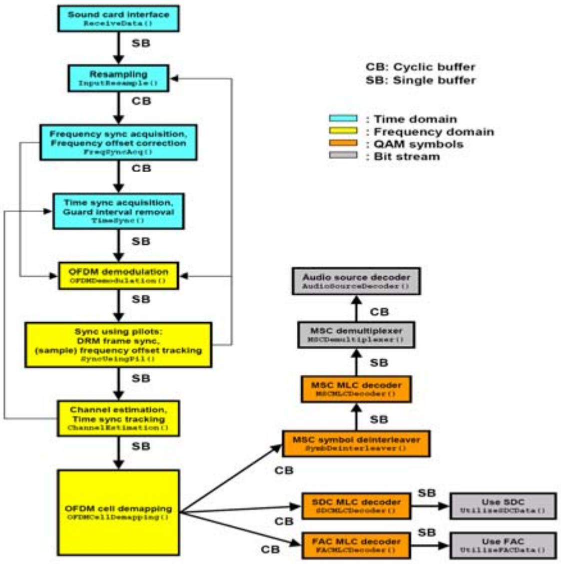


DRM code is designed to run on a desktop computer

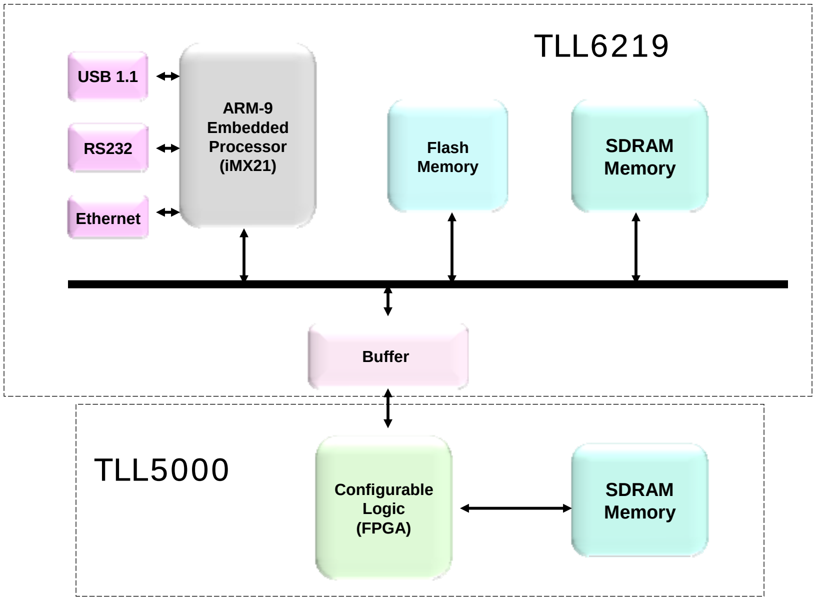
DRM Software Overview



DRM SW System Architecture



High Level HW Architecture



HW Development Tasks

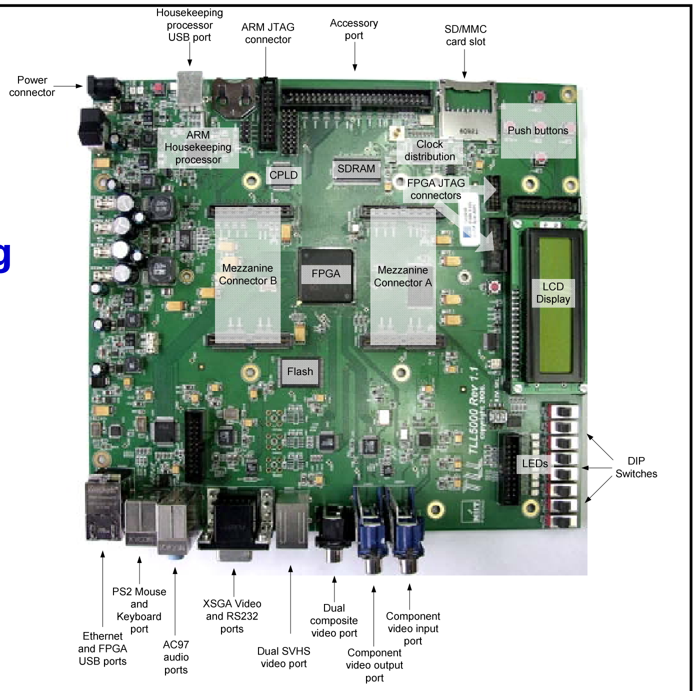
- **Develop the following FPGA modules:**
  - Memory Controller
  - Interface to ARM Board and on chip bus
  - Hardware Accelerators (using Catapult code)
  - Clocking & Reset
  - Interrupt logic
  - Diagnostics

Software based tasks

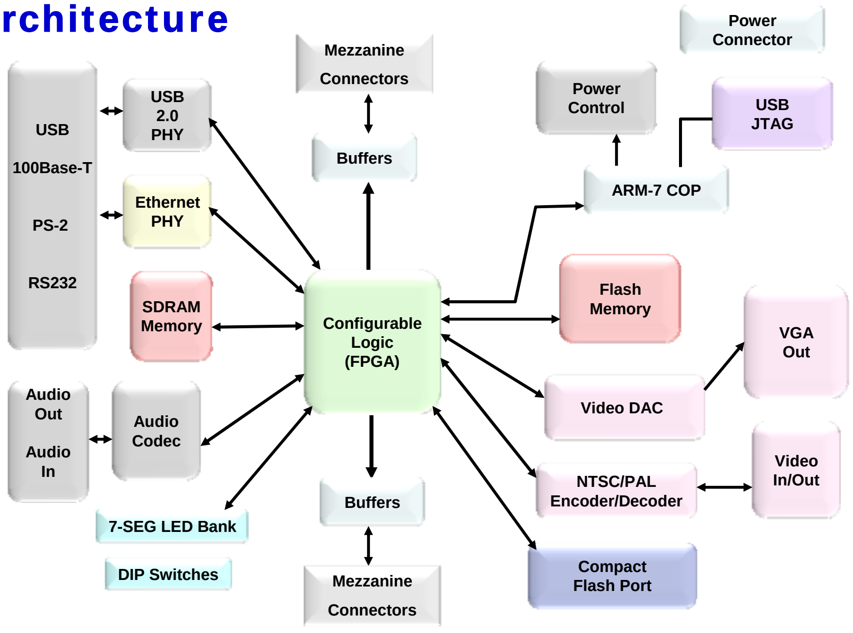
- **Compile FLP DRM and get it running on ARM board**
  - Profile code on ARM board
- **Convert FLP -> FXP in DRM code**
  - Run SNR checks
  - Modify conversion as needed
- **Compile FXP DRM and get it running on ARM board**
  - Profile code on ARM board
- **Develop streaming I/O handler**
- **Develop interrupt handler**
- **Develop HAL**

TLL500 Prototyping Board

TLL5000 Prototyping Platform



TLL 5000 Architecture



Power Connector

Mezzanine Connectors

Power Control

USB JTAG

USB

100Base-T

PS-2

RS232

USB 2.0 PHY

Buffers

ARM-7 COP

Ethernet PHY

SDRAM Memory

Configurable Logic (FPGA)

Flash Memory

VGA Out

Audio Out

Audio In

Audio Codec

Video DAC

Video In/Out

NTSC/PAL Encoder/Decoder

Buffers

7-SEG LED Bank

DIP Switches

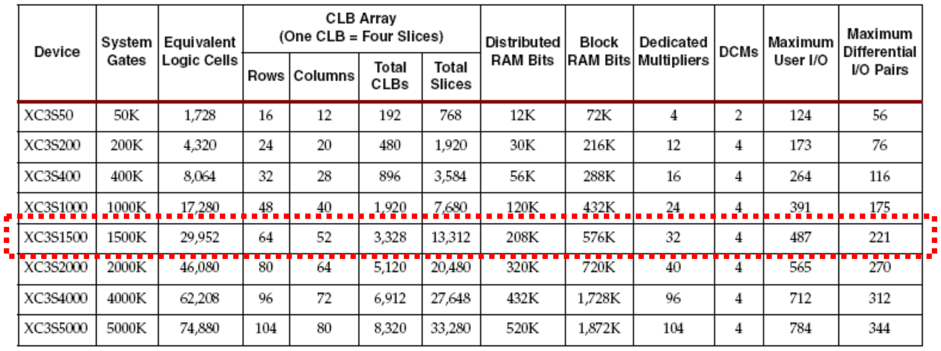
Mezzanine Connectors

Compact Flash Port

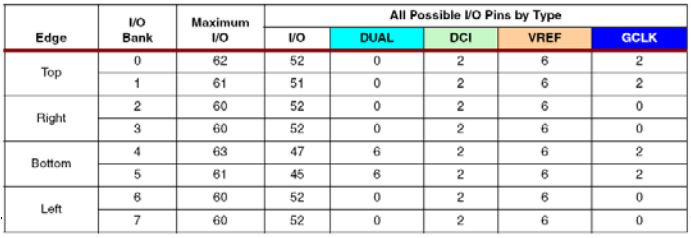
Xilinx Spartan 3 FPGA

- **Spartan 3 XC3S1500 Discussion**
  - Overview
  - Logic Resources
  - Memory Resources
  - Clock Resources
  - Input/Output Resources

Spartan 3 Overview



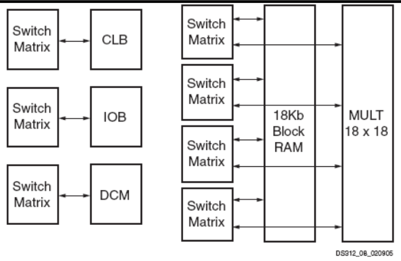
Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM Bits	Block RAM Bits	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S50	50K	1,728	16	12	192	768	12K	72K	4	2	124	56
XC3S200	200K	4,320	24	20	480	1,920	30K	216K	12	4	173	76
XC3S400	400K	8,064	32	28	896	3,584	56K	288K	16	4	264	116
XC3S1000	1000K	17,280	48	40	1,920	7,680	120K	432K	24	4	391	175
XC3S1500	1500K	29,952	64	52	3,328	13,312	208K	576K	32	4	487	221
XC3S2000	2000K	46,080	80	64	5,120	20,480	320K	720K	40	4	565	270
XC3S4000	4000K	62,208	96	72	6,912	27,648	432K	1,728K	96	4	712	312
XC3S5000	5000K	74,880	104	80	8,320	33,280	520K	1,872K	104	4	784	344

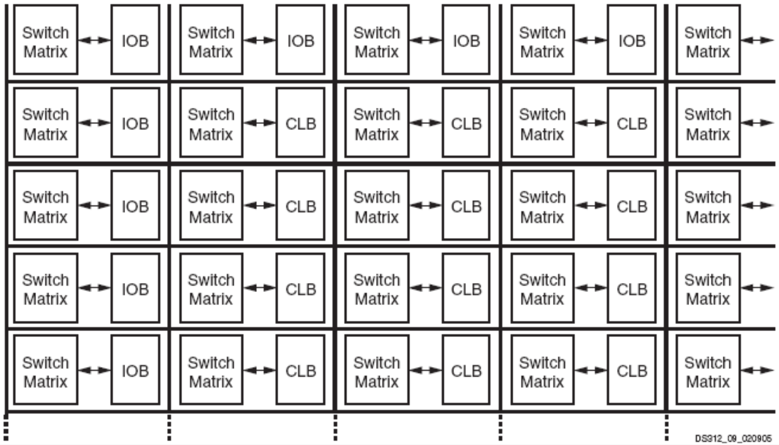


Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	DUAL	DCI	VREF	GCLK
Top	0	62	52	0	2	6	2
	1	61	51	0	2	6	2
Right	2	60	52	0	2	6	0
	3	60	52	0	2	6	0
Bottom	4	63	47	6	2	6	2
	5	61	45	6	2	6	2
Left	6	60	52	0	2	6	0
	7	60	52	0	2	6	0

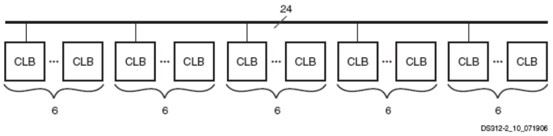
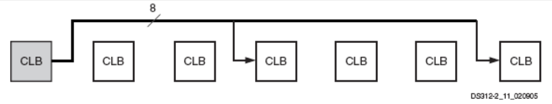
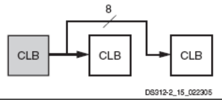
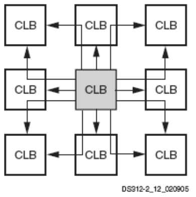
Interconnect Matrix

- Channels contain various connection resources



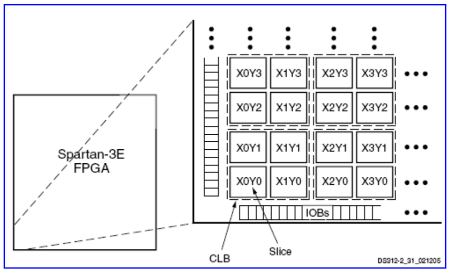


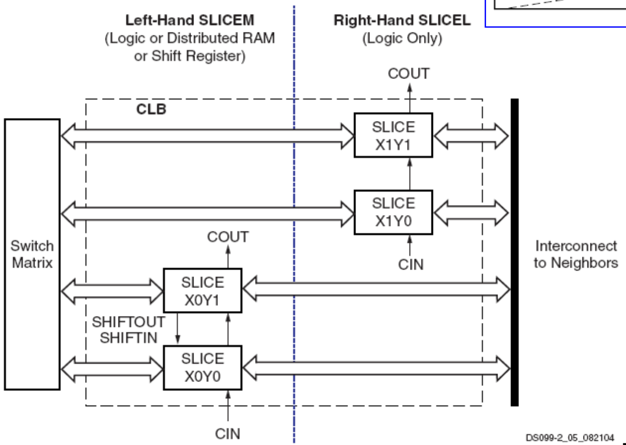
Channel Interconnects

Horizontal and Vertical Long Lines (horizontal channel shown as an example)	
Horizontal and Vertical Hex Lines (horizontal channel shown as an example)	
Horizontal and Vertical Double Lines (horizontal channel shown as an example)	
Direct Connections	

CLBs & Slices

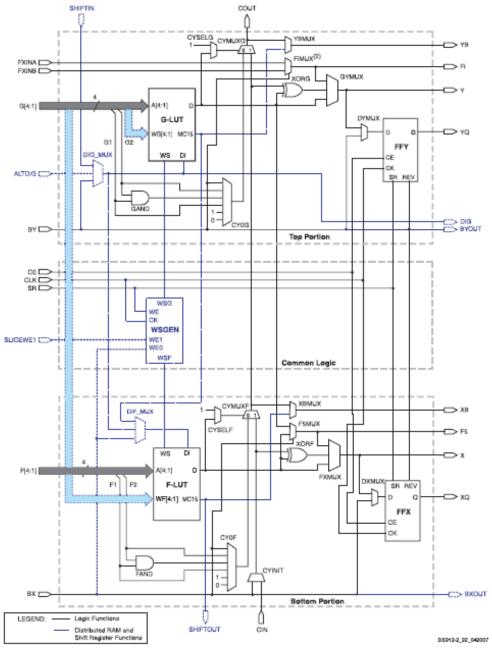
- Each slice has 2 LUTs & 2 storage elements



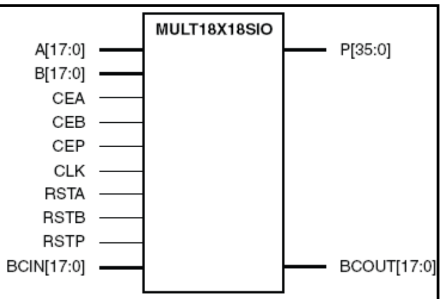


CLB Slice

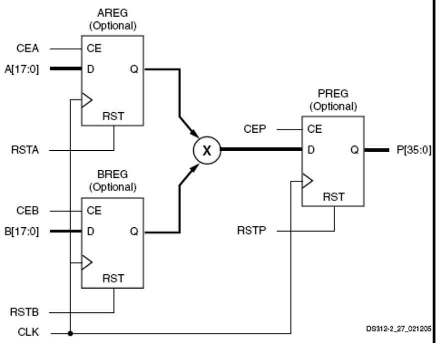
- 2 FFs or latches
- 2 LUTs for combinational logic
- Some LUTs can be used as distributed RAM or ROM, or shift registers
- Carry look-ahead
- Dedicated muxes



Multipliers

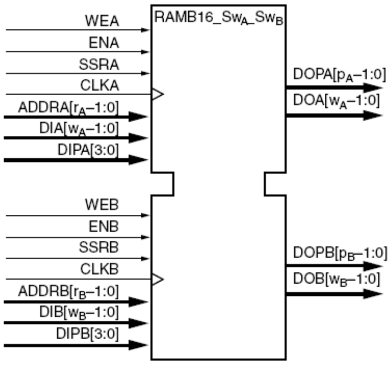


- 2’s-complement multipliers distributed across fabric
  - Primarily to support DSP
    - Cascade connections
  - Pipeline registers on inputs and outputs
  - Can do 2 small width op
- Can also be used for
  - Barrel shifters
  - Data storage
- Some shared connections with adjacent block RAM

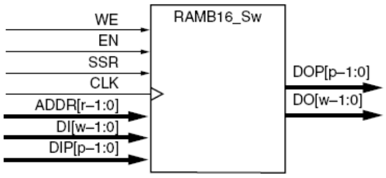


Block RAM

Device	Total Number of RAM Blocks	Total Addressable Locations (bits)	Number of Columns
XC3S50	4	73,728	1
XC3S200	12	221,184	2
XC3S400	16	294,912	2
XC3S1000	24	442,368	2
XC3S1500	32	589,824	2
XC3S2000	40	737,280	2
XC3S4000	96	1,769,472	4
XC3S5000	104	1,916,928	4



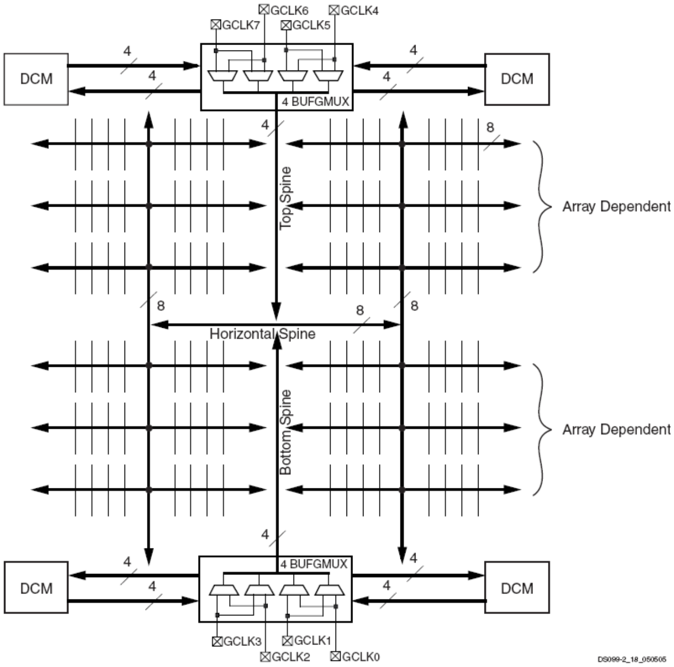
(a) Dual-Port



(b) Single-Port

There is no dedicated monitor to arbitrate the result of identical addresses on both ports. The application must time the two clocks appropriately. However, conflicting simultaneous writes to the same location never cause any physical damage.

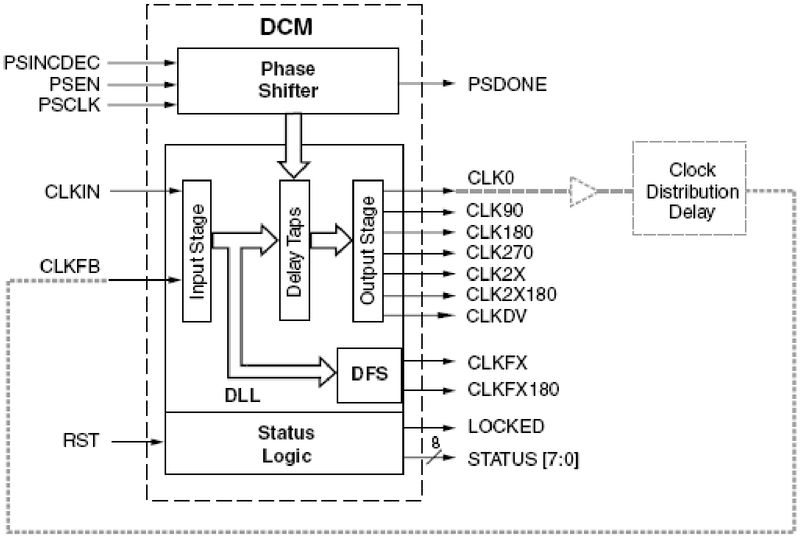
Clock Network



Digital Clock Manager (DCM)

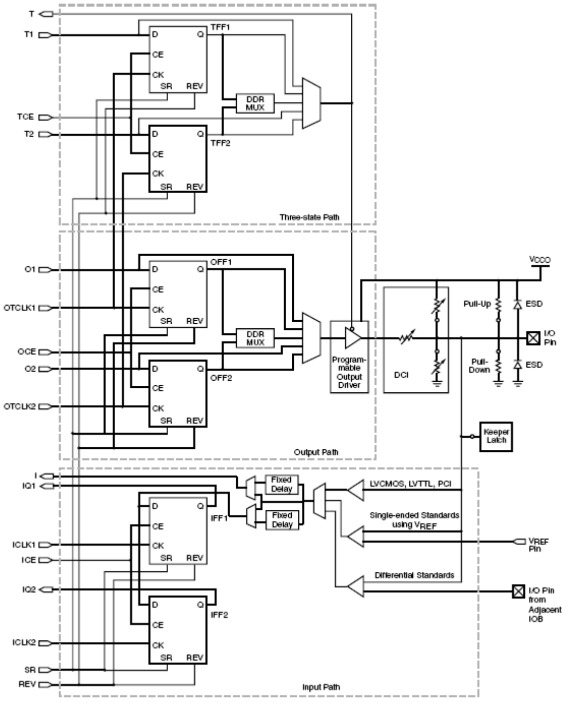
- DCM functions
  - Eliminate clock skew using Delay-Locked Loop (DLL)
    - Monitors clock skew on output and corrects
    - Performs frequency doubling
    - Creates multiphase clocks
  - Fractional Digital Frequency Synthesizer (DFS)
    - fOUT = M/N fIN
  - Clock conditioning
  - Clock buffering and signal translation

Digital Clock Manager (DCM)



Input/Output Block (IOB)

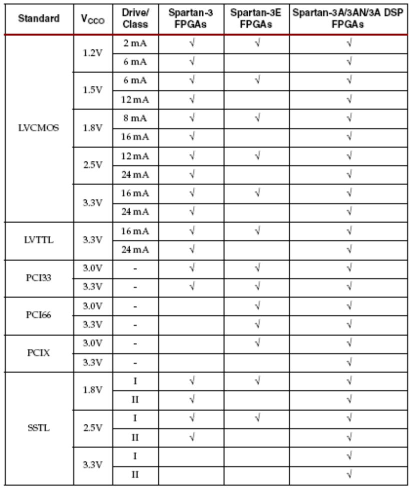
- Slew rate and drive strength control
- Pull-up, pull-down and keeper
- DDR signals
- Controlled-Z input/output
- Boundary scan



Note: All IOB signals originating from the FPGA's internal logic have an optional polarity inverter.

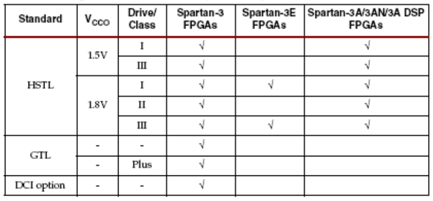
I/O Standards

Table 1-8: Single-Ended I/O Standards



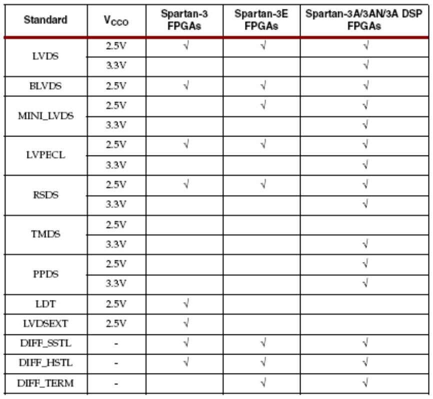
Standard	V_{CCO}	Drive/ Class	Spartan-3 FPGAs	Spartan-3E FPGAs	Spartan-3A/3AN/3A DSP FPGAs
LVCMOS	1.2V	2 mA	√	√	√
		6 mA	√		√
	1.5V	6 mA	√	√	√
		12 mA	√		√
	1.8V	8 mA	√	√	√
		16 mA	√		√
	2.5V	12 mA	√	√	√
		24 mA	√		√
	3.3V	16 mA	√	√	√
		24 mA	√		√
LVTTL	3.3V	16 mA	√	√	√
		24 mA	√		√
PCI33	3.0V	-	√	√	√
	3.3V	-	√	√	√
PCI66	3.0V	-		√	√
	3.3V	-		√	√
PCIX	3.0V	-		√	√
	3.3V	-			√
SSTL	1.8V	I	√	√	√
		II	√		√
	2.5V	I	√	√	√
		II	√		√
	3.3V	I			√
		II			√

Table 1-8: Single-Ended I/O Standards *(Continued)*



Standard	V_{CCO}	Drive/ Class	Spartan-3 FPGAs	Spartan-3E FPGAs	Spartan-3A/3AN/3A DSP FPGAs
HSTL	1.5V	I	√		√
		III	√		√
	1.8V	I	√	√	√
		II	√		√
		III	√	√	√
GTL	-	-	√		
	-	Plus	√		
DCI option	-	-	√		

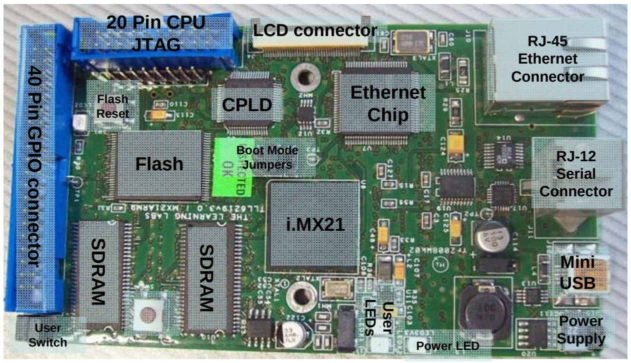
Table 1-9: Differential I/O Standards



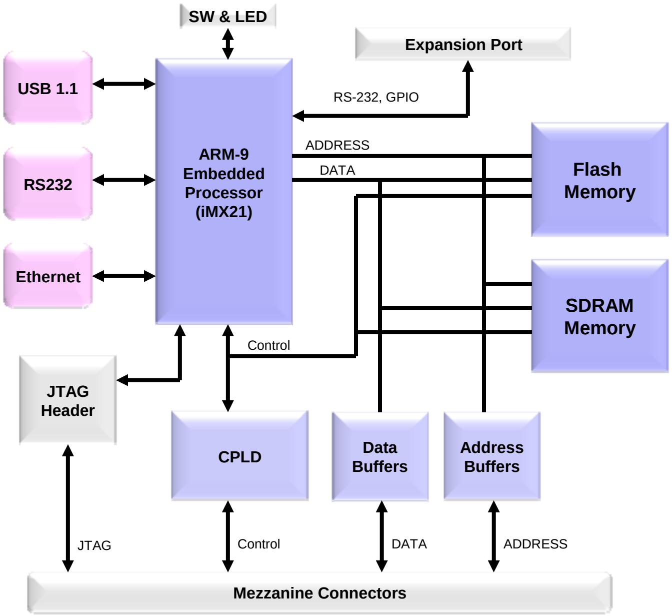
Standard	V_{CCO}	Spartan-3 FPGAs	Spartan-3E FPGAs	Spartan-3A/3AN/3A DSP FPGAs
LVDS	2.5V	√	√	√
	3.3V			√
BLVDS	2.5V	√	√	√
MINI_LVDS	2.5V		√	√
	3.3V			√
LVPECL	2.5V	√	√	√
	3.3V			√
RSDS	2.5V	√	√	√
	3.3V			√
TMDS	2.5V			
	3.3V			√
PPDS	2.5V			√
	3.3V			√
LDT	2.5V	√		
LVDSEXT	2.5V	√		
DIFF_SSTL	-	√	√	√
DIFF_HSTL	-	√	√	√
DIFF_TERM	-		√	√

TLL6219 ARM Processor Board

TLL6219 ARM Processor Board



TLL6219 Block Diagram



SW & LED

Expansion Port

USB 1.1

RS232

Ethernet

ARM-9 Embedded Processor (iMX21)

RS-232, GPIO

ADDRESS

DATA

Flash Memory

SDRAM Memory

Control

JTAG Header

CPLD

Data Buffers

Address Buffers

JTAG

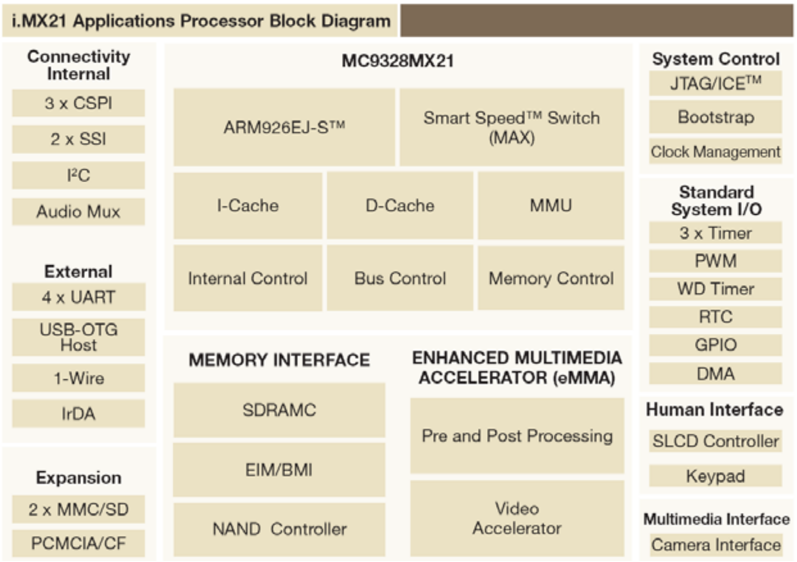
Control

DATA

ADDRESS

Mezzanine Connectors

i.MX21 Features



i.MX21 Applications Processor Block Diagram

Connectivity Internal
- 3 x CSPI
- 2 x SSI
- I²C
- Audio Mux

External
- 4 x UART
- USB-OTG Host
- 1-Wire
- IrDA

Expansion
- 2 x MMC/SD
- PCMCIA/CF

MC9328MX21
- ARM926EJ-S™
- Smart Speed™ Switch (MAX)
- I-Cache
- D-Cache
- MMU
- Internal Control
- Bus Control
- Memory Control

MEMORY INTERFACE
- SDRAMC
- EIM/BMI
- NAND Controller

ENHANCED MULTIMEDIA ACCELERATOR (eMMA)
- Pre and Post Processing
- Video Accelerator

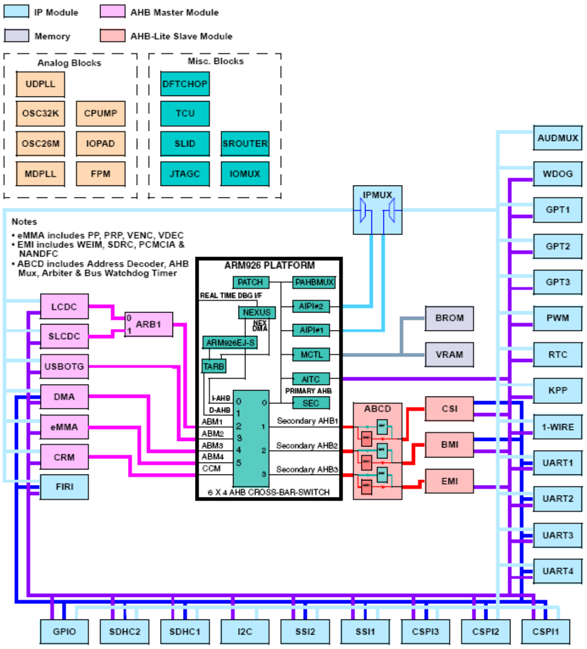
System Control
- JTAG/ICE™
- Bootstrap
- Clock Management

Standard System I/O
- 3 x Timer
- PWM
- WD Timer
- RTC
- GPIO
- DMA

Human Interface
- SLCD Controller
- Keypad

Multimedia Interface
- Camera Interface

Block Diagram



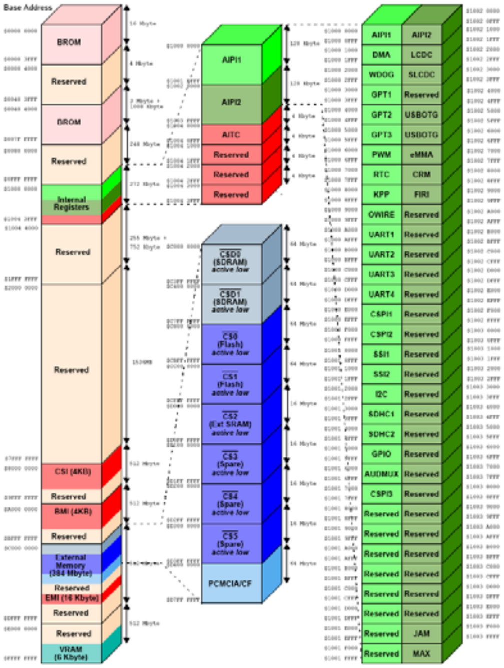
Notes
- eMMA includes PP, PRP, VENC, VDEC
- EMI includes WEIM, SDRC, PCMCIA & NANDFC
- ABCD includes Address Decoder, AHB Mux, Arbiter & Bus Watchdog Timer

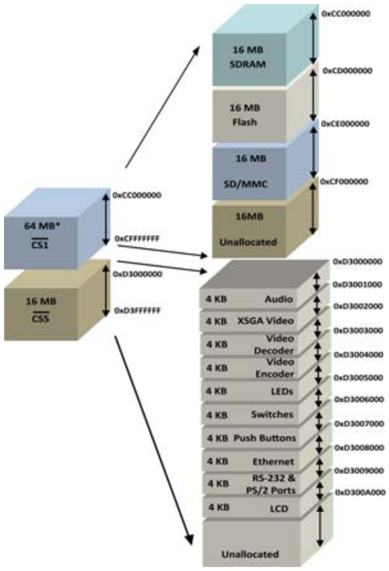
iMX21 Memory Map

There are eight 512MB partitions

Address	Size	Usage
0x00000000	512 Mbyte	ROM, Primary AHB Slaves, and Peripherals
0x20000000	512 Mbyte	Reserved
0x40000000	512 Mbyte	Reserved
0x60000000	512 Mbyte	Reserved
0x80000000	512 Mbyte	Secondary AHB Slave Port 1
0xA0000000	512 Mbyte	Secondary AHB Slave Port 2
0xC0000000	512 Mbyte	Secondary AHB Slave Port 3
0xE0000000	512 Mbyte	Primary AHB (RAM)

iMX21 Memory Map Details





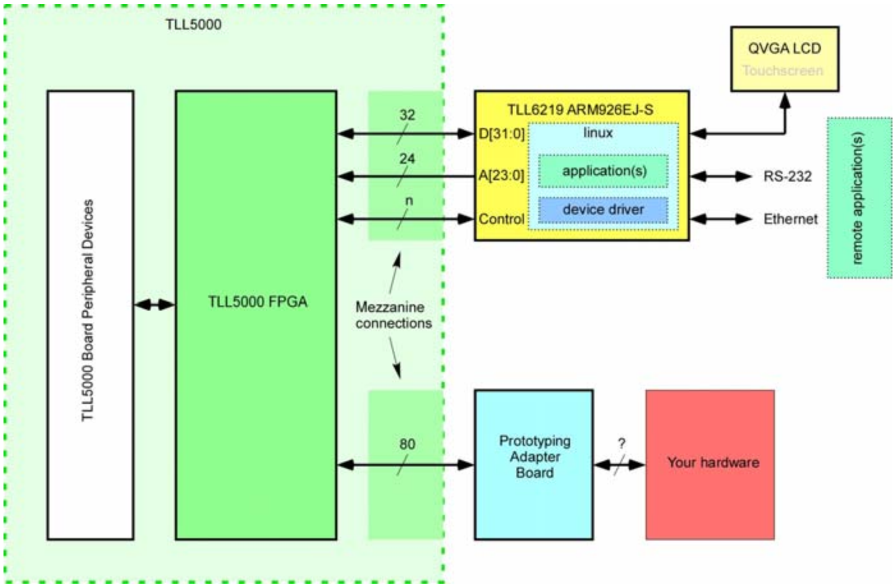
TLL6219 ARM926EJ-S Board

- **External interfaces**
  - RS-232 serial port
  - Ethernet
  - USB-OTG (Linux host driver for flash disk)
  - Graphic LCD panel
- **TLL5000 Interface**
  - External memory interface
    - /CS1, /CS5 memory regions
    - D[31:0], A[23:0], control signals (thru CPLD)
  - Connections to TLL6219 CPLD

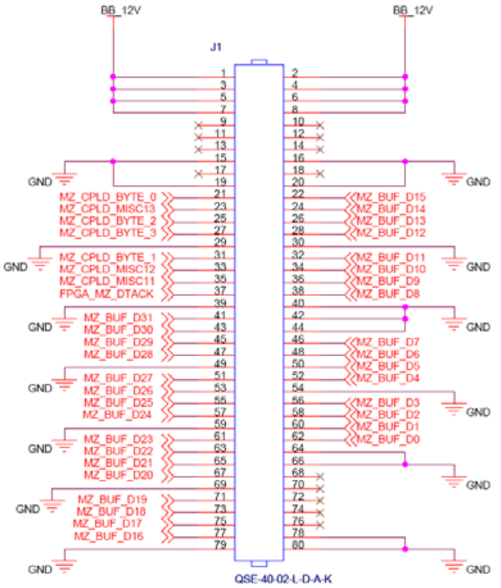
Interface from ARM to FPGA

- All access from the ARM9 to hardware will be through the Chip Select 1 & 5 memory regions
- All TLL5000 peripherals must be accessed through the FPGA
- The only direct connection to the ARM9 is
  - QVGA LCD with touchscreen
  - RS-232
  - Ethernet

System Block Diagram

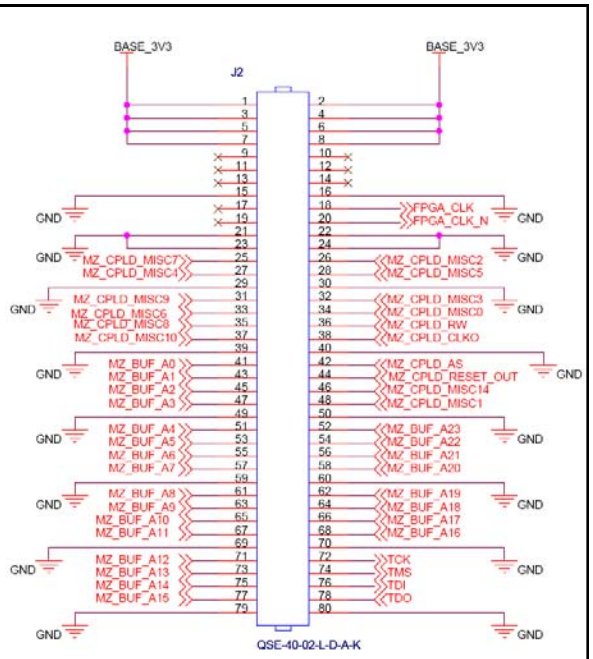


TLL6219 Mezzanine Connector A


BB_12V
BB_12V
J1
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
GND 17 18 GND
19 20
MZ_CPLD_BYTE_0 21 22 MZ_BUF_D15
MZ_CPLD_MISC13 23 24 MZ_BUF_D14
MZ_CPLD_BYTE_2 25 26 MZ_BUF_D13
MZ_CPLD_BYTE_3 27 28 MZ_BUF_D12
29 30
GND MZ_CPLD_BYTE_1 31 32 MZ_BUF_D11 GND
MZ_CPLD_MISC12 33 34 MZ_BUF_D10
MZ_CPLD_MISC11 35 36 MZ_BUF_D9
FPGA_MZ_DTACK 37 38 MZ_BUF_D8
39 40
GND MZ_BUF_D31 41 42 GND
MZ_BUF_D30 43 44
MZ_BUF_D29 45 46 MZ_BUF_D7
MZ_BUF_D28 47 48 MZ_BUF_D6
49 50 MZ_BUF_D5
GND MZ_BUF_D27 51 52 MZ_BUF_D4
MZ_BUF_D26 53 54
MZ_BUF_D25 55 56 MZ_BUF_D3 GND
MZ_BUF_D24 57 58 MZ_BUF_D2
59 60 MZ_BUF_D1
GND MZ_BUF_D23 61 62 MZ_BUF_D0
MZ_BUF_D22 63 64
MZ_BUF_D21 65 66
MZ_BUF_D20 67 68 GND
69 70
GND MZ_BUF_D19 71 72
MZ_BUF_D18 73 74
MZ_BUF_D17 75 76
MZ_BUF_D16 77 78
79 80
GND GND
QSE-40-02-L-D-A-K

MEZZANINE CONNECTOR I

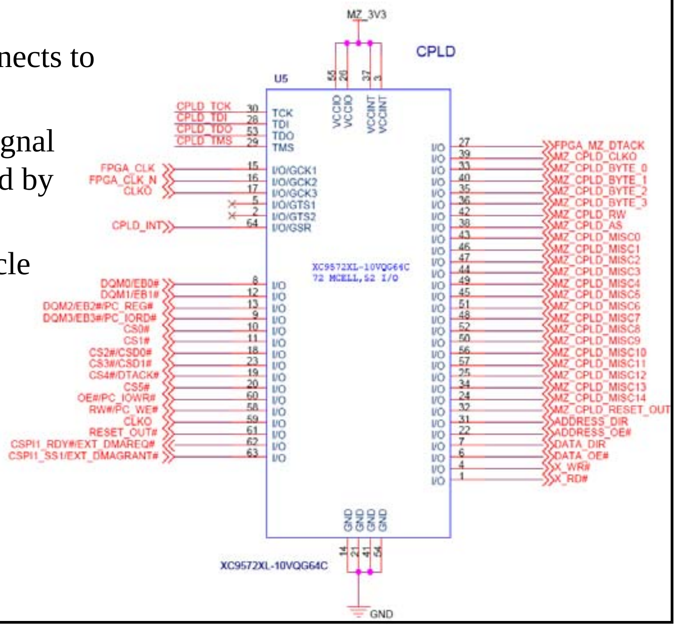
TLL6219 Mezzanine Connector B


BASE_3V3
BASE_3V3
J2
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18 FPGA_CLK
GND 19 20 FPGA_CLK_N GND
21 22
23 24
GND MZ_CPLD_MISC7 25 26 MZ_CPLD_MISC2 GND
MZ_CPLD_MISC4 27 28 MZ_CPLD_MISC5
29 30
MZ_CPLD_MISC9 31 32 MZ_CPLD_MISC3
GND MZ_CPLD_MISC6 33 34 MZ_CPLD_MISC0 GND
MZ_CPLD_MISC8 35 36 MZ_CPLD_RW
MZ_CPLD_MISC10 37 38 MZ_CPLD_CLKO
39 40
MZ_BUF_A0 41 42 MZ_CPLD_AS
GND MZ_BUF_A1 43 44 MZ_CPLD_RESET_OUT GND
MZ_BUF_A2 45 46 MZ_CPLD_MISC14
MZ_BUF_A3 47 48 MZ_CPLD_MISC1
49 50
MZ_BUF_A4 51 52 MZ_BUF_A23
GND MZ_BUF_A5 53 54 MZ_BUF_A22 GND
MZ_BUF_A6 55 56 MZ_BUF_A21
MZ_BUF_A7 57 58 MZ_BUF_A20
59 60
MZ_BUF_A8 61 62 MZ_BUF_A19
GND MZ_BUF_A9 63 64 MZ_BUF_A18 GND
MZ_BUF_A10 65 66 MZ_BUF_A17
MZ_BUF_A11 67 68 MZ_BUF_A16
69 70
MZ_BUF_A12 71 72 TCK
GND MZ_BUF_A13 73 74 TMS GND
MZ_BUF_A14 75 76 TDI
MZ_BUF_A15 77 78 TDO
79 80
GND GND
QSE-40-02-L-D-A-K

MEZZANINE CONNECTOR II

TLL6219 CPLD Connections

- CPLD_INT connects to PF[16]
- MISC[xxxxx] signal functions defined by CPLD
- /DTACK for cycle timing



TLL6219 CPLD Overview

- The CPLD generates read and write strobes for accesses in the /CS1 and /CS5 spaces (combinational logic)
  - cs1_rs_b = ~(~cs1_b & ~oe_b);
  - cs1_ws_b = ~(~cs1_b & ~(&eb) & ~rw_b);
  - cs5_rs_b = ~(~cs5_b & ~oe_b);
  - cs5_ws_b = ~(~cs5_b & ~(&eb) & ~rw_b);
- /DTACK is synchronized in the CPLD
  - Single flip-flop synchronizer

TLL6219 CPLD_MISC[] Pins

mz_cpld_misc[0] = cs1_rs_b;	/CS1 read strobe (active-low)
mz_cpld_misc[1] = cs1_ws_b;	/CS1 write strobe (active-low)
mz_cpld_misc[2] = cs5_rs_b;	/CS5 read strobe (active-low)
mz_cpld_misc[3] = cs5_ws_b;	/CS5 write strobe (active-low)
mz_cpld_misc[4] = oe_b;	from ARM926
mz_cpld_misc[5] = cs0_b;	from ARM926 (flash memory)
mz_cpld_misc[6] = cs1_b;	from ARM926 (FPGA access)
mz_cpld_misc[7] = cs2_b;	from ARM926 (SDRAM)
mz_cpld_misc[8] = cs3_b;	from ARM926 (Ethernet)
mz_cpld_misc[9] = cs5_b;	from ARM926 (FPGA access)
mz_cpld_misc[10] = nfio4;	TLL6219 jumper
mz_cpld_misc[11] = nfio5;	TLL6219 jumper
mz_cpld_misc[12] = data_dir;	TLL6219 transceiver control
mz_cpld_misc[13] = data_oe;	TLL6219 transceiver control
mz_cpld_misc[14] = fpga_interrupt;	FPGA IRQ to ARM926 PF[16]

TLL6219 Transceiver Control

- **The NFIO4 jumper is used to control data transceiver operation when the ARM926 is NOT accessing /CS1 or /CS5 space**
- **If the jumper is NOT installed, the data transceivers are disabled**
- **If the jumper IS installed, the data transceivers are enabled toward the FPGA to permit snooping bus activity that is not in the /CS1 or /CS5 spaces**

iMX21 External Interface Module (EIM)

- The EIM permits very fine-grained control of the bus interface
  - Bus width
  - Timing of /CSx assertion/negation
  - Timing of /OE, /WE assertion/negation
  - Dead cycles between transfers
  - DTACK sensitivity and sampling
  - Byte enable behavior
  - Burst mode

iMX21 EIM Timing Example

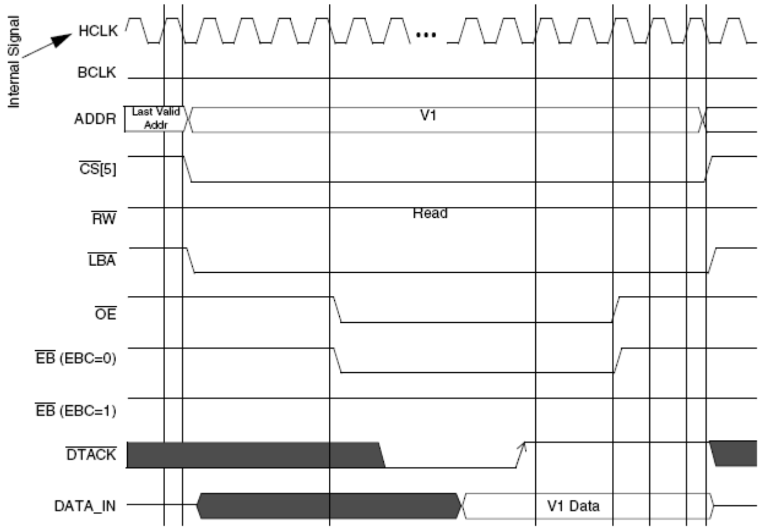
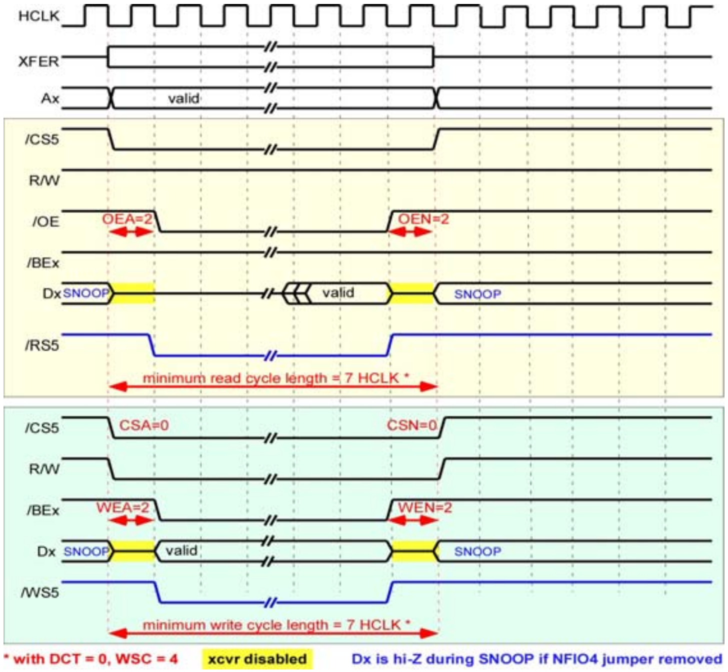


Figure 77. DTACK Edge Triggered Read Access, WSC=3F, OEA=8, OEN=5, AGE=1.

iMX21 Bus Timing with uMon Settings



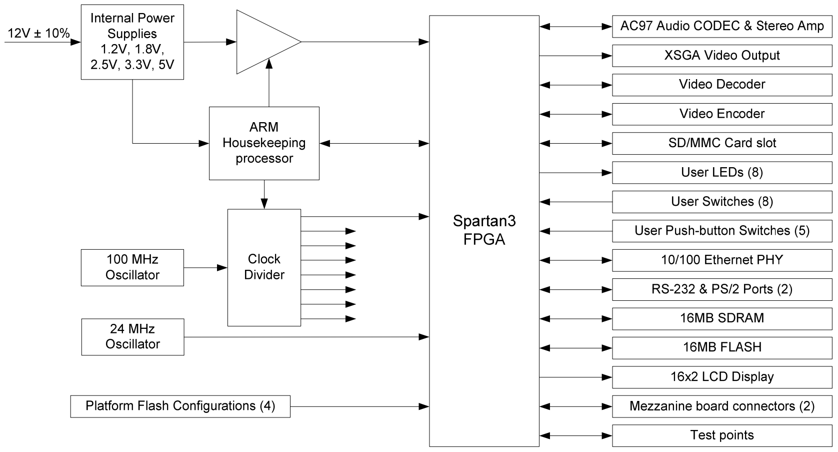
Chip Select configuration set uMon

- Chip Select 1 & 5 Upper Register settings in uMon
  - CS1U,CS5U = 0x00000480
    - DCT = 0, at least 2 HCLK before /DTACK checked
    - RWA = 0, R/W asserted when address valid
    - WSC = 4 wait states (minimum cycle = 6 HCLK)
    - EW = 1, level sensitive /DTACK

Chip Select configuration set uMon

- **Chip Select 1 & 5 Lower Register settings in uMon**
  - CS1L,CS5L = 0x22220E01
    - WEA = 2, byte enables asserted 2 half-clocks after start of access
    - WEN = 2, byte enables negated 2 half-clocks before end of access
    - OEA, OEN = 2, similar for /OE on reads
    - CSA = 0, /CS asserted when write starts
    - CSN = 0, /CS negated when write ends
    - EBC = 1, byte enables during writes only
    - DSZ = 6, 32-bit bus width
    - CSEN = 1, /CS enabled

TLL5000 Block Diagram


12V ± 10%
Internal Power Supplies 1.2V, 1.8V, 2.5V, 3.3V, 5V
ARM Housekeeping processor
Clock Divider
100 MHz Oscillator
24 MHz Oscillator
Platform Flash Configurations (4)
Spartan3 FPGA
AC97 Audio CODEC & Stereo Amp
XSGA Video Output
Video Decoder
Video Encoder
SD/MMC Card slot
User LEDs (8)
User Switches (8)
User Push-button Switches (5)
10/100 Ethernet PHY
RS-232 & PS/2 Ports (2)
16MB SDRAM
16MB FLASH
16x2 LCD Display
Mezzanine board connectors (2)
Test points