An Overview of the Virginia Tech Program in Software Radios Implemented with Reconfigurable Computing

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Web Address:
http://www.ee.vt.edu/mprg/research/glomo/index.html
Objective of the Project

• Design and build a high speed radio testbed using *configurable computing modules* and advanced receiver architectures
  → Improved capacity
  → Flexibility of platform
  → Increases in processing power of platform
• Demonstrate smart antennas at the handset
• Create a hardware/software testbed to prove networking concepts
Overview of the Presentation

• Software Radio Using Reconfigurable Computing
  → Introduction to Reconfigurable Computing
  → Example Application: Multiuser Detection
  → Architecture for a General Purpose Configurable Radio
  → Evolution of the Configurable Computing Platform and Configurable Radio

• Smart Antennas at the Handset
  → Project goals
  → Measurements
  → Hardware development
Introduction to Reconfigurable Computing

• Configurable Computing (CC) Attempts To Increase Performance And Silicon Utilization Efficiency Through Logic Recycling using FPGA and FPGA-like Devices

• Hardware Algorithms Can Be “Paged” Into/Out Of CC Modules Much As Operating Systems Perform Software Paging

• Factors Impacting the Performance
  → Logic Speed
  → Speed Of Reconfiguration
  → Flexibility Of Configuration
FPGAs vs. DSPs

- FPGAs can support multiple memory ports
- FPGAs outperform DSPs:
  - Parallelism in the algorithm
  - Simple operations in a fixed sequence
  - FPGAs provide greater computational density using less power
  - Large data sets, low resolution (8 - 12 bits)
  - Simple control
- DSPs outperform FPGAs
  - MAC operations
  - Complex arithmetic
Wormhole RTR Stream Format

Stream Format

Program/Flow Header

Data

Configuration information
→ Routing information
→ Variable size
→ Possibly removed as stream routes

Application data stream
→ Possibly chained
→ Variable size
Multiuser Receiver Data Flow

FROM DDC
ACTUAL RECV'D SIGNAL
BUFFER RECV'D SIGNAL & INITIALIZE STREAMS
MATCHED FILTER CORRELATOR
MATCHED FILTER CORRELATOR
ACQUISITION AND TRACKING
REGENERATE & COMBINE
ESTIMATED RECV'D SIGNAL
REGENERATE & COMBINE
GENERATE REVISED RECV'D SIGNAL & BUFFER
MATCHED FILTER CORRELATOR
MATCHED FILTER CORRELATOR
REVISED RECV'D SIGNAL
MATCHED FILTER CORRELATOR
DEMODULATE
OUTPUT
RECV'D DATA
Multiuser Receiver Hardware

RF Front End
Transmitter
Digital Downconverter
Host PC
Reconfigurable Computing Platform
Reconfigurable Computing Modules Under Development

- Turbo Coder/Decoder
- Equalizer/ Single User CDMA Receiver
- Symbol/Carrier/Code Synchronizers
- Next Modules
  - Generic sample rate converter
  - Coder/Decoder library
  - Demodulator library
Phase 1 Implementation of the Configurable Radio

Direction for replacement of DSP μP functions with reconfigurable computing
**Phase 3 Final Architecture**

**Features**
- Wider bandwidth front end
- Stallion processor
- Run-time reconfiguration
- Library of communication functions
Hardware Based Simulator

• Fast simulation engine by taking advantage of reconfigurable processor

• Supports radio development effort

PC
(Preprocessor for system configuration and for setting system parameters)

Enable
reset
init_stat
reg_length

External input

Ac
θ
mod_sel

2x1 MUX

Modulator

I
Q

Noise generator

I
Q

Receiver

(Demod and data decisions)

PC
(Post-processor for data collection and analysis)
Adaptive Antenna and Direction Finding Algorithms and Hardware
Third Generation Array

Applications

Demonstrate interference rejection through spatial filtering

Perform AoA estimation for position location applications

Study algorithm performance

Developing spatial channel models

Third Generation Array

Front End for Antenna 1

Front End for Antenna 8

Local Oscillator

ADC / DDC (SigTek ST-114)

DSP

TI C549/C541

Demodulator and Beamforming Algorithm

BPF

IF LPF

IF AMP

ADC / DDC

BPF

IF LPF

IF AMP

Local Oscillator

f=1982 MHz

f=1982 MHz

f=2050 MHz

f=2050 MHz
MPRG Vector Measurement System

- Fully functional 8 elements, 1.25 MHz Bandwidth, 2.050 GHz center frequency
- Flexible for adapting various antenna/polarization inputs, carrier frequencies, bandwidths, real-time algorithms, or data collection scenarios
- Eight Harris 40214 Programmable Direct Digital Downconverters, eight C54x DSPs, one Analog Devices 21010

- New features being added
  - CDMA capability
  - Improved system executive processing
Research Issues

- Adaptive array algorithm performance in real situations
- Vector channel measurements
- Practical AOA algorithm and hardware development
- Adaptive array algorithm convergence issues
Measurement Result

Signal strength using LSCMA

- Indoor environment
- 2.050 GHz carrier
- Stationary rx and tx
- 10 second collect
Circular Model (Macrocell)*

- Models macrocell environments
- Scatterers are uniformly distributed in a circular region about the mobile
- Approximate radius, $30 \text{ m} < R < 200 \text{ m}$
Joint TOA-AOA (Circular BS View)

\[ f_{\tau,\theta_b}(\tau, \theta_b) = \begin{cases} 
\frac{(D^2 - \tau^2c^2)(D^2c + \tau^2c^3 - 2\tau c^2 D \cos(\theta_b))}{4\pi R_m^2 (D \cos(\theta_b) - \tau c)^3} & : \frac{D^2 - 2\tau c D \cos(\theta_b) + \tau^2 c^2}{\tau c - D \cos(\theta_b)} \leq 2R_m \\
0 & : \text{else.}
\end{cases} \]

D = 1km
R_m = 100m
Summary of GloMo2 Accomplishments

• Over one hundred publications produced
• Three generations of smart antennas built
• Three spread spectrum receivers built
• Vector channel models created
• Fully reconfigurable radio being built