Embedded System Design and Modeling

EE382V, Fall 2008

Lecture Notes 1

Introduction

Dates: Sep 2, 2008
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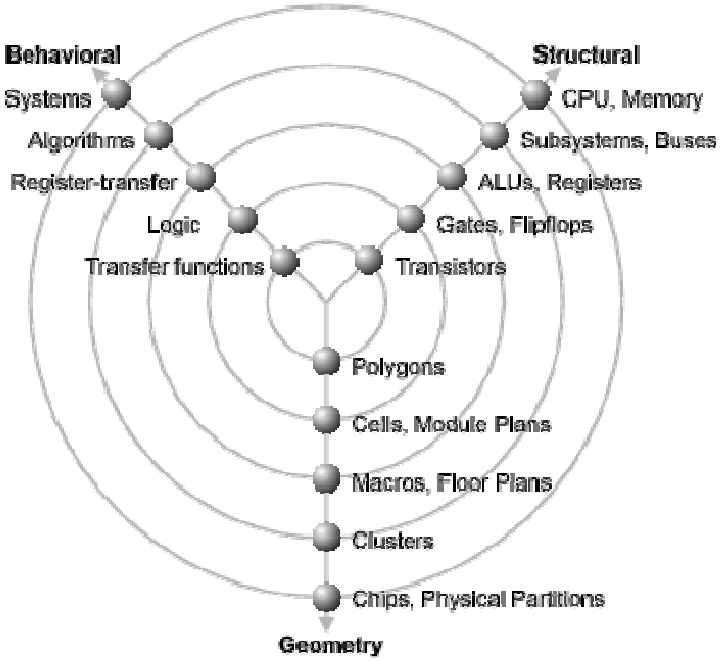
Gajski's Y Chart



Gajski's Y chart gives the different abstractions that can be used at 3 different design views namely: Behavioral, Structural and Geometry. The outermost circle is the highest level of abstraction and the level of detail increases as we move inwards.

A top down flow starts from the System level specification, say in SpecC, which represents the high level behavior of the system without the hardware/software partitioning. This is further partitioned into Hardware Components and Software Algorithms. The high level hardware specification is then synthesized into ALUs and registers which is at the RT-level (Verilog or VHDL). This RT-level specification is then passed through a logic synthesis tool to get the gate level specification.

A bottom up approach would have databases for the innermost abstractions starting with transistor, gates and so on. The libraries would have the specification of abstractions in the most general format. For eg. Gate level libraries would have 2-input, 3-input gates of different speeds and sizes.

A typical ASIC design flow would have combination of top down and bottom up flow, which usually meet at the gate level.

Q: Where do fpga's fit in?

FPGAs would largely have the same design methodology as ASICs except the estimates for area, power and timing would be based on FPGA synthesis instead of gate libraries as used for ASICs.

FPGAs are also used for prototyping even when the required end product is an ASIC.

Q: How does testing feature in the design methodology?

There are two broad categories for "testing". One is verification where the design is verified using formal verification and simulation tools to check if the design specification is meeting the requirements. This happens during the different stages in the design flow. The other category is testing where the chip is tested after tape-out to check if there are defects etc.

Platform Based Design:

Here the design involves the reuse of IP instead of designing hardware from scratch. So this is a strategy where the top down and bottom up methodology meet at the top (subsystems,buses level). This methodology is favorable because of its low time to market.

Lecture1, slide 13:

Partitioning is spatial (physical).

Scheduling is temporal (time based).

Design Space Exploration:

Even though the exact value of design space parameters such as area, power and timing will be clear only when we get to the physical layer the key to design space exploration is to abstract out the details such that the estimates of area, power and timing are fairly accurate.