Lecture 12: Outline

- System models
  - Specification model
  - Transaction-level models
  - Bus-cycle accurate model
  - Cycle-accurate model

- Modeling results
  - Accuracy vs. speed
System Design Flow

- Abstraction based on level of detail & granularity
- Computation and communication

- System design flow
  - Path from model A to model F

- Design methodology and modeling flow
  - Set of models and transformations between models


System Models

- From layers to system models…
**Specification Model**

- **Abstract, high-level system functionality**
  - Computation
    - Processes
    - Variables
  - Communication
    - Sync./async. message-passing
    - Memory interfaces
    - Events

**Network TLM**

- **Topology of communication architecture.**
  - PEs + Memories + CEs
  - Upper protocol layers inserted into PEs/CEs
  - Communication via point-to-point links
    - Synchronous packet transfers (data transfers)
    - Memory accesses (shared memory, memory-mapped I/O)
    - Events (control flow)
Protocol TLM

- Abstract component & bus structure/architecture
  - PEs + Memories + CEs + Busses
  - Communication layers down to protocol transactions
  - Communication via transaction-level channels
    - Bus protocol transactions (data transfers)
    - Synchronization events (interrupts)

Bus Cycle-Accurate Model (BCAM)

- Component & bus structure/architecture
  - PEs + Memories + CEs + Busses
  - Pin-accurate bus-functional components
  - Pin- and cycle-accurate communication
    - Bus and interrupt protocols
    - Pins and wires
Cycle-Accurate Model (CAM)

- Component & bus implementation
- PEs + Memories + CEs + Busses
- Cycle-accurate components
  - Instruction-set simulators (ISS) running final target binaries
  - RTL hardware models
  - Bus protocol state machines

Modeling Results

<table>
<thead>
<tr>
<th></th>
<th>Spec.</th>
<th>TLM (Net)</th>
<th>TLM (Prot)</th>
<th>BCAM</th>
<th>CAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation Time [s]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MP3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JPEG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GSM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Spec.</th>
<th>TLM (Net)</th>
<th>TLM (Prot)</th>
<th>BCAM</th>
<th>CAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Error [%]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MP3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JPEG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GSM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Lecture 12: Summary

• Modeling of system computation and communication
  • From specification
    – System behavior, Models of Computation (MoCs)
  • To implementation
    – Layers of implementation detail
      ➢ Flow of well-defined models as basis for automated design process

• Various level of abstraction, accuracy and speed
  • Functional specification
    – Native speeds but inaccurate
  • Traditional cycle-accurate model (CAM)
    – 100% accurate but slow
      ➢ Transaction-level models (TLMs)
        ➢ Fast and accurate virtual prototyping